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FAIRCHILD SEMICONDUCTOR®

June 2013

FAB1200 Class-G Ground-Referenced Headphone Amplifier with Integrated Buck Converter

Features

- Class-G Headphone Amplifier Uses Multiple Rails for High Efficiency
- Integrated Inductive Buck Converter for Direct Battery Connection
- Differential Analog Inputs
- Capable of Driving 16 Ω to 600 Ω Loads and Line Level Inputs
- Ground-Referenced Output
- Ground-Sense Input Eliminates Ground-Loop Noise
- I^2C Controls
  - 32-Step Volume Control
  - Channel-Independent Shutdown Control and Short-Circuit Protection
- 16-Bump, 0.4 mm Pitch, 1.56 mm x 1.56 mm WLCSP Package

Applications

- Cellular Handsets
- MP3 and Portable Media Players
- Personal Navigation Devices

Description

The FAB1200 is a stereo class-G headphone amplifier. A charge pump generates a negative supply voltage that allows its output to be ground centered. An integrated buck regulator adjusts the voltage supplies between two different levels based on the output signal level to reduce power consumption.

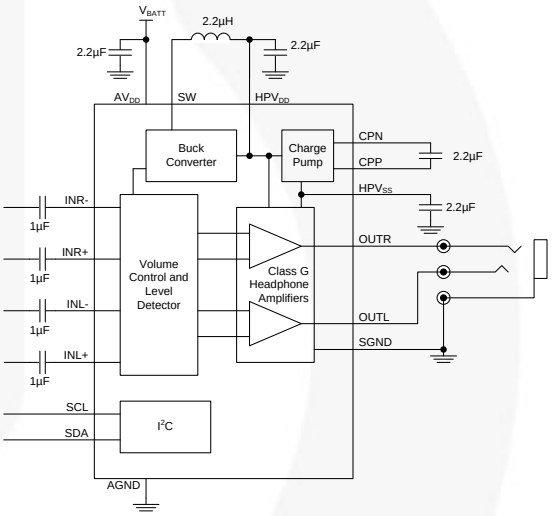

Figure 1. Typical Application Circuit

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAB1200UCX	-40 to +85°C	16-Bump, 0.4 mm Pitch, 1,56 mm x 1.56 mm, Wafer-Level Chip-Scale Package (WLCSP)	4000 Units on Tape & Reel

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Pin Configuration

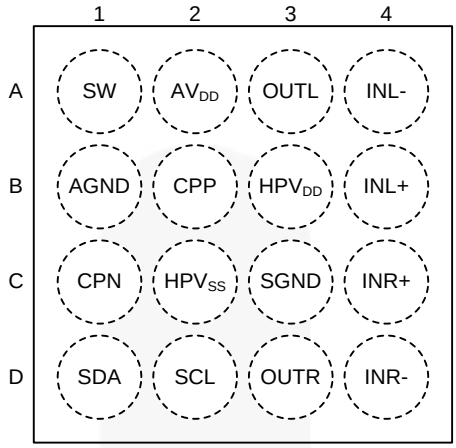

Figure 2. 16-Bump, 0.4 mm Pitch WLCSP Package (Top View)

Pin Definitions

WLCSP	Name	Description	Type
A1	SW	Buck converter switching node	Output
A2	AV_{DD}	Power supply for the device; connect to battery	Power
A3	OUTL	Left channel output	Output
A4	INL-	Left channel input, negative terminal	Input
B1	AGND	Main ground	Power
B2	CPP	Charge pump flying capacitor, positive terminal	Power
B3	HPV_{DD}	Power supply for headphone amplifier (DC-DC output)	Power
B4	INL+	Left channel input, positive terminal	Input
C1	CPN	Charge pump flying capacitor, negative terminal	Power
C2	HPV_{SS}	Charge pump output	Power
C3	SGND	Ground sense; connect to headphone jack ground	Input
C4	INR+	Right channel input, positive terminal	Input
D1	SDA	I^2C Serial Data (SDA) line	Bi-Directional
D2	SCL	I^2C Serial Clock (SCL) line	Input
D3	OUTR	Right channel output	Output
D4	INR-	Right channel input, negative terminal	Input

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
AV_{DD}	Supply Voltage	-0.3	6.0	V
HPV_{DD_AMP}	Amplifier Supply Voltage, HPV_{DD} Pin	-0.3	2.5	V
V_{IA}	INL+, INL-, INR+, INR- Voltage	HPV_{SS} - 0.3	HPV_{DD} + 0.3	V
V_{I2C}	I^2C Voltage	-0.3	AV_{DD} + 0.3	V
V_{OUT}	OUTL, OUTR Voltage	$-HPV_{SS}$ - 0.3	HPV_{DD} + 0.3	V
I_{BKD}	Output Protection Diodes Breakdown Continuous Current		200	mA

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+85	°C
	Storage Relative Humidity Range	15		70	%
T_L	Peak Reflow Temperature			+260	°C
Θ_{JA}	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		75		°C/W

Electrostatic Discharge Capability

Symbol	Parameter	Condition	Level	Unit
ESD	Human Body Model, JESD22-A114	According to JESD22-A114-B Level 2, Compatible with IEC61340-3-1: 2002 Level 2 or ESD-STM5.1-2001 Level 2 or MIL-STD-883E 3015.7 Level 2	±4000	V
	Charged Device Model, JESD22-C101	According to JESD22-C101-C Level III, Compatible with IEC61340-3-3 Level C4 or ESD-STM5.3.1-1999 Level C4	±1500	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Temperature Range	-40	+85	°C
AV_{DD}	Supply Voltage Range	2.5	5.5	V
t_{SLEW}	Power Supply Slew Rate		1	V/µs

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Electrical Characteristics

Unless otherwise noted, AV_{DD} = 3.6 V, Gain = 0d B, R_L = 15Ω + 32 Ω || 5 nF with audio measurements across the 32Ω || 5 nF load, f = 1 KHz, T_A = 25°C.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
I_{DD}	Quiescent Current	Both Channels Enabled, No Audio Signal			1.2	2.2	mA
I_S	Supply Current	Output: 2 x 100 µW at 3 dB Crest Factor, R_L = 32 Ω Only			2.6	3.5	mA
		Output: 2 x 500 µW at 3 dB Crest Factor, R_L = 32 Ω Only			4.4	5.5	
		Output: 2 x 1 mW at 3 dB Crest Factor, R_L = 32 Ω Only			5.7	7.5	
		HIZL = HIZR = 1			1.0	2.3	
I_{SD}	Shutdown Current	SWSBY = 1, Inputs AC Grounded, SCL and SDA Pulled HIGH			1.8	6.0	µA
t_{WK}	Wake-Up Time				1.5	5.0	ms
P_O	Output Power Per Channel (Outputs In Phase)	AV_{DD} = 2.7 V, THD < 1%, f = 1 KHz, R_L = 32 Ω Only			36		mW
		AV_{DD} = 2.7V, THD < 10%, f = 1 KHz, R_L = 32 Ω Only			48		
		AV_{DD} = 2.7V, THD < 1%, f = 1 KHz, R_L = 16 Ω Only			51		
HPV_{DD}	HIGH Rail Voltages	Buck and CP Output	Outer Rail	1.70	1.80	1.90	V
			Inner Rail	1.20	1.25	1.30	
HPV_{SS}	LOW Rail Voltages		Outer Rail	-1.90	-1.80	-1.70	
			Inner Rail	-1.30	-1.25	-1.20	
THD+N	Total Harmonic Distortion + Noise	700mV_{RMS}, 1 KHz			0.01	0.02	%
PSRR	Power Supply Rejection Ratio(1)	Gain 0 dB, 200 mV_{PP} Ripple at 217Hz		80	100		dB
V_{IN}	Input Voltage Range	Input Stage Does Not Clip			±1.4		Vp
CMRR	Common Mode Rejection Ratio	1 V_{PP}, f = 1 KHz, Gain 0 dB, R_L = 32 Ω Only			65		dB
SNR	Signal-to-Noise Ratio	1 V_{RMS}, f = 1 KHz, R_L = 32 Ω Only		100	106		dB
	Channel Separation	P_O = 15 mW, f = 1 KHz			80		dB
		R_L ≥ 16 Ω		75			dB
		Line Out >10KΩ(1)		80			
V_n	Output Noise	Gain 0dB, A-Weight, R_L = 32 Ω Only			4.7	9.0	$µV_{RMS}$
DC-Out	Output DC-Offset	Both Channels Enabled		-500		500	µV
	Gain Matching				1		%
	Mute Attenuation	MUTEx = 1			-110	-80	dB
		HIZx = 1				-80	

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Electrical Characteristics (Continued)

Unless otherwise noted, AV_{DD} = 3.6 V, Gain = 0 dB, R_L = 15 Ω + 32 Ω || 5 nF with audio measurements across the 32 Ω || 5 nF load, f = 1 KHz, T_A = 25°C.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Z_{IN}	Input Impedance	Differential		20.0			kΩ
	Differential Input Impedance	Gain = 0dB, per Input Node			38		
	Single Ended Input Impedance	Gain = 0dB, per Input Node			18		
Z_{OUT}	Output Impedance	HIZx = 1, SWSBY = 0	<40 kHz	10.0	11.5		kΩ
			6 MHz	500	1200		Ω
			13 MHz		800		Ω
			36 MHz	75	380		Ω
C_{LOAD}	Capacitive Load	ESD Protection, External Capacitor		0.8	5.0	100.0	nF
T_{SD}	Thermal Shutdown Threshold				150		°C
T_{HYS}	Thermal Shutdown Hysteresis				55		°C

Note:
1. Guaranteed by Characterization.

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I²C DC Characteristics

Unless otherwise noted, AV_{DD} = 2.5 V to 5.5 V and T_A = 25°C.

Symbol	Parameter	Conditions	Fast Mode (400kHz)		
			Min.	Max.	Unit
V_{IL}	Low-Level Input Voltage	AV_{DD} 2.9 to 4.5 V	-0.3	0.6	V
V_{IH}	High-Level Input Voltage	AV_{DD} 2.9 to 4.5 V	1.2		V
V_{OL}	Low-Level Output Voltage	at 3mA Sink Current (Open-Drain or Open-Collector)	0	0.4	V
I_{IH}	High-Level Input Current of Each I/O Pin	Input Voltage = A V_{DD}	-1	1	µA
I_{IL}	Low-Level Input Current of Each I/O Pin	Input Voltage = 0 V	-1	1	µA

I²C AC Electrical Characteristics

Unless otherwise noted, AV_{DD} = 2.5 V to 5.5 V and T_A = 25°C.

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	LOW Period of SCL Clock	1.3		µs
t_{HIGH}	HIGH Period of SCL Clock	0.6		µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time	0	0.9	µs
$t_{SU;DAT}$	Data Set-up Time(2)	100		ns
t_r	Rise Time of SDA and SCL Signals(3)	20+0.1C_b	300	ns
t_f	Fall Time of SDA and SCL Signals(3)	20+0.1C_b	300	ns
$t_{SU;STO}$	Set-up Time for STOP Condition	0.6		µs
t_{BUF}	Bus Free Time between STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

2. A fast-mode I²C-Bus® device can be used in a standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq$ 250ns LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r_max} + t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the standard-mode I²C bus specification) before the SCL line is released.
3. C_b equals the total capacitance of one bus line in pf. If mixed with high-speed mode devices, faster fall times are allowed according to the I²C specification.

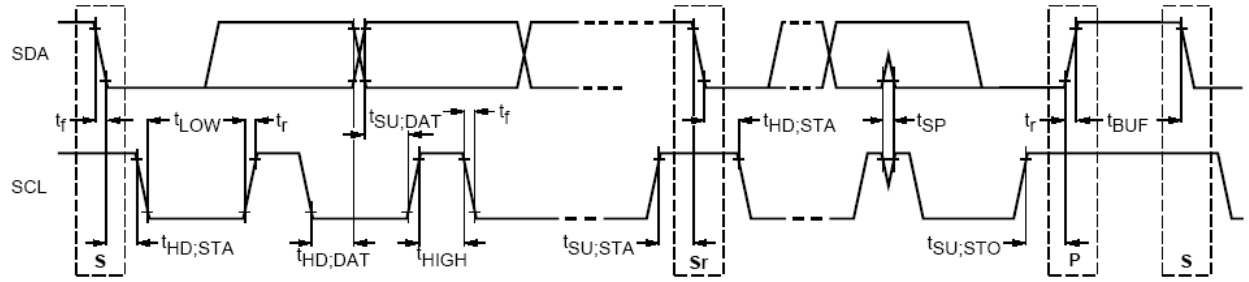

Figure 3. Definition of Timing for Full-Speed Mode Devices on the I²C Bus®

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Typical Characteristics

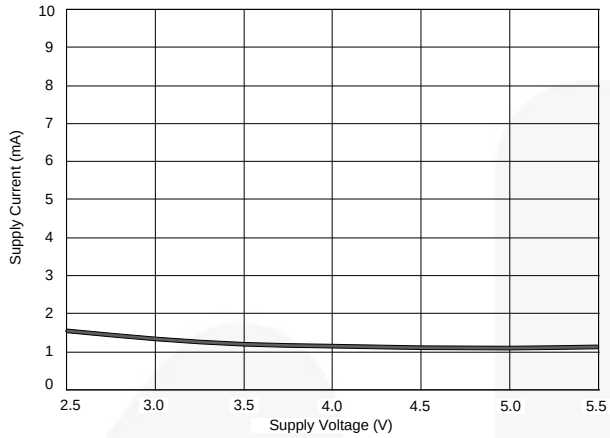

Figure 4. Quiescent Supply Current vs. Supply Voltage

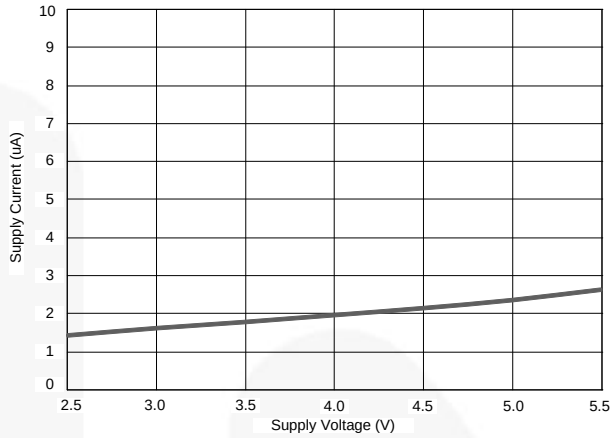

Figure 5. Shutdown Supply Current vs. Supply Voltage

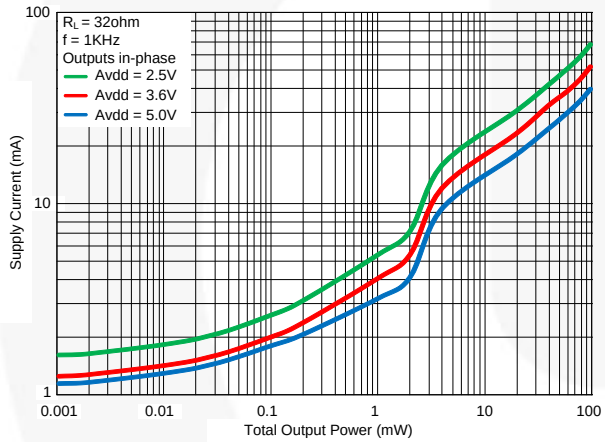

Figure 6. Supply Current vs. Total Output Power 32 Ω

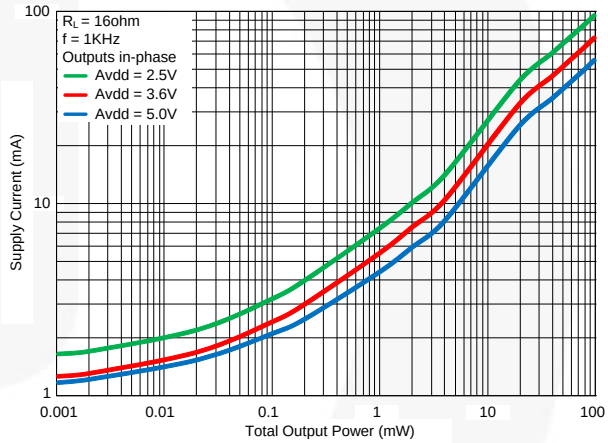

Figure 7. Supply Current vs. Total Output Power 16 Ω

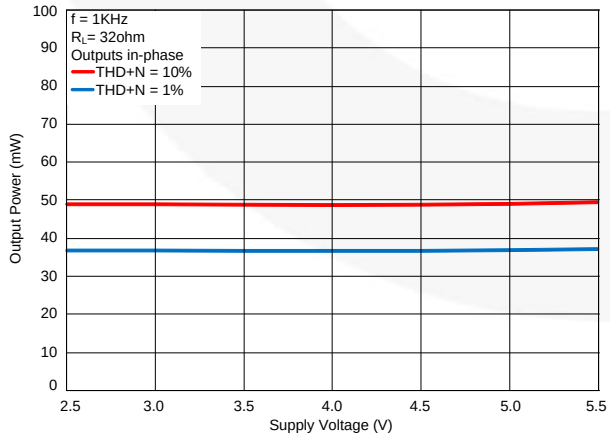

Figure 8. Output Power vs. Supply Voltage at 32 Ω

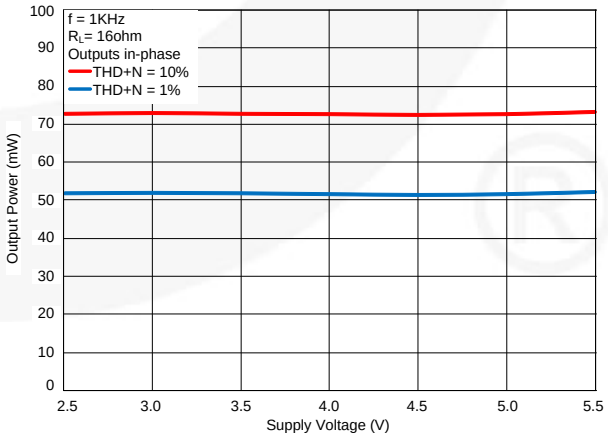

Figure 9. Output Power vs. Supply Voltage at 16 Ω

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Typical Characteristics

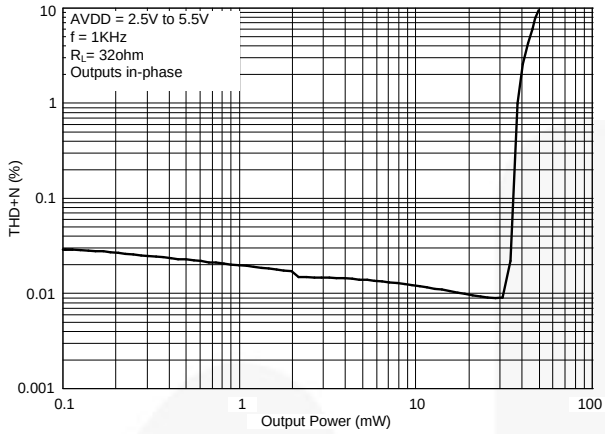

Figure 10. THD+N vs. Output Power at 32 Ω

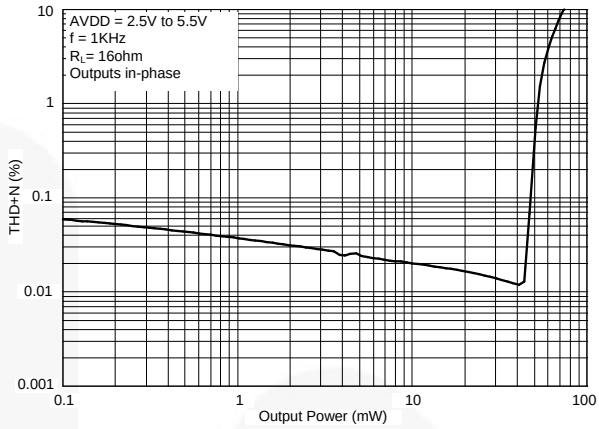

Figure 11. THD+N vs. Output Power at 16 Ω

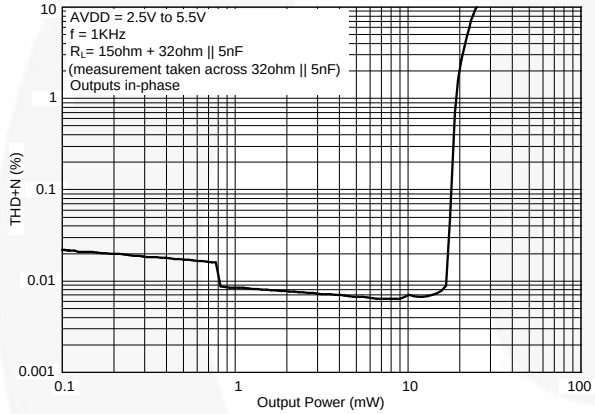

Figure 12. THD+N vs. Output Power

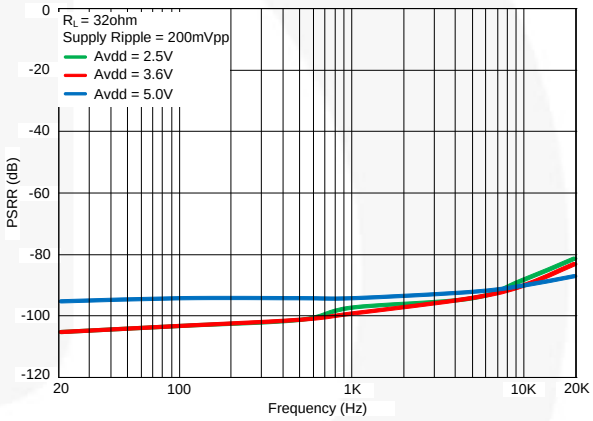

Figure 13. PSRR vs. Frequency

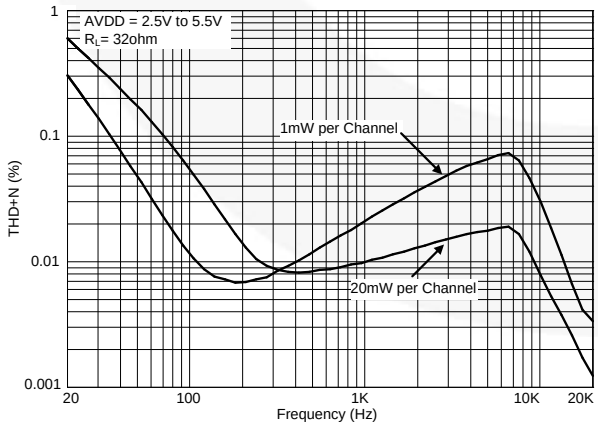

Figure 14. THD+N vs. Frequency at 32 Ω

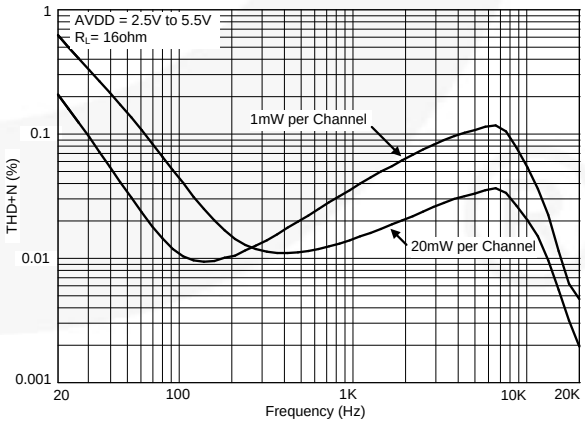

Figure 15. THD vs. Frequency at 16 Ω

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Typical Characteristics

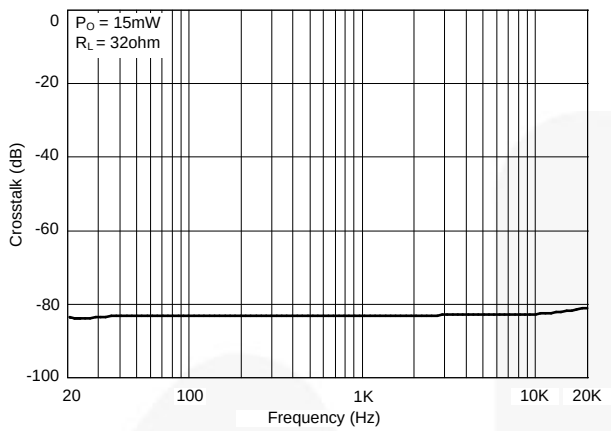

Figure 16. Crosstalk vs. Frequency at 32 Ω

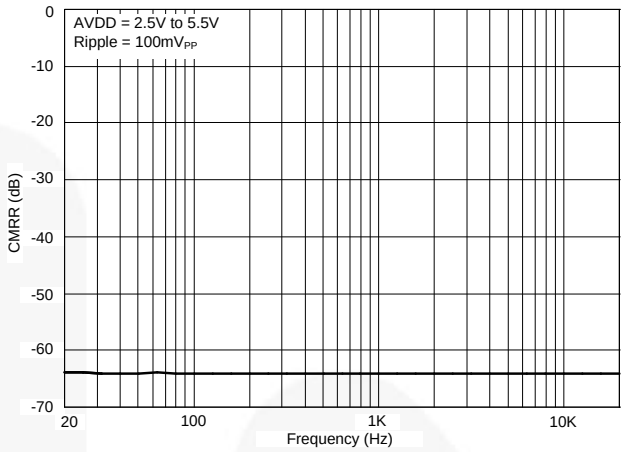

Figure 17. CMRR vs. Frequency

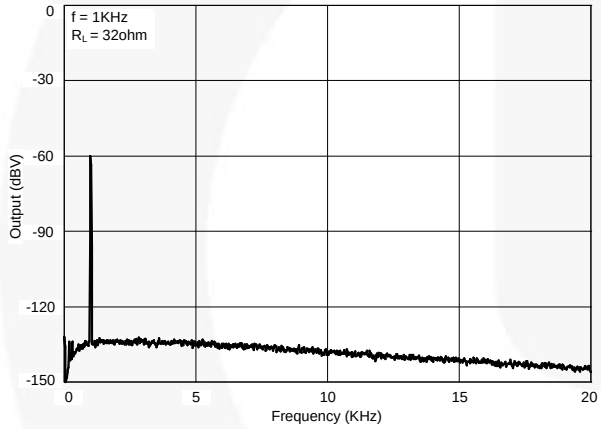

Figure 18. Output vs. Frequency at 32 Ω

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Functional Description

Class G

The FAB1200 uses a class-G headphone architecture for low power dissipation. An integrated converter creates the headphone amplifier positive supply voltage, HPV_{DD}. A charge pump inverts HPV_{DD} and creates an amplifier negative supply voltage, HPV_{SS}. This allows the headphone amplifier output to be centered at 0 V and eliminates the need for DC blocking capacitors.

When the output signal amplitude is low, the buck converter generates a low HPV_{DD} voltage. When needed, the buck converter generates a higher HPV_{DD} to accommodate higher amplitude output signals. This change occurs faster than audio signals so no distortion or clipping is introduced.

Thermal and Current Protection

If the junction temperature of the regulator or headphone amplifier exceeds limits (*see the Electrical Characteristics table*), the system is disabled for approximately one second and the THERM bit is set to one. After one second, the system is enabled. If the fault condition still exists, the system is disabled again. This cycle repeats until the fault condition is removed. The THERM bit stays set to 1 until the fault condition is removed and it is read.

Output current is limited to prevent internal damage. A signal that would exceeds current limits is clipped so that it falls within limits.

Shutdown

Setting the SWSBY bit to 1 places the device in a low-current shutdown state. The I^2C port is still active and register values are not lost. During shutdown, HPV_{DD} and HPV_{SS} are powered down. Therefore, no signal should be present at the inputs during shutdown. During shutdown, junction temperature is not monitored. If junction temperature exceeds limits during shutdown, the THERM bit does not set to 1.

Output Impedance

The FAB1200 headphone outputs can be placed in high-impedance mode by setting the HIZx bits to 1. This can be useful if the system's headphone jack is shared with other devices. For proper high-impedance operation, the device must not be in a shutdown or protection mode and voltages on OUTL and OUTR must not exceed ±1.8 V. Actual impedance values are shown in the Electrical Characteristics table.

Applications Information

Layout Considerations

General layout and supply bypassing play a major role in analog performance and thermal characteristics. Fairchild offers a demonstration board to guide layout and aid device evaluation. Contact a Fairchild representative for demonstration board information. Following this layout configuration provides optimum performance for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should always run on top of the ground plane.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Place bypass capacitors within 0.1 inches of the device power pin.
- Minimize all trace lengths to reduce series inductance.

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I²C Control

Writing to and reading from the registers is accomplished via the I²C interface. The I²C protocol requires that one device on the bus initiates and controls all read and write operations. This device is called the “master” device. The master device also generates the SCL signal, which is the clock signal for all other “slave” devices on the bus. The FAB1200 is a slave device. Both the master and slave devices can send and receive data on the bus.

During I²C operations, one data bit is transmitted per clock cycle. All I²C operations follow a repeating nine-clock-cycle pattern that consists of eight bits (one byte) of transmitted data followed by an acknowledge (ACK) or not acknowledge (NACK) from the receiving device. Note that there are no unused clock cycles during any operation; therefore, there must be no breaks in the stream of data and ACKs/NACKs during data transfers.

For most operations, I²C protocol requires the serial data (SDA) line remain stable (unmoving) whenever serial clock line (SCL) is HIGH: transitions on the SDA line can only occur when SCL is LOW. The exceptions to this rule are when the master device issues a START or STOP condition. The slave device cannot issue a START or STOP condition.

START Condition: This condition occurs when the SDA line transitions from HIGH to LOW while SCL is HIGH. The master device uses this condition to indicate that a data transfer is about to begin.

STOP Condition: This condition occurs when the SDA line transitions from LOW to HIGH while SCL is HIGH. The master device uses this condition to signal the end of a data transfer.

Acknowledge (ACK) and Not Acknowledge (NACK): When data is transferred to the slave device, it sends an acknowledge (ACK) after receiving every byte of data. The receiving device sends an ACK by pulling SDA LOW for one clock cycle.

When the master device is reading data from the slave device, the master sends an ACK after receiving every byte of data. Following the last byte, a master device sends a "not acknowledge" (NACK) instead of an ACK, followed by a STOP condition. A NACK is indicated by leaving SDA HIGH during the clock after the last byte.

Slave Address

Each slave device on the bus has a unique address so the master can identify which device is sending or receiving data. The FAB1200 slave address is 1100000X binary where “X” is the read/write bit. Master write operations are indicated when X=0. Master read operations are indicated when X=1.

Writing to and Reading from the FAB1200

All read and write operations must begin with a START condition generated by the master device. After the START condition, the master device must immediately send a slave address (7 bits), followed by a read/write bit. If the slave address matches the address of the FAB1200, the FAB1200 sends an ACK after receiving the read/write bit by pulling the SDA line LOW for one clock cycle.

Setting the Pointer

For all operations, the pointer stored in the command register must be pointing to the register to be written to or read from. To change the pointer value in the command register, the Read/Write bit following the address must be 0. This indicates that the master will write new information into the Command register.

After the FAB1200 sends an ACK in response to receiving the address and Read/Write bit, the master device must transmit an appropriate 8-bit pointer value, as explained in the I²C Registers section. The FAB1200 sends an ACK after receiving the new pointer data.

The pointer set operation is illustrated in Figure 21 and Figure 22. Any time a pointer set is performed, it must be immediately followed by a read or write operation. The Command register retains the current pointer value between operations; therefore, once a register is indicated, subsequent read operations do not require a pointer set cycle. Write operations always require the pointer be reset.

Reading

If the pointer is already pointing to the desired register, the master can read from that register by setting the Read/Write bit (following the slave address) to 1. After sending an ACK, the FAB1200 begins transmitting data during the following clock cycle. The master should respond with a NACK, followed by a STOP condition *(see Figure 19)*.

The master can read multiple bytes by responding to the data with an ACK instead of a NACK and continuing to send SCL pulses, as shown in Figure 20. The FAB1200 increments the pointer by one and sends the data from the next register. The master indicates the last data byte by responding with a NACK, followed by a STOP.

To read from a register other than the one currently indicated by the Command register, a pointer to the desired register must be set. Immediately following the pointer set, the master must perform a REPEAT START condition (*see Figure 22*), which indicates to the FAB1200 that a new operation is about to occur. If the REPEAT START condition does not occur, the FAB1200 assumes that a write is taking place and the selected register is overwritten by the upcoming data on the data bus. After the START condition, the master must again send the device address and Read/Write bit. This time, the Read/Write bit must be set to 1 to indicate a read. The rest of the read cycle is the same as described in the previous paragraphs for reading from a preset pointer location.

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Writing

All writes must be preceded by a pointer set, even if the pointer is already pointing to the desired register.

Immediately following the pointer set, the master must begin transmitting the data to be written. After transmitting each byte of data, the master must release the SDA line for one clock cycle to allow the FAB1200 to acknowledge receiving the byte. The write operation should be terminated by a STOP condition from the master *(see Figure 21).*

As with reading, the master can write multiple bytes by continuing to send data. The FAB1200 increments the pointer by ones and accept data for the next register. The master indicates the last data byte by issuing a STOP condition.

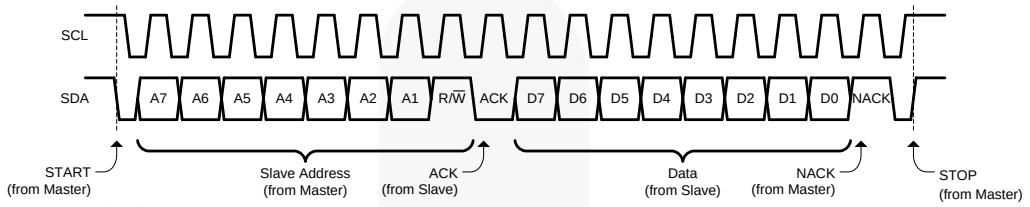

Figure 19. I²C Read

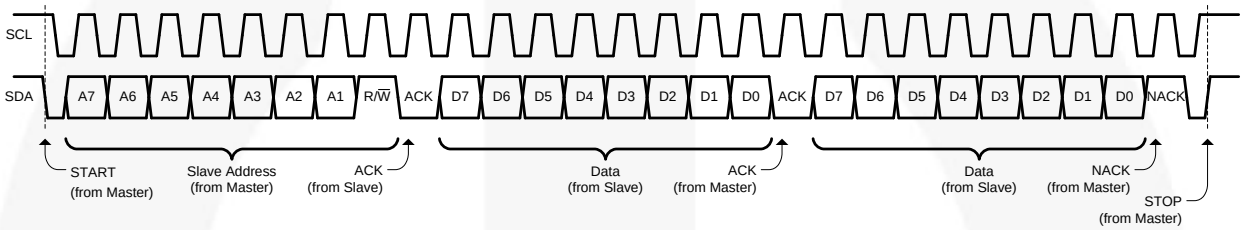

Figure 20. I²C Multiple-Byte Read

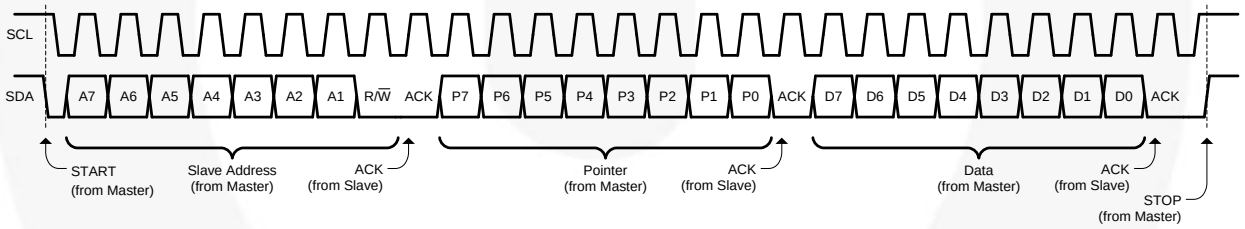

Figure 21. I²C Write

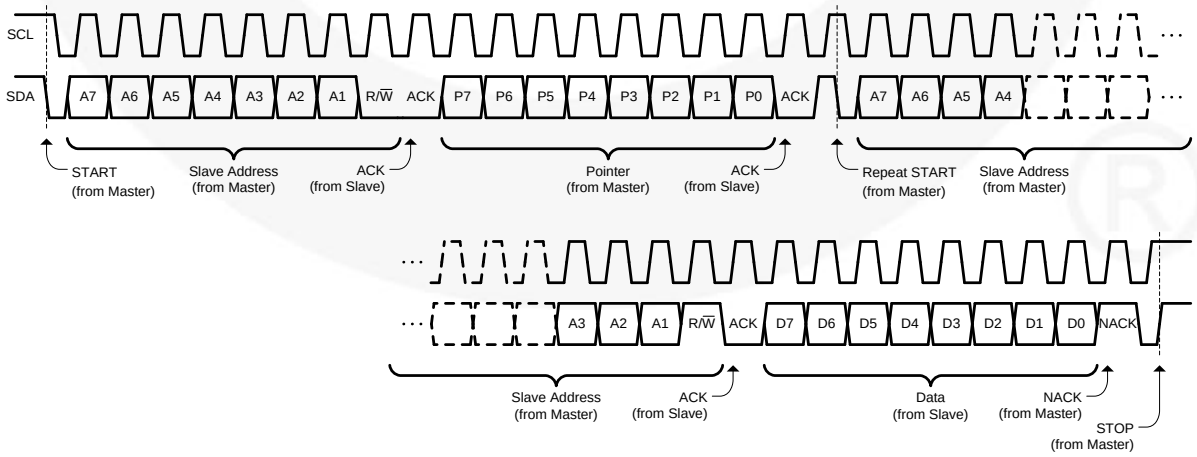

Figure 22. I²C Write Followed by Read

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I²C Registers

Table 1. Register Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	HPENL	HPENR	0	0	0	0	THERM	SWSBY
0x02	MUTEL	MUTER	VOL4	VOL3	VOL2	VOL1	VOL0	0
0x03	0	0	0	0	0	0	HIZL	HIZR
0x04	ID	ID	0	0	Revision 3	Revision 2	Revision 1	Revision 0

Notes:
4. Bits labeled “0” have no effect if written. When read, their value is always 0.
5. Bits not mentioned in the register map are for testing only. These bits should never be written. When read, they may return any value.

Table 2. Register 0x01

Bit	Label	R/W	Default	Description
0	SWSBY	R/W	1	1 = Low-power software standby. Charge pumps are turned off. I²C is still active. Register values are not lost during shutdown. 0 = Normal operation.
1	THERM	R	0	1 = A thermal shutdown has occurred. This bit stays set until it is read. 0 = No thermal shutdown.
5:2	0	R	0000	Value is always 0. No effect if written.
6	HPENR	R/W	0	1 = Enable right headphone amplifier. 0 = Disable right headphone amplifier.
7	HPENL	R/W	0	1 = Enable left headphone amplifier. 0 = Disable left headphone amplifier.

Table 3. Register 0x02

Bit	Label	R/W	Default	Description
0	0	R	0	Value is always 0. No effect if written.
5:1	VOL[4:0]	R/W	00000	00000 : -59 dB 11111 : +4 dB Audio taper over entire range *(see Table 6)*
6	MUTER	R/W	1	1 = Mute right channel. 0 = Un-mute right channel.
7	MUTEL	R/W	1	1 = Mute left channel. 0 = Un-mute left channel.

Table 4. Register 0x03

Bit	Label	R/W	Default	Description
0	HIZR	R/W	0	1 = 3-state right channel. 0 = Normal operation.
1	HIZL	R/W	0	1 = 3-state left channel. 0 = Normal operation.
7:2	0	R	000000	Value is always 0. No effect if written.

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Table 5. Register 0x04

Bit	Label	R/W	Default	Description
3:0	Revision[3:0]	R	0101	Denotes silicon revision.
5:4	0	R	00	Value is always 0. No effect if written.
7:6	ID[1:0]	R	00	Supplier identification.

Table 6. Volume Control

Volume Control Word	Gain (dB)	Volume Control Word	Gain (dB)
10xxxxxx	Mute_L	0001111x	-13
01xxxxxx	Mute_R	0010000x	-11
0000000x	-59	0010001x	-10
0000001x	-55	0010010x	-9
0000010x	-51	0010011x	-8
0000011x	-47	0010100x	-7
0000100x	-43	0010101x	-6
0000101x	-39	0010110x	-5
0000110x	-35	0010111x	-4
0000111x	-31	0011000x	-3
0001000x	-27	0011001x	-2
0001001x	-25	0011010x	-1
0001010x	-23	0011011x	0
0001011x	-21	0011100x	+1
0001100x	-19	0011101x	+2
0001101x	-17	0011110x	+3
0001110x	-15	0011111x	+4

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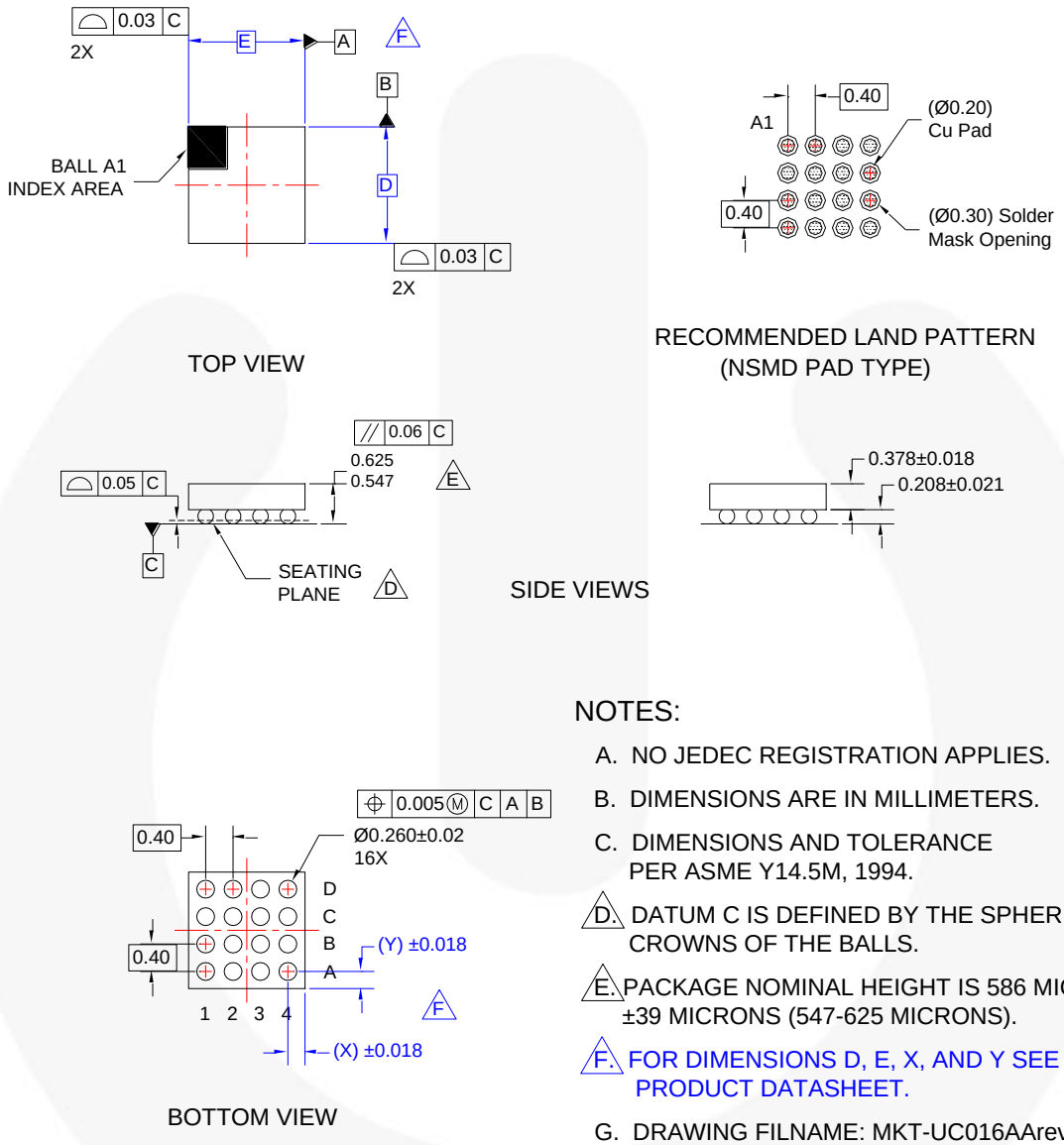
Physical Dimensions



NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC016AArev2.

Figure 23. 16-Ball WLCSP, 4x4 Array, 0.4 mm Pitch, 250 µm Ball

Product-Specific Dimensions

Product	D	E	X	Y
FAB1200UCX	1.56 mm	1.56 mm	0.18 mm	0.18 mm

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