5.7 kV rms/1.5 kV rms, Quad-Channel LVDS 2.5 Gigabit Isolators

FEATURES

- 5.7 kV rms and 1.5 kV rms LVDS isolators
- Complies with TIA/EIA-644-A LVDS signal levels
- Quad-channel configuration (ADN4622: 2 + 2, ADN4624: 4 + 0)
- Any data rate up to 2.5 Gbps switching with low jitter
  - 10 Gbps total bandwidth across four channels
  - 2.15 ns typical propagation delay
  - Typical jitter: 0.82 ps rms random, 40 ps total peak
- Lower power 1.8 V supplies
- ±8 kV IEC 61000-4-2 ESD protection across isolation barrier
- High common-mode transient immunity: 100 kV/µs typical
- Safety and regulatory approvals (28-lead SOIC_W_FP package)
  - UL (pending): 5700 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A (pending)
  - VDE certificate of conformity (pending)
    - DIN V VDE V 0884-11 (VDE V 0884-11):2017-01
    - V_{IORM} = 849 V_{PEAK} (working voltage)
- Enable or disable refresh (low-speed output correctness check)
- Operating temperature range: −40°C to +125°C
- 28-lead, wide-body, finer pitch SOIC_W_FP package with 8.3 mm creepage and clearance or 6 mm × 6 mm LFCSP package with 1.27 mm creepage and clearance

APPLICATIONS

- Isolated video and imaging data
- Analog front-end isolation
- Data plane isolation
- Isolated high speed clock and data links
- Multi-gigabit SERDES
- Board-to-board optical replacement (for example, short reach fiber)

FUNCTIONAL BLOCK DIAGRAMS

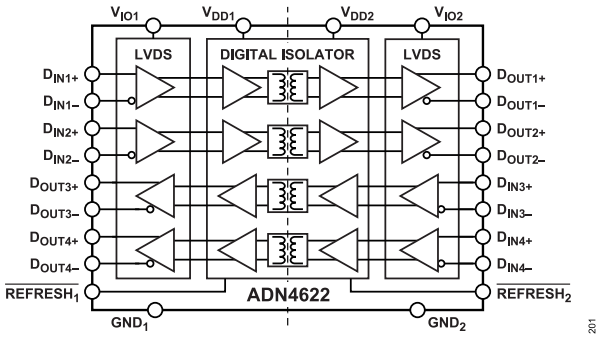

Figure 1. ADN4622 Functional Block Diagram with Two Forward and Two Reverse Channels

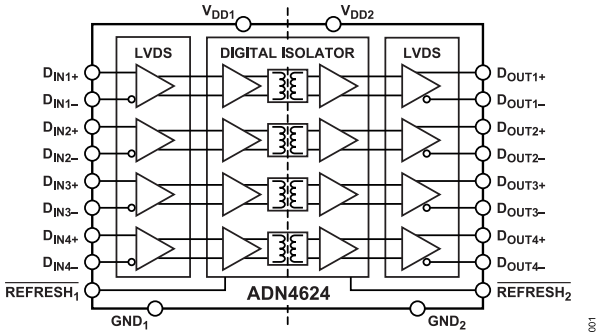

Figure 2. ADN4624 Functional Block Diagram with Four Forward Channels

GENERAL DESCRIPTION

The ADN4622/ADN4624[1] are quad-channel, signal isolated, low-voltage differential signaling (LVDS) buffers that operate at up to 2.5 Gbps with very low jitter. The devices integrate Analog Devices, Inc., *i*Coupler® technology, enhanced for high-speed operation to provide drop-in galvanic isolation of LVDS signal chains. AC coupling and/or level shifting to the LVDS receivers and from the LVDS drivers allows isolation of other high-speed signals such as current-mode logic (CML).

The ADN4622/ADN4624 include a refresh mechanism to monitor the input and output states and ensure they remain the same in the absence of data transitions. For lower power consumption and high-speed operation with low jitter, the LVDS and isolator circuits rely on 1.8 V supplies. The ADN4622/ADN4624 are fully specified over a wide industrial temperature range and are available in a 28-lead, wide-body, finer pitch SOIC_W_FP package with 8.3 mm creepage and clearance (for 5.7 kV rms or 8 kV_{PEAK} surge and impulse voltages and reinforced insulation at AC mains voltages) or 6 mm × 6 mm LFCSP package with 1.27 mm creepage and clearance (for basic/functional isolation).

[1] Protected by U.S. Patents 7,075,329; 9,941,565; and 10,205,442. Other patents are pending.

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10/2022—Rev. A to Rev. B

Added ADN4622 and Figure 1; Renumbered Sequentially ... 1
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Changes to Specifications Section and Table 1 Section ... 4
Changes to Channel to Channel Parameter, Table 3 ... 5
Changes to CSA (Pending), Standard Certification/Approval Column, Table 7 ... 7
Changes to Table 11 ... 9
Added Table 12 ... 10
Added Figure 5 and Table 18; Renumbered Sequentially ... 12
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Added Figure 8, Figure 9, Figure 11, and Figure 12 ... 15
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10/2021—Rev. 0 to Rev. A

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Changes to Features Section and General Description Section ... 1
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4/2021—Revision 0: Initial Version

SPECIFICATIONS

For all minimum and maximum specifications, V_{DD1} = 1.7 V to 1.9 V, V_{DD2} = 1.7 V to 1.9 V, V_{IO1} = 3 V to 3.6 V, V_{IO2} = 3 V to 3.6 V, and T_A = −40°C to +125°C, unless otherwise noted. For all typical specifications, V_{DD1} = V_{DD2} = 1.8 V, V_{IO1} = V_{IO2} = 3.3 V, and T_A = 25°C, unless otherwise noted. For all specifications, $\overline{REFRESH_1}$ = GND_1 and $\overline{REFRESH_2}$ = GND_2, unless otherwise noted.

Table 1. Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUTS (RECEIVERS)						
Input Threshold						See Figure 38 and Table 2
High	V_{TH}			100	mV	
Low	V_{TL}	−100			mV	
Differential Input Voltage	$\|V_{ID}\|$	100			mV	See Figure 38 and Table 2
Input Common-Mode Voltage	V_{IC}	$0.5\|V_{ID}\|$		$2.4 - 0.5\|V_{ID}\|$	V	See Figure 38 and Table 2
Input Current, High and Low	I_{IH}, I_{IL}	−5		+5	µA	One $D_{INx\pm}$ = 2.4 V or 0 V, another $D_{INx\pm}$ = 1.2 V, V_{DDx} = 1.8 V or 0 V, and V_{IOx} = 3.3 V or 0 V
Differential Input Capacitance[1]	$C_{INx\pm}$		1.7		pF	One $D_{INx\pm}$ = 0.4 sin(30 × 10^6πt) V + 0.5 V and another $D_{INx\pm}$ = 1.2 V[2]
LOGIC INPUTS						V_{DDx} = V_{DD1} for $\overline{REFRESH_1}$, V_{DDx} = V_{DD2} for $\overline{REFRESH_2}$
Input High Voltage	V_{INH}	0.65 V_{DDx}			V	
Input Low Voltage	V_{INL}			0.35 V_{DDx}	V	
Input-Current High	$\|I_{INH}\|$			1	µA	$\overline{REFRESH_x}$ = V_{DDx}
				25	µA	$\overline{REFRESH_x}$ = 1.9 V, V_{DDx} = 0 V
Input-Current Low	$\|I_{INL}\|$			16	µA	$\overline{REFRESH_x}$ = 0 V
OUTPUTS (DRIVERS)						
Differential Output Voltage	$\|V_{OD}\|$	250	310	450	mV	See Figure 36 and Figure 37, load resistance (R_L) = 100 Ω
V_{OD} Magnitude Change	$\Delta\|V_{OD}\|$			50	mV	See Figure 36 and Figure 37, R_L = 100 Ω
Offset Voltage	V_{OS}	1.125	1.17	1.375	V	See Figure 36, R_L = 100 Ω
V_{OS} Magnitude Change	ΔV_{OS}			50	mV	See Figure 36, R_L = 100 Ω
V_{OS}, Peak-to-Peak[1]	$V_{OS(PP)}$			150	mV	See Figure 36, R_L = 100 Ω
Output Short-Circuit Current	I_{OS}			−20	mA	$D_{OUTx\pm}$ = 0 V
				12	mA	$\|V_{OD}\|$ = 0 V
Differential Output Capacitance[1]	$C_{OUTx\pm}$		5		pF	One $D_{OUTx\pm}$ = 0.4 sin(30 × 10^6πt) V + 0.5 V, another $D_{OUTx\pm}$ = 1.2 V, and V_{DD1} or V_{DD2} = 0 V
ADN4622 SUPPLY CURRENT						
Supply Current Side 1	I_{DD1}		116	135	mA	Frequency (f) = 1.25 GHz, R_L = 100 Ω
			102	125		f = 1.25 GHz, R_L = 100 Ω, $\overline{REFRESH_1}$ = V_{DD1}
Supply Current Side 2	I_{DD2}		113	133	mA	f = 1.25 GHz, R_L = 100 Ω
			99	121	mA	f = 1.25 GHz, R_L = 100 Ω, $\overline{REFRESH_2}$ = V_{DD2}
V_{IO1} or V_{IO2} Supply	I_{IO1} or I_{IO2}		11	14	mA	f = 1.25 GHz
ADN4624 SUPPLY CURRENT						
Supply Current Side 1	I_{DD1}		140	175	mA	f = 1.25 GHz
Supply Current Side 2	I_{DD2}					
			115	140	mA	f = 1.25 GHz, R_L = 100 Ω
			95	135	mA	f = 1.25 GHz, R_L = 100 Ω, $\overline{REFRESH_2}$ = V_{DD2}
COMMON-MODE TRANSIENT IMMUNITY[3]	|CM|	40	100		kV/µs	Common-mode voltage (V_{CM}) = 1000 V, transient magnitude = 800 V

[1] These specifications are guaranteed by design and characterization.

[2] t denotes time.

[3] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining any D_{OUTx+} or D_{OUTx-} pin in the same state as the corresponding D_{INx+} or D_{INx-} pin (no change in output) or producing the expected transition on any D_{OUTx+} or D_{OUTx-} pin if the applied common-mode transient edge is coincident with a data transition on the corresponding D_{INx+} or D_{INx-} pin. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

SPECIFICATIONS

RECEIVER INPUT THRESHOLD TEST VOLTAGES

Table 2. Test Voltages for Receiver Operation

Applied Voltages				
D_{INx+} (V)	D_{INx-} (V)	Input Voltage, Differential, V_{ID} (V)	Input Voltage, Common-Mode, V_{IC} (V)	Driver Output, Differential V_{OD} (mV)
1.25	1.15	0.1	1.2	>250
1.15	1.25	−0.1	+1.2	<−250
2.4	2.3	0.1	2.35	>250
2.3	2.4	−0.1	+2.35	<−250
0.1	0	0.1	0.05	>250
0	0.1	−0.1	+0.05	<−250
1.5	0.9	0.6	1.2	>250
0.9	1.5	−0.6	+1.2	<−250
2.4	1.8	0.6	2.1	>250
1.8	2.4	−0.6	+2.1	<−250
0.6	0	0.6	0.3	>250
0	0.6	−0.6	+0.3	<−250

TIMING SPECIFICATIONS

For all minimum and maximum specifications, V_{DD1} = V_{DD2} = 1.7 V to 1.9 V and T_A = −40°C to +125°C, unless otherwise noted. For all typical specifications, V_{DD1} = V_{DD2} = 1.8 V and T_A = 25°C. For all specifications, $\overline{REFRESH_1}$ = V_{DD1} and $\overline{REFRESH_2}$ = V_{DD2}, unless otherwise noted.

Table 3. Timing Specifications

Parameter	Symbol	Min	Typ	Max[1]	Unit	Test Conditions/Comments
PROPAGATION DELAY	t_{PLH}, t_{PHL}		2.15	2.8	ns	See Figure 39, from any D_{INx+} and D_{INx-} to D_{OUTx+} and D_{OUTx-}
SKEW						See Figure 39, across all D_{OUTx+} and D_{OUTx-}
Duty Cycle[2]	$t_{SK(D)}$		2	16	ps	
Channel to Channel[3]	$t_{SK(CH)}$		40	120	ps	ADN4622 SOIC_W_FPpackage
			38	92	ps	ADN4624 SOIC_W_FP package
			40	114	ps	ADN4622 LFCSP package
			29	67	ps	ADN4624 LFCSP package
			20	60	ps	ADN4622 Channel 1 to Channel 2, or Channel 3 to Channel 4 only
Part to Part[4]	$t_{SK(PP)}$		150	300	ps	
JITTER[5]						See Figure 39, for any D_{OUTx+} and D_{OUTx-}
Random Jitter, RMS[6] (1σ)	$t_{RJ(RMS)}$		0.82	1.44	ps rms	1.25 GHz clock input
Deterministic Jitter, Peak-to-Peak[6, 7]	$t_{DJ(PP)}$		28	54	ps	2.5 Gbps, 2^{23} − 1 pseudorandom bit stream (PRBS)
Total Jitter, Peak-to-Peak, at Bit Error Rate (BER) 1 × 10^{-12}	$t_{TJ(PP)}$		40	70	ps	1.25 GHz/2.5 Gbps, 2^{23} − 1 PRBS[8]
With Crosstalk			50		ps	1.25 GHz/2.5 Gbps, 2^{23} − 1 PRBS all channels[8]
With Crosstalk and Refresh			55		ps	1.25 GHz/2.5 Gbps, 2^{23} − 1 PRBS all channels, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2[8]
Additive Phase Jitter	t_{ADDJ}					
SOIC_W_FP Package			225		fs rms	100 Hz to 100 kHz, output frequency (f_{OUT}) = 10 MHz[9]
			270		fs rms	100 Hz to 100 kHz, f_{OUT} = 10 MHz, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2[9]
			85		fs rms	12 kHz to 20 MHz, f_{OUT} = 1.25 GHz[10]
			200		fs rms	12 kHz to 20 MHz, f_{OUT} = 1.25 GHz, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2[10]
LFCSP Package			152		fs rms	100 Hz to 100 kHz, output frequency (f_{OUT}) = 10 MHz[9]
			182		fs rms	100 Hz to 100 kHz, f_{OUT} = 10 MHz, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2[9]

SPECIFICATIONS

Table 3. Timing Specifications

Parameter	Symbol	Min	Typ	Max[1]	Unit	Test Conditions/Comments
			152		fs rms	12 kHz to 20 MHz, f_{OUT} = 1.25 GHz[10]
			348		fs rms	12 kHz to 20 MHz, f_{OUT} = 1.25 GHz, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2[10]
RISE AND FALL TIME	t_R, t_F			180	ps	See Figure 39, 1.25 GHz clock input, any D_{OUTx+} and D_{OUTx-}, 20% to 80%, R_L = 100 Ω, load capacitance (C_L) = 5 pF
MAXIMUM DATA RATE		2.5			Gbps	

1 These specifications are guaranteed by design and characterization.

2 Duty cycle or pulse skew is the magnitude of the maximum difference between t_{PLH} and t_{PHL} for any Channel x of a device (where x = 1, 2, 3, or 4), that is, $|t_{PLHx} - t_{PHLx}|$.

3 Channel to channel or output skew is the difference between the largest and smallest values of t_{PLHx} within a device or the difference between the largest and smallest values of t_{PHLx} within a device, whichever of the two is greater.

4 Part to part output skew is the difference between the largest and smallest values of t_{PLHx} across multiple devices or the difference between the largest and smallest values of t_{PHLx} across multiple devices, whichever of the two is greater.

5 Jitter parameters are guaranteed by design and characterization. Values do not include stimulus jitter. V_{ID} = 400 mV p-p, V_{IC} = 1.2 V, and t_R / t_F < 0.05 ns (20% to 80%).

6 This specification is measured over a population of ~3,000,000 edges.

7 Peak-to-peak jitter specifications include jitter due to pulse skew ($t_{SK(D)}$).

8 Using the following formula: $t_{TJ(PP)} = 14 \times t_{RJ(RMS)} + t_{DJ(PP)}$.

9 With an input phase jitter of 340 fs rms subtracted.

10 With an input phase jitter of 155 fs rms subtracted.

INSULATION AND SAFETY RELATED SPECIFICATIONS

For additional information, see www.analog.com/icouplersafety.

Table 4. RN-28-1 Wide Body with Finer Pitch [SOIC_W_FP] Package

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5.7	kV rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material Group per IEC 60664-1

Table 5. CP-32-32 Lead Frame Chip-Scale Package [LFCSP]

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		1.5	kV rms	1 minute duration
Minimum External Air Gap (Clearance)	L (I01)	1.27	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	1.27	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	1.27	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	Tested in accordance to IEC 60112
Material Group		I		Material Group per IEC 60664-1

SPECIFICATIONS

PACKAGE CHARACTERISTICS

Table 6. RN-28-1 Wide Body with Finer Pitch [SOIC_W_FP] Package and CP-32-32 Lead Frame Chip-Scale Package [LFCSP]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	Voltage (input to output) (V_{I-O}) = 500 V DC
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		3.4		pF	

1 The device is considered a 2-terminal device: Pin 1 through Pin 14 are shorted together (Pin 1 through Pin 16 for LFCSP), and Pin 15 through Pin 28 are shorted together (Pin 17 through Pin 32 for LFCSP).

2 Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 14 and the Insulation Lifetime section for details regarding the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 7. RN-28-1 Wide-Body with Finer Pitch [SOIC_W_FP] Package

Regulatory Agency	Standard Certification/Approval	File
UL (Pending)	To be recognized under UL 1577 Component Recognition Program[1] Single protection, 5700 V rms isolation voltage	E214100
CSA (Pending)[2]	To be approved under CSA Component Acceptance Notice 5A CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 third edition Basic insulation at 830 V rms Reinforced insulation at 415 V rms CSA 61010-1-12+A1 and IEC 61010-1 third edition Basic insulation at 600 V rms Reinforced insulation at 300 V rms CSA 60601-1:14 and IEC60601-1 third edition+A1 1 means of patient protection (MOPP) for 261 V rms	205078
VDE (Pending)	To be certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01[3] Reinforced insulation, V_{IORM} = 849 V_{PEAK}, V_{IOSM} = 8000 V_{PEAK}	2471900-4880-0001
CQC (Pending)	To be certified according to GB4943.1-2011 per CQC11-471543-2015 Basic insulation at 820 V rms (1159 V_{PEAK}) Reinforced insulation at 410 V rms (578 V_{PEAK})	Pending

1 In accordance with UL 1577, each ADN4622/ADN4624 is proof tested by applying an insulation test voltage ≥6840 V rms for 1 sec.

2 Working voltages are quoted for Pollution Degree 2, Material Group III. ADN4622/ADN4624 case material has been evaluated by CSA as Material Group I.

3 In accordance with DIN V VDE V 0884-11, each ADN4622/ADN4624 is proof tested by applying an insulation test voltage ≥1592 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

Table 8. CP-32-32 Lead Frame Chip-Scale Package [LFCSP]

Regulatory Agency	Standard Certification/Approval	File
UL (Pending)	To be recognized under UL 1577 Component Recognition Program[1] Single protection, 1500 V rms isolation voltage	E214100
CSA (Pending)	To be approved under CSA Component Acceptance Notice 5A	205078
VDE (Pending)	To be certified according to DIN V VDE V 0884-11 (VDE V 0884-11):2017-01[2] Reinforced insulation, V_{IORM} = 560 V_{PEAK}, V_{IOSM} = 8000 V_{PEAK}	2471900-4880-0001
CQC (Pending)	To be certified according to GB4943.1-2011 per CQC11-471543-2015	Pending

1 In accordance with UL 1577, each ADN4622/ADN4624 is proof tested by applying an insulation test voltage ≥1800 V rms for 1 sec.

2 In accordance with DIN V VDE V 0884-11, each ADN4622/ADN4624 is proof tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).

SPECIFICATIONS

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data.

Table 9. RN-28-1 Wide Body with Finer Pitch [SOIC_W_FP] Package

Description	Test Conditions/Comments[1]	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{PD\ (M)}$, 100% production test, t_{INI} = t_M = 1 sec, partial discharge < 5 pC	$V_{PD\ (m)}$	1592	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{PD\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		1274	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		1019	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	8000	V_{PEAK}
Surge Isolation Voltage				
Basic	V_{PEAK} = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	16,000	V_{PEAK}
Reinforced	V_{PEAK} = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.74	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

[1] For information about t_M, t_{INI}, and V_{IO}, see DIN V VDE V 0884-11.

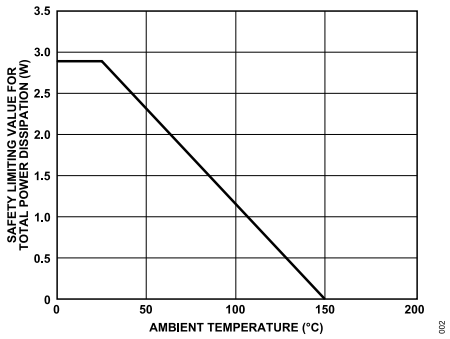

Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-11, SOIC_W_FP

SPECIFICATIONS

Table 10. CP-32-32 Lead Frame Chip-Scale Package [LFCSP]

Description	Test Conditions/Comments[1]	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to III	
For Rated Mains Voltage ≤ 300 V rms			I to II	
For Rated Mains Voltage ≤ 400 V rms			I	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V_{PEAK}
Input to Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{PD\ (M)}$, 100% production test, t_{INI} = t_M = 1 sec, partial discharge < 5 pC	$V_{PD\ (m)}$	1050	V_{PEAK}
Input to Output Test Voltage, Method A		$V_{PD\ (m)}$		
After Environmental Tests Subgroup 1	V_{IORM} × 1.5 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		840	V_{PEAK}
After Input or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{PD\ (M)}$, t_{INI} = 60 sec, t_M = 10 sec, partial discharge < 5 pC		672	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	2500	V_{PEAK}
Surge Isolation Voltage				
Basic	V_{PEAK} = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	16,000	V_{PEAK}
Reinforced	V_{PEAK} = 16 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	4.12	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	>10^9	Ω

[1] For information about t_M, t_{INI}, and V_{IO}, see DIN V VDE V 0884-11.

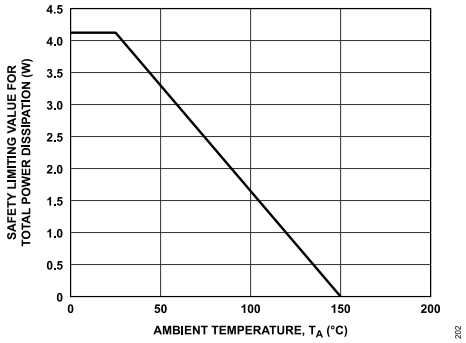

Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-11, LFCSP

RECOMMENDED OPERATING CONDITIONS

Table 11. Recommended Operating Conditions

Parameter	Symbol	Rating
Operating Temperature	T_A	−40°C to +125°C
V_{DDx} Supply Voltage Side 1 or Side 2	V_{DD1}, V_{DD2}	1.7 V to 1.9 V
V_{IOx} Supply Voltage Side 1 or Side 2	V_{IO1}, V_{IO2}	3 V to 3.6 V

ABSOLUTE MAXIMUM RATINGS

Table 12. Absolute Maximum Ratings

Parameter	Rating
V_{DD1} to GND_1, V_{DD2} to GND_2	−0.3 V to +2 V
V_{IO1} to GND_1, V_{IO2} to GND_2	−0.3 V to +4 V
Input Voltage $\overline{REFRESH_1}$ to GND_1, $\overline{REFRESH_2}$ to GND_2	−0.3 V to +2 V
Input Voltage (D_{INx+}, D_{INx-}) to GND_x on the Same Side	−0.3 V to +4 V
Output Voltage (D_{OUTx+}, D_{OUTx-}) to GND_x on the Same Side	−0.3 V to +2 V
Short-Circuit Duration (D_{OUTx+}, D_{OUTx-}) to GND_x on the Same Side	Continuous
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J Maximum)	150°C
Power Dissipation	(T_J maximum − T_A)/θ_{JA}

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 13. Maximum Continuous Working Voltage, RN-28-1 Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP] Package

Parameter[1]	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	650 V rms	Basic insulation rating per IEC60747-17. Accumulative failure rate over lifetime (FROL) ≤ 1000 ppm at 20 years.
Reinforced Insulation	600 V rms	Reinforced insulation rating per IEC60747-17. Accumulative FROL ≤ 1 ppm at 26 years.
Unipolar Waveform		
Basic Insulation	1782 V_{PEAK}	Rating limited by AC bipolar waveform accumulative FROL ≤ 1000 ppm at 20 years.
Reinforced Insulation	1330 V_{PEAK}	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
DC Voltage		
Basic Insulation	1660 V DC	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
Reinforced Insulation	830 V DC	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment. See the Insulation Lifetime section for more details.

Table 14. Maximum Continuous Working Voltage, CP-32-32 Lead Frame Chip-Scale Package [LFCSP]

Parameter[1]	Rating	Constraint
AC Voltage		
Bipolar Waveform		
Basic Insulation	253 V rms	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
Reinforced Insulation	63 V rms	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
Unipolar Waveform		
Basic Insulation	413 V_{PEAK}	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
Reinforced Insulation	102 V_{PEAK}	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
DC Voltage		
Basic Insulation	253 V DC	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.
Reinforced Insulation	63 V DC	Rating limited by package creepage per IEC 60664-1 in Pollution Degree 2 environment.

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier in a Pollution Degree 2 environment. See the Insulation Lifetime section for more details.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operation environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

Table 15. Thermal Resistance

Package Type[1]	θ_{JA}	Unit
RN-28-1	43.45	°C/W
CP-32-32	30.3	°C/W

[1] Test Condition 1: thermal impedance simulated with 4-layer standard JEDEC PCB.

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2.

ESD Ratings for ADN4622/ADN4624

Table 16. ADN4622/ADN4624, 28-Lead SOIC_W_FP

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±4000	3A
IEC[2]	±8000 (contact discharge)	Level 4

[1] All pins to respective GNDx, 1.5 kΩ, 100 pF.

[2] LVDS pins to isolated GNDx across isolation barrier.

Table 17. ADN4622/ADN4624, 32-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±4000	3A
IEC[2]	±2000 (contact discharge)	Level 1

[1] All pins to respective GNDx, 1.5 kΩ, 100 pF.

[2] LVDS pins to isolated GNDx across isolation barrier.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

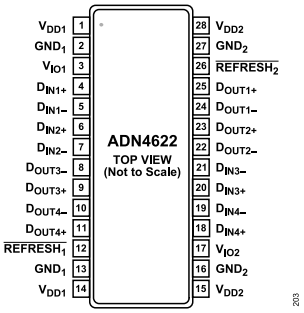

Figure 5. ADN4622 SOIC_W_FP Pin Configuration

Table 18. ADN4622 SOIC_W_FP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 14	V_{DD1}	1.8 V Power Supply for Side 1. Connect both pins externally and bypass to the adjacent GND_1 pins with 0.1 µF capacitors.
2, 13	GND_1	Ground, Side 1.
3	V_{IO1}	3.3 V Input and Output Power Supply for Side 1. Bypass to the adjacent GND_1 pin with a 0.1 µF capacitor.
4	D_{IN1+}	Noninverted Differential Input 1.
5	D_{IN1-}	Inverted Differential Input 1.
6	D_{IN2+}	Noninverted Differential Input 2.
7	D_{IN2-}	Inverted Differential Input 2.
8	D_{OUT3-}	Inverted Differential Output 3.
9	D_{OUT3+}	Noninverted Differential Output 3.
10	D_{OUT4-}	Inverted Differential Output 4.
11	D_{OUT4+}	Noninverted Differential Output 4.
12	$\overline{REFRESH_1}$	Active-Low Enable for Side 1 Refresh Function. Short to GND_1 for normal operation with refresh enabled, or short to V_{DD1} for lower power, lower jitter, and quieter operation with refresh disabled.
15, 28	V_{DD2}	1.8 V Power Supply for Side 2. Connect both pins externally and bypass to the adjacent GND_2 pins with 0.1 µF capacitors.
16, 27	GND_2	Ground, Side 2.
17	V_{IO2}	3.3 V Input and Output Power Supply for Side 2. Bypass to the adjacent GND_2 pin with a 0.1 µF capacitor.
18	D_{IN4+}	Noninverted Differential Input 4.
19	D_{IN4-}	Inverted Differential Input 4.
20	D_{IN3+}	Noninverted Differential Input 3.
21	D_{IN3-}	Inverted Differential Input 3.
22	D_{OUT2-}	Inverted Differential Output 2.
23	D_{OUT2+}	Noninverted Differential Output 2.
24	D_{OUT1-}	Inverted Differential Output 1.
25	D_{OUT1+}	Noninverted Differential Output 1.
26	$\overline{REFRESH_2}$	Active-Low Enable for Side 2 Refresh Function. Short to GND_2 for normal operation with refresh enabled, or short to V_{DD2} for lower power, lower jitter, and quieter operation with refresh disabled.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

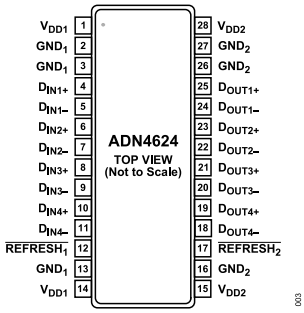

Figure 6. ADN4624 SOIC_W_FP Pin Configuration

Table 19. ADN4624 SOIC_W_FP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 14	V_{DD1}	1.8 V Power Supply for Side 1. Connect both pins externally and bypass to the adjacent GND_1 pins with 0.1 µF capacitors.
2, 3, 13	GND_1	Ground, Side 1.
4	D_{IN1+}	Noninverted Differential Input 1.
5	D_{IN1-}	Inverted Differential Input 1.
6	D_{IN2+}	Noninverted Differential Input 2.
7	D_{IN2-}	Inverted Differential Input 2.
8	D_{IN3+}	Noninverted Differential Input 3.
9	D_{IN3-}	Inverted Differential Input 3.
10	D_{IN4+}	Noninverted Differential Input 4.
11	D_{IN4-}	Inverted Differential Input 4.
12	$\overline{REFRESH_1}$	Active-Low Enable for Side 1 Refresh Function. Short to GND_1 for normal operation with refresh enabled, or short to V_{DD1} for lower power, lower jitter, and quieter operation with refresh disabled.
15, 28	V_{DD2}	1.8 V Power Supply for Side 2. Connect both pins externally and bypass to the adjacent GND_2 pins with 0.1 µF capacitors.
16, 26, 27	GND_2	Ground, Side 2.
17	$\overline{REFRESH_2}$	Active-Low Enable for Side 2 Refresh Function. Short to GND_2 for normal operation with refresh enabled, or short to V_{DD2} for lower power, lower jitter, and quieter operation with refresh disabled.
18	D_{OUT4-}	Inverted Differential Output 4.
19	D_{OUT4+}	Noninverted Differential Output 4.
20	D_{OUT3-}	Inverted Differential Output 3.
21	D_{OUT3+}	Noninverted Differential Output 3.
22	D_{OUT2-}	Inverted Differential Output 2.
23	D_{OUT2+}	Noninverted Differential Output 2.
24	D_{OUT1-}	Inverted Differential Output 1.
25	D_{OUT1+}	Noninverted Differential Output 1.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

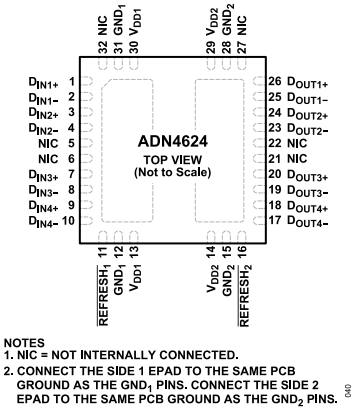

Figure 7. ADN4624 LFCSP Pin Configuration

Table 20. ADN4624 LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D_{IN1+}	Noninverted Differential Input 1.
2	D_{IN1-}	Inverted Differential Input 1.
3	D_{IN2+}	Noninverted Differential Input 2.
4	D_{IN2-}	Inverted Differential Input 2.
5, 6, 21, 22, 27, 32	NIC	Not Internally Connected. These pins are not internally connected.
7	D_{IN3+}	Noninverted Differential Input 3.
8	D_{IN3-}	Inverted Differential Input 3.
9	D_{IN4+}	Noninverted Differential Input 4.
10	D_{IN4-}	Inverted Differential Input 4.
11	$\overline{REFRESH_1}$	Active-Low Enable for Side 1 Refresh Function. Short to GND_1 for normal operation with refresh enabled, or short to V_{DD1} for lower power, lower jitter, and quieter operation with refresh disabled.
12, 31	GND_1	Ground, Side 1.
13, 30	V_{DD1}	1.8 V Power Supply for Side 1. Connect both pins externally and bypass to the adjacent GND_1 pins with 0.1 µF capacitors.
14, 29	V_{DD2}	1.8 V Power Supply for Side 2. Connect both pins externally and bypass to the adjacent GND_2 pins with 0.1 µF capacitors.
15, 28	GND_2	Ground, Side 2.
16	$\overline{REFRESH_2}$	Active-Low Enable for Side 2 Refresh Function. Short to GND_2 for normal operation with refresh enabled, or short to V_{DD2} for lower power, lower jitter, and quieter operation with refresh disabled.
17	D_{OUT4-}	Inverted Differential Output 4.
18	D_{OUT4+}	Noninverted Differential Output 4.
19	D_{OUT3-}	Inverted Differential Output 3.
20	D_{OUT3+}	Noninverted Differential Output 3.
23	D_{OUT2-}	Inverted Differential Output 2.
24	D_{OUT2+}	Noninverted Differential Output 2.
25	D_{OUT1-}	Inverted Differential Output 1.
26	D_{OUT1+}	Noninverted Differential Output 1.
	EPAD	Exposed Pad. Connect the Side 1 EPAD to the same PCB ground as the GND_1 pins. Connect the Side 2 EPAD to the same PCB ground as the GND_2 pins.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD1} = V_{DD2} = 1.8 V, T_A = 25°C, $\overline{REFRESH_1}$ = GND_1, $\overline{REFRESH_2}$ = GND_2, R_L = 100 Ω, 1.25 GHz clock input with $|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V, and t_R and t_F < 0.05 ns, unless otherwise noted.

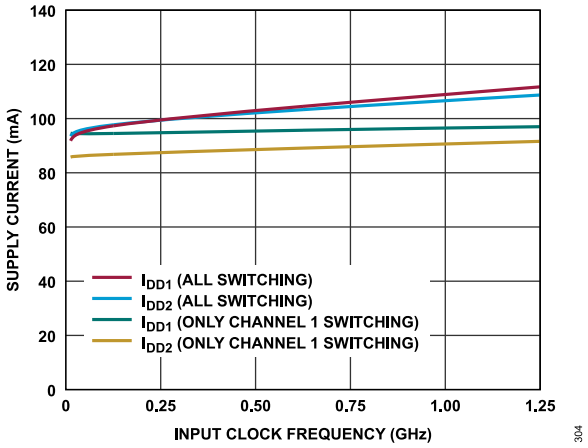

Figure 8. Supply Current vs. Input Clock Frequency for the ADN4622

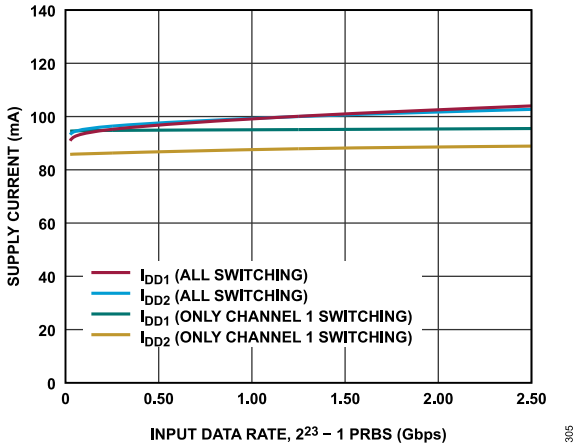

Figure 11. Supply Current vs. Input Data Rate, 2^{23} – 1 PRBS for the ADN4622

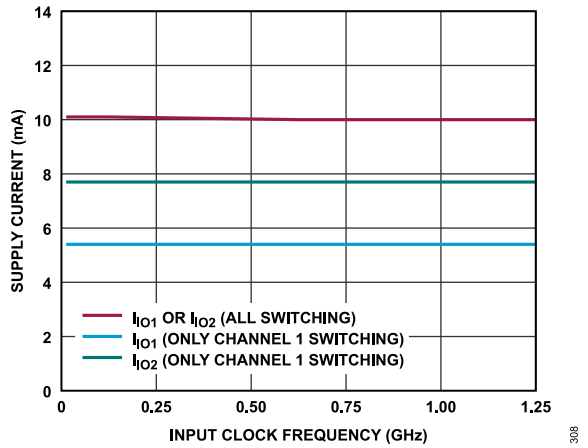

Figure 9. V_{IO1} and V_{IO2} Supply Current vs. Input Clock Frequency for the ADN4622

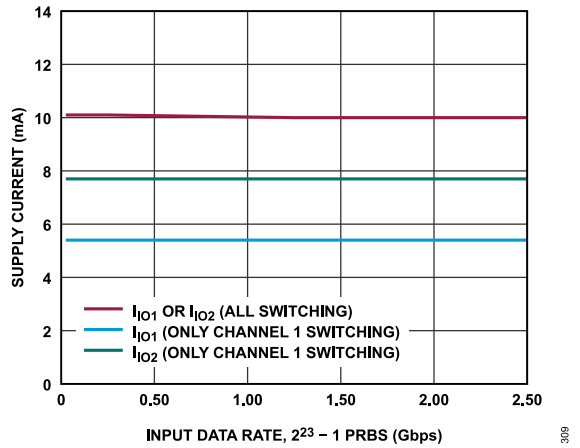

Figure 12. V_{IO1} and V_{IO2} Supply Current vs. Input Data Rate, 2^{23} – 1 PRBS for the ADN4622

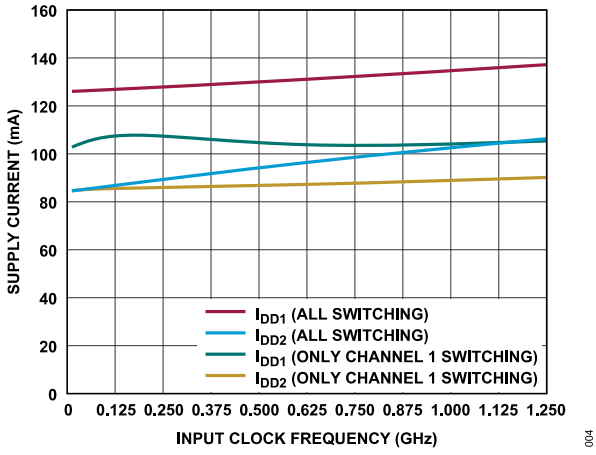

Figure 10. Supply Current vs. Input Clock Frequency for the ADN4624

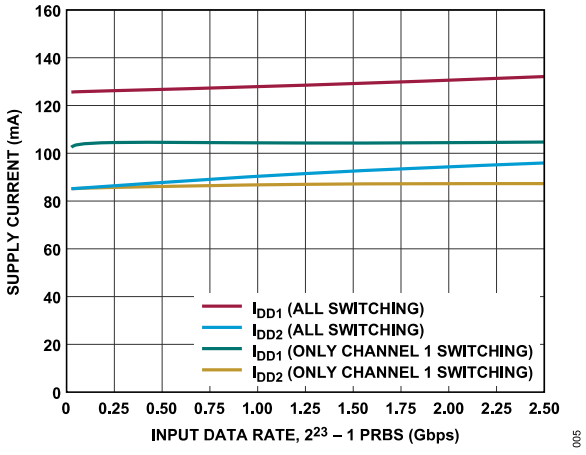

Figure 13. Supply Current vs. Input Data Rate, 2^{23} – 1 PRBS for the ADN4624

TYPICAL PERFORMANCE CHARACTERISTICS

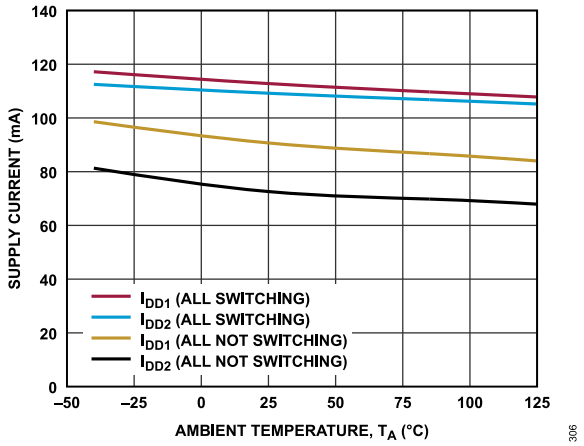

Figure 14. Supply Current vs. Ambient Temperature for the ADN4622

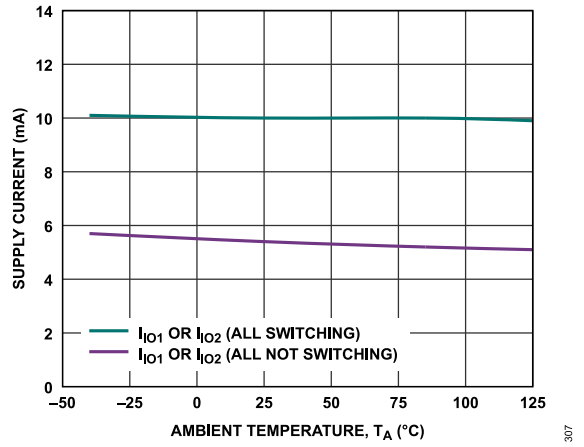

Figure 15. V_{IO1} and V_{IO2} Supply Current vs. Ambient Temperature for the ADN4622

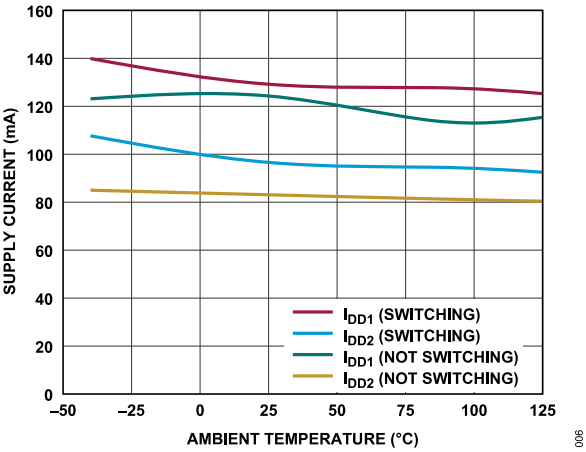

Figure 16. Supply Current vs. Ambient Temperature for the ADN4624

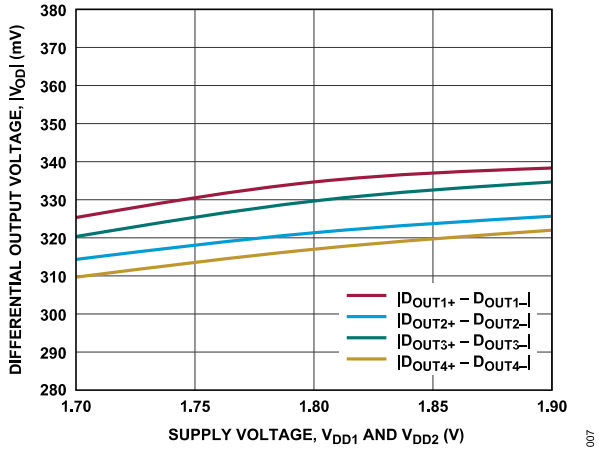

Figure 17. Differential Output Voltage, |V_{OD}| vs. Supply Voltage, V_{DD1} and V_{DD2}

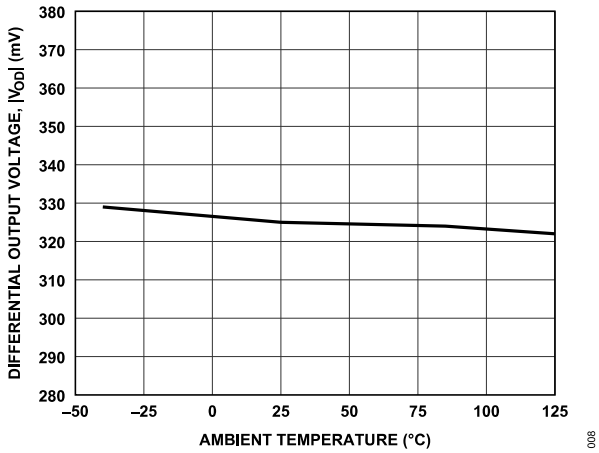

Figure 18. Differential Output Voltage, |V_{OD}| vs. Ambient Temperature

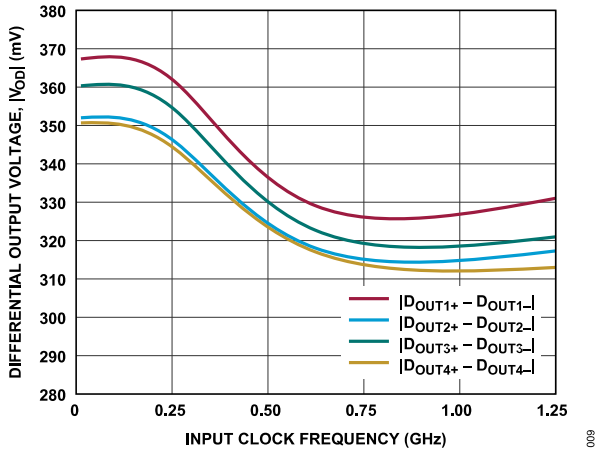

Figure 19. Differential Output Voltage, |V_{OD}| vs. Input Clock Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

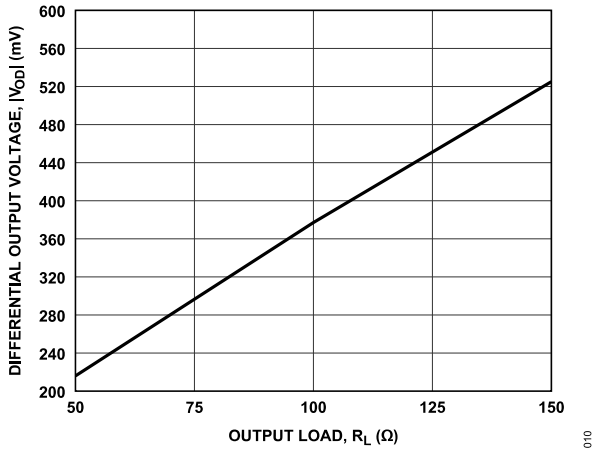

Figure 20. Differential Output Voltage, $|V_{OD}|$ vs. Output Load, R_L (DC Input)

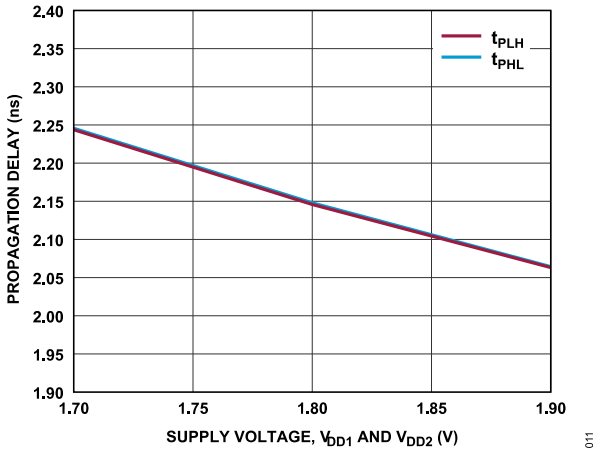

Figure 21. Propagation Delay vs. Supply Voltage, V_{DD1} and V_{DD2}

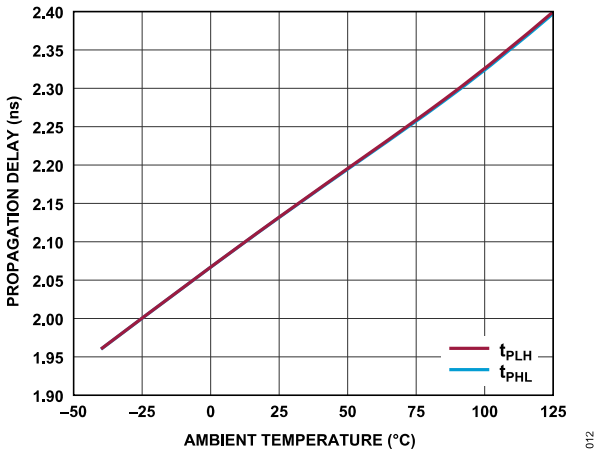

Figure 22. Propagation Delay vs. Ambient Temperature

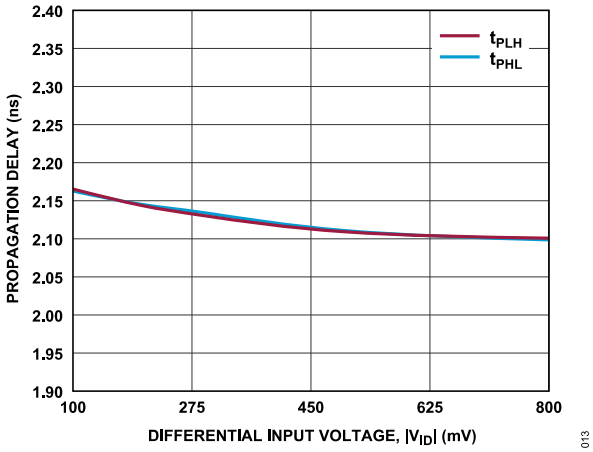

Figure 23. Propagation Delay vs. Differential Input Voltage, $|V_{ID}|$

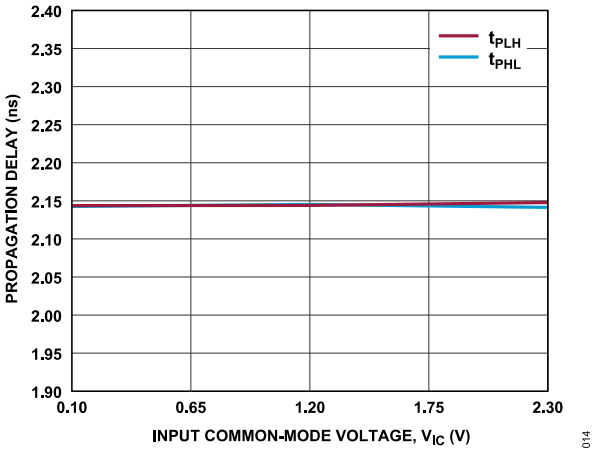

Figure 24. Propagation Delay vs. Input Common-Mode Voltage, V_{IC}

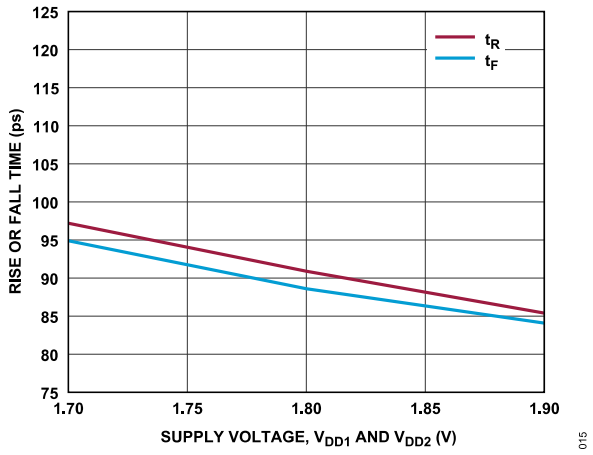

Figure 25. Rise or Fall Time vs. Supply Voltage, V_{DD1} and V_{DD2}

TYPICAL PERFORMANCE CHARACTERISTICS

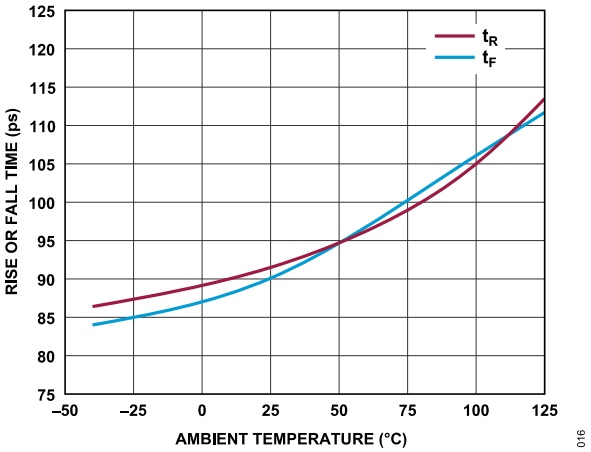

Figure 26. Rise or Fall Time vs. Ambient Temperature

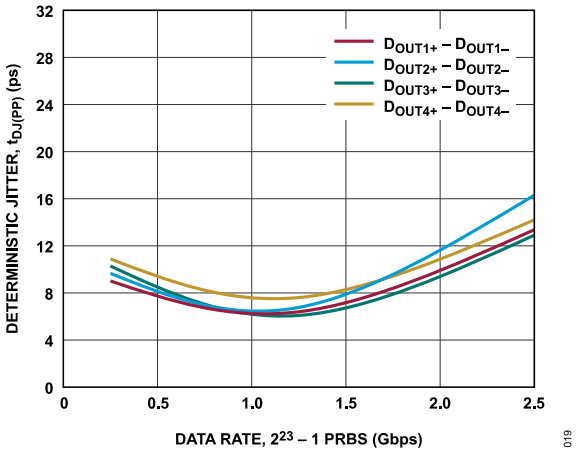

Figure 29. Deterministic Jitter, $t_{DJ(PP)}$ vs. Data Rate, 2^{23} – 1 PRBS

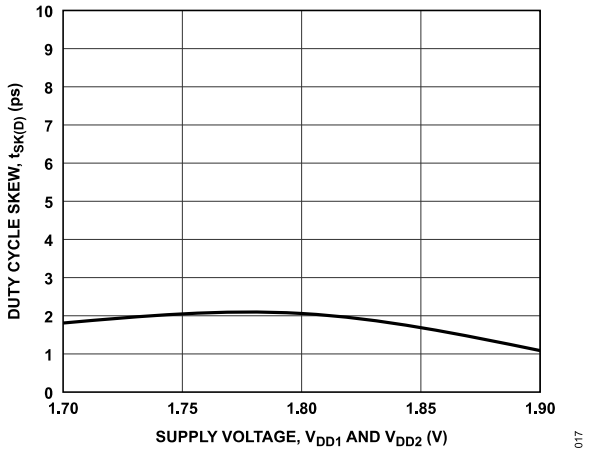

Figure 27. Duty Cycle Skew, $t_{SK(D)}$ vs. Supply Voltage, V_{DD1} and V_{DD2}

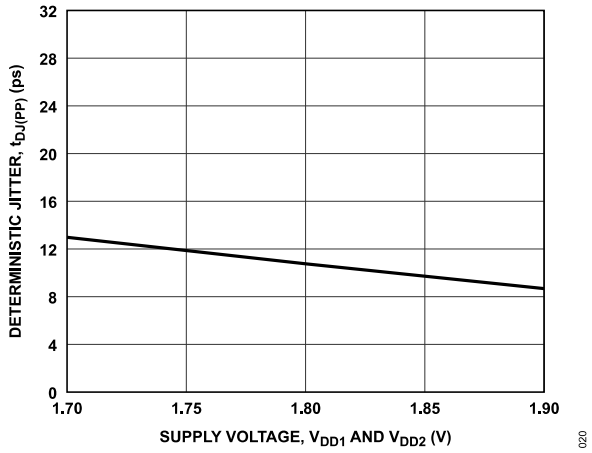

Figure 30. Deterministic Jitter, $t_{DJ(PP)}$ vs. Supply Voltage, V_{DD1} and V_{DD2}

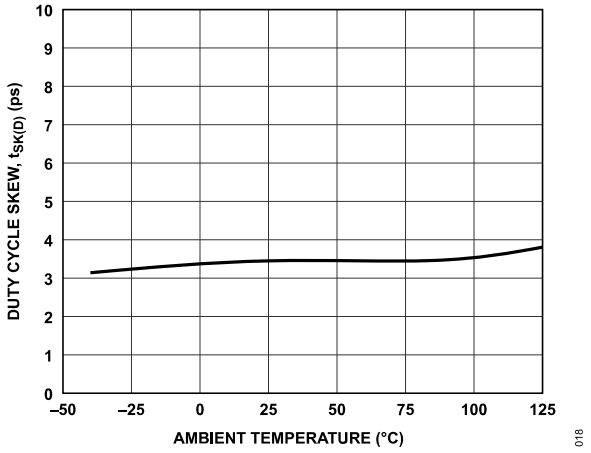

Figure 28. Duty Cycle Skew, $t_{SK(D)}$ vs. Ambient Temperature

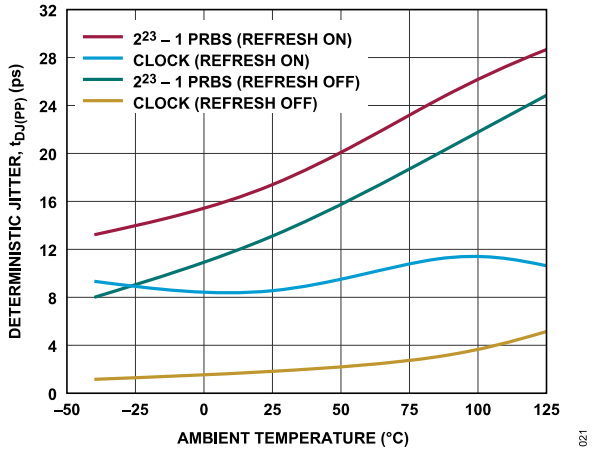

Figure 31. Deterministic Jitter, $t_{DJ(PP)}$ vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

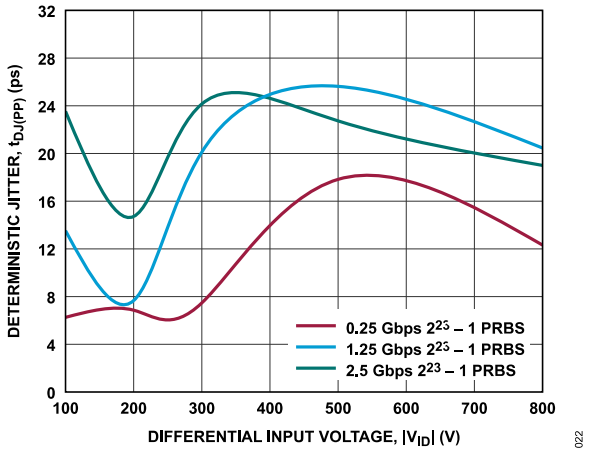

Figure 32. Deterministic Jitter, $t_{DJ(PP)}$ vs. Differential Input Voltage, $|V_{ID}|$

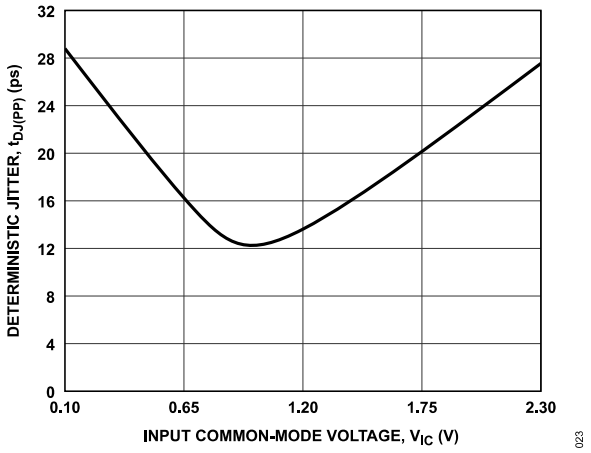

Figure 33. Deterministic Jitter, $t_{DJ(PP)}$ vs. Input Common-Mode Voltage, V_{IC}

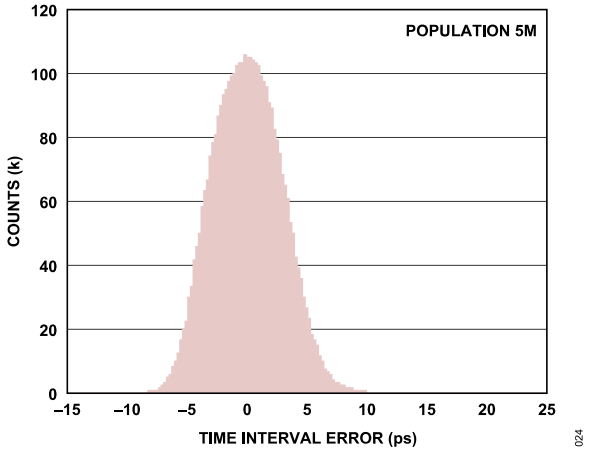

Figure 34. Time Interval Error (TIE) Histogram for $D_{OUT1\pm}$ at 1.25 GHz

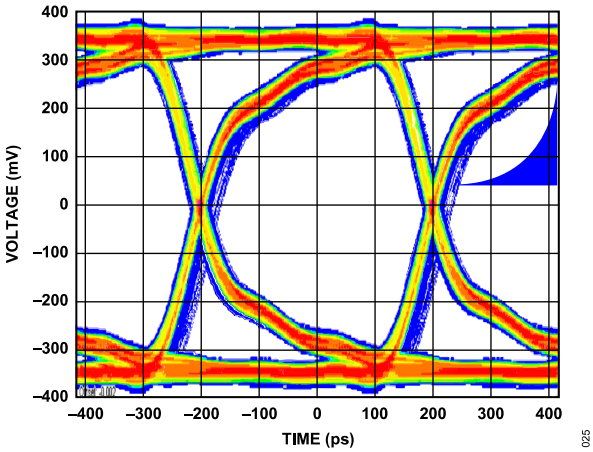

Figure 35. Eye Diagram for $D_{OUT1\pm}$ at 1.25 GHz

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

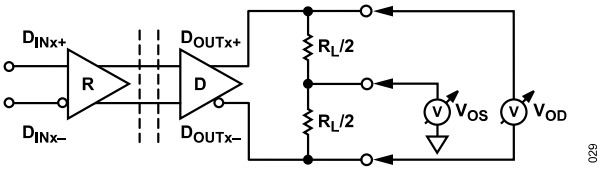

Figure 36. Driver Test Circuit

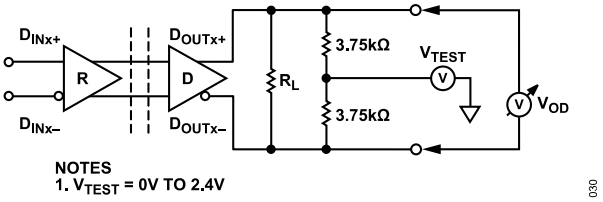

Figure 37. Driver Test Circuit (Full Load Across Common-Mode Range)

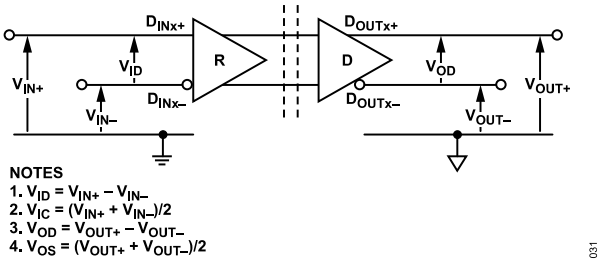

Figure 38. Voltage Definitions

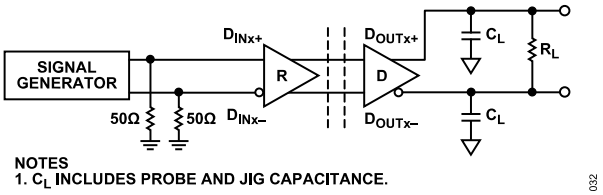

Figure 39. Timing Test Circuit

THEORY OF OPERATION

The ADN4622/ADN4624 are a high-speed differential signal isolators capable of switching up to 2.5 Gbps with signal levels compliant to TIA/EIA-644-A. The devices couple differential signals applied to the LVDS receiver inputs across the isolation barrier to the outputs on the other side and re-transmits the bit stream or clock as LVDS. This integration allows drop-in isolation of LVDS signal chains and isolation of other signals such as CML.

The LVDS receiver detects the differential voltage present across a termination resistor on an LVDS input. An integrated digital isolator transmits the input state across the isolation barrier, and an LVDS driver outputs the same state as the input.

When there is a positive differential voltage of ≥100 mV across a termination resistor between any D_{INx+} pin and a corresponding D_{INx-} pin, the corresponding D_{OUTx+} pin sources current. This current flows across the connected transmission line and termination at the receiver at the far end of the bus, while D_{OUTx-} sinks the return current. When there is a negative differential voltage of ≤−100 mV across any $D_{INx\pm}$ pin, the corresponding D_{OUTx+} pin sinks current with the D_{OUTx-} pin sourcing the current. Table 21 shows these input and output combinations.

The output drive current is between ±2.5 mA and ±4.5 mA (typically ±3.1 mA), developing between ±250 mV and ±450 mV across a 100 Ω termination resistor (R_T). The received voltage is centered around 1.2 V. Because the differential voltage (V_{ID}) reverses polarity, the peak-to-peak voltage swing across R_T is twice the differential voltage magnitude ($|V_{ID}|$).

ISOLATION AND REFRESH

In response to any change in the input state detected by the integrated LVDS receiver, an encoder circuit sends narrow (~1 ns) pulses to a decoder circuit using integrated transformer coils. The decoder is bistable and is, therefore, either set or reset by the pulses that indicate input transitions. The decoder state determines the LVDS driver output state in normal operation, which reflects the isolated LVDS buffer input state.

For normal operation of the ADN4622/ADN4624, the active-low enable pins, $\overline{REFRESH_1}$ and $\overline{REFRESH_2}$, are shorted to GND_1 and GND_2, respectively, to enable a refresh function. When enabled, this function means that in the absence of input transitions for more than approximately 1 µs, a periodic set of refresh pulses, indicative of the correct input state, ensures DC correctness at the output (including the fail-safe output state, if applicable).

On power-up, the output state can initially be in the incorrect DC state if there are no input transitions. The output state is corrected within 1 µs by the refresh pulses.

If the decoder receives no internal pulses for more than approximately 1 µs, the device assumes that the input side is unpowered or nonfunctional, in which case, the output is set to a positive differential voltage (logic high).

For clocks, constant bit streams, or protocols with error correction, the refresh functionality may not be required. If $\overline{REFRESH_1}$ and $\overline{REFRESH_2}$ are shorted to VDD1 and VDD2, respectively, the refresh functionality is disabled, allowing for lower power operation with no internal clock-like signals (potentially reducing conducted or radiated emissions). In this mode of operation, a new data transition at the input can be required to correct the output state, either after power-up or after a common-mode transient event beyond the guaranteed common-mode transient immunity specification.

TRUTH TABLE

The LVDS standard, TIA/EIA-644-A, defines normal receiver operation under two conditions: an input differential voltage of ≥+100 mV corresponding to one logic state, and a voltage of ≤−100 mV for the other logic state. Between these thresholds, the standard LVDS receiver operation is undefined (the LVDS receiver can detect either state), as shown in Table 21.

Table 21. Input and Output Operation

Input ($D_{INx\pm}$)			Output ($D_{OUTx\pm}$)		
Powered On	**V_{ID} (mV)**	**Logic**	**Powered On**	**V_{OD} (mV)**	**Logic**
Yes	≥100	High	Yes	≥250	High
Yes	≤−100	Low	Yes	≤−250	Low
Yes	$-100 < V_{ID} < +100$	Indeterminate	Yes	Indeterminate	Indeterminate
No	Don't care	Don't care	Yes	≥250	High

APPLICATIONS INFORMATION

PCB LAYOUT

The ADN4622/ADN4624 can operate with high-speed LVDS signals up to 1.25 GHz clock, or 2.5 Gbps nonreturn to zero (NRZ) data. When operating with such high frequencies, apply best practices for the LVDS trace layout and termination. Place a 100 Ω termination resistor as close as possible to the receiver, across the D_{INx+} and D_{INx-} pins.

Controlled impedance traces (100 Ω differential) are needed on LVDS signal lines for full signal integrity, reduced system jitter, and for minimizing electromagnetic interference (EMI) from the PCB. Trace widths, lateral distance within each pair, and distance to the ground plane underneath all must be chosen appropriately. Via fencing to the PCB ground between pairs is also a best practice to minimize crosstalk between adjacent pairs.

The ADN4624 has passed EN 55032 Class B emissions limits without extra considerations required for the isolator when operating with up to 2 Gbps PRBS data. When isolating at higher data rates or for high-speed clocks, specific PCB layout measures can be required to reduce dipole antenna effects from the isolation gap and provide sufficient margin below Class B emissions limits. The ADN4622 has passed EN 55032 Class B emissions limits when operating with up to 900 Mbps PRBS data, using a high-speed PCB design with an embedded PCB stitching capacitor (constructed by overlapping internal PCB Layer 2 and Layer 3 under the area of the isolator).

The best practice for high-speed PCB design avoids emissions from traces with high-speed LVDS signals. Special care is recommended for off board connections, where switching transients from high-speed LVDS signals (and clocks in particular) can conduct onto cabling, resulting in radiated emissions. Use common-mode chokes, ferrites, or other filters as appropriate at LVDS connectors and power supplies, as well as cable shield or PCB ground connections to earth or chassis.

The ADN4622/ADN4624 require appropriate decoupling of the V_{DDx} pins with 100 nF capacitors. Power supplies must also have appropriate filtering to avoid possible radiated emissions due to high-frequency switching noise.

APPLICATION EXAMPLES

High-speed LVDS interfaces for the analog front end (AFE), processor to processor serial communication, or video and imaging data can be isolated using the ADN4622/ADN4624 between components, between boards, or at a cable interface.

The ADN4622/ADN4624 provides the galvanic isolation required for robust external ports, and the low jitter and high drive strength of the device allow communication along short cable runs of a few meters. High common-mode immunity ensures communication integrity even in harsh, noisy environments, and isolation can protect against electromagnetic compatibility (EMC) transients up to ±8 kV_{PEAK}, such as ESD, electrical fast transient (EFT), and surge.

Standard LVDS inputs and outputs allow simple integration into high-speed signal chains using field-programmable gate arrays (FPGAs), redrivers, or coupling networks to interface to CML and other physical layers.

Isolated AFE applications provide an example of the ADN4622/ADN4624 isolating an LVDS interface between components. The ADN4624 can isolate four channels simultaneously, which suits the isolation of high-bandwidth measurement data from analog-to-digital converters (ADCs) with parallel LVDS outputs, and the ADN4622 can isolate two LVDS channels in each direction, which suits the isolation of the ADCs relying on echoed clocks. Both can alternatively be used with serialization and deserialization (SERDES) applications using FPGAs to aggregate large arrays of CMOS inputs or outputs through the 2.5 Gbps isolation channels. The ADN4622/ADN4624 additive phase jitter is sufficiently low that it does not affect the ADC performance even when isolating the sample clock. In addition, implementing the galvanic isolation improves ADC performance by removing digital and power-supply noise from the FPGA and application-specific IC (ASIC) circuit.

PCB to PCB connections and even cable interfaces can leverage LVDS signaling for high bandwidth links with low-latency synchronous data transfer. Serialized Gigabit Ethernet connections can be isolated to robustly cascade Ethernet or multiprotocol switches for industrial controller communication modules. The ADN4622 with two LVDS channels in each direction can isolate the 1.25 Gbps transmit and receive signals for two ports at each Gigabit Ethernet switch. The propagation delay of just over a couple of nanoseconds provides the low latency needed for industrial automation and process control.

The ADN4624 can isolate a range of video and imaging protocols, including protocols that use CML rather than LVDS for the physical layer. One example is High-Definition Multimedia Interface (HDMI), where AC coupling and biasing and termination resistor networks are used, as shown in Figure 40 to convert between CML (used by the transition minimized differential signaling (TMDS) data and clock lanes) and the LVDS levels required by the ADN4624. Additional Analog Devices isolator components, such as the ADuM2250 and ADuM2251 I^2C isolators, can be used to isolate control signals and power (ADuM6421A and ADuM6028 *iso*Power integrated, isolated DC-DC converter). This circuit supports resolutions up to 1080p.

Other coupling networks, processing nodes, and translation circuits can use the ADN4624 as part of an overall signal chain to isolate MIPI CSI-2, DisplayPort, and LVDS-based protocols such as FPD-Link. Use of an FPGA or an application-specific integrated circuit (ASIC) serializer/deserializer (SERDES) expands bandwidth through multiple ADN4624 devices to support 1080p or 4K video resolutions, providing an alternative to short reach fiber links.

APPLICATIONS INFORMATION

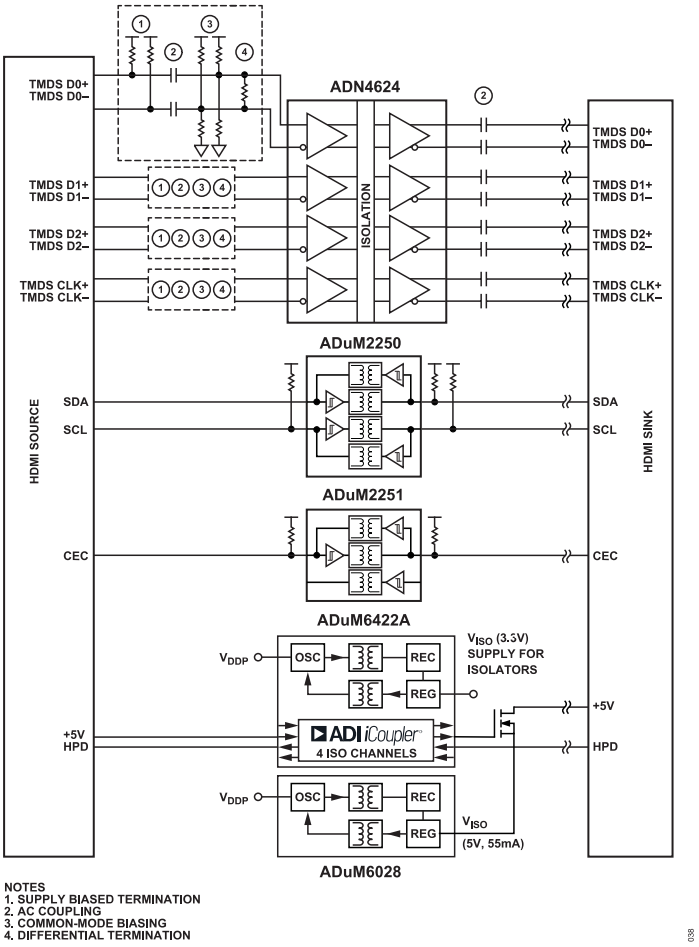

Figure 40. Example Isolated Video Interface (HDMI) Using the ADN4624

MAGNETIC FIELD IMMUNITY

The limitation on the magnetic field immunity of the device is set by the condition in which the induced voltage in the transformer receiving coil is sufficiently large, either to falsely set or reset the decoder. The following analysis defines such conditions. The ADN4622/ADN4624 is examined in a 1.7 V operating condition because this operating condition represents the most susceptible mode of operation for these products.

The pulses at the transformer output have an amplitude greater than 0.35 V. The decoder has a sensing threshold of about 0.11 V, therefore establishing a 0.24 V margin in which induced voltages are tolerated.

The voltage (V) induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N \quad (1)$$

where:

$d\beta$ is the change in magnetic flux density.

dt is the change in time.

r_n is the radius of the n^{th} turn in the receiving coil.

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADN4622/ADN4624 and an imposed requirement that the induced voltage be, at most, 50% of the 0.11 V threshold at the decoder, a maximum allowable external magnetic flux density is calculated as shown in Figure 41.

APPLICATIONS INFORMATION

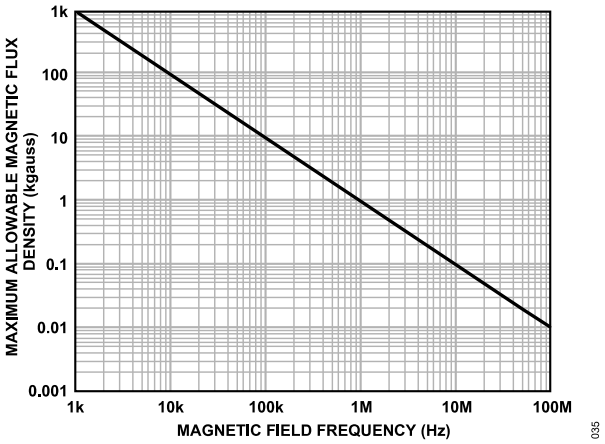

Figure 41. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 1.06 kgauss induces a voltage of 0.055 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs with the worst case polarity during a transmitted pulse, the applied magnetic field reduces the received pulse from >0.35 V to 0.295 V. This voltage is still higher than the 0.11 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADN4622/ADN4624 transformers. Figure 42 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADN4622/ADN4624 is insensitive to external fields. Only extremely large, high frequency currents that are close to the component can potentially be a concern. For the 1 MHz example noted, a 2.64 kA current must be placed 5 mm from the ADN4622/ADN4624 to affect component operation.

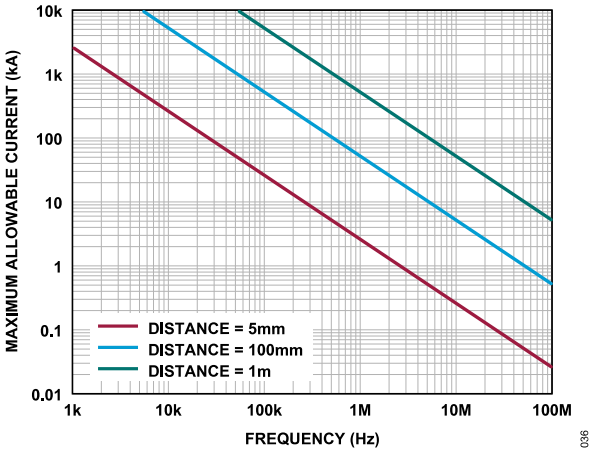

Figure 42. Maximum Allowable Current for Various Current to ADN4622/ ADN4624 Spacings

In combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Avoid PCB structures that form loops.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, which allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total RMS voltage across the isolation barrier, pollution degree, and material group. The material group and creepage for ADN4622/ADN4624 are detailed in Table 4 and Table 5.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the thickness of the insulation, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as DC stress, which causes little wear out because there is no displacement current, and an AC component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this type of waveform reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz AC and DC across the isolation barrier, as shown in Equation 1. Because only the AC portion of the stress

APPLICATIONS INFORMATION

causes wear out, the equation can be rearranged to solve for the AC RMS voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in this product, the AC RMS voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \quad (2)$$

where:

V_{RMS} is the total RMS working voltage.

$V_{AC\ RMS}$ is the time varying portion of the working voltage.

V_{DC} is the DC offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V AC RMS and a 400 V DC bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 43 and the following equations.

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}^2 + V_{DC}^2} \quad (2)$$

$$V_{RMS} = \sqrt{240^2 + 400^2} \quad (3)$$

V_{RMS} = 466 V

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the AC RMS voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}^2 - V_{DC}^2} \quad (4)$$

$$V_{AC\ RMS} = \sqrt{466^2 - 400^2} \quad (5)$$

$V_{AC\ RMS}$ = 240 V RMS

In this case, the AC RMS voltage is simply the line voltage of 240 V RMS. This calculation is more relevant when the waveform is not sinusoidal. Table 13 and Table 14 compare the value to the limits for the working voltage for the expected lifetime. Note that the DC working voltage limit in Table 13 and in Table 14 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

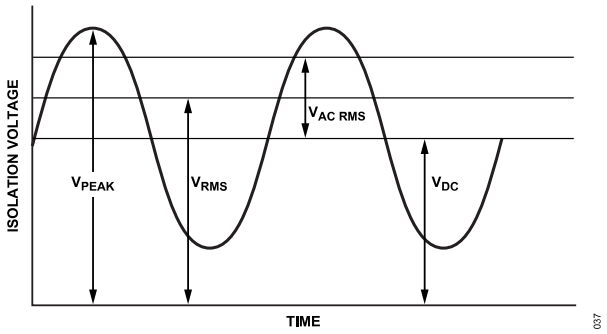

Figure 43. Critical Voltage Example

OUTLINE DIMENSIONS

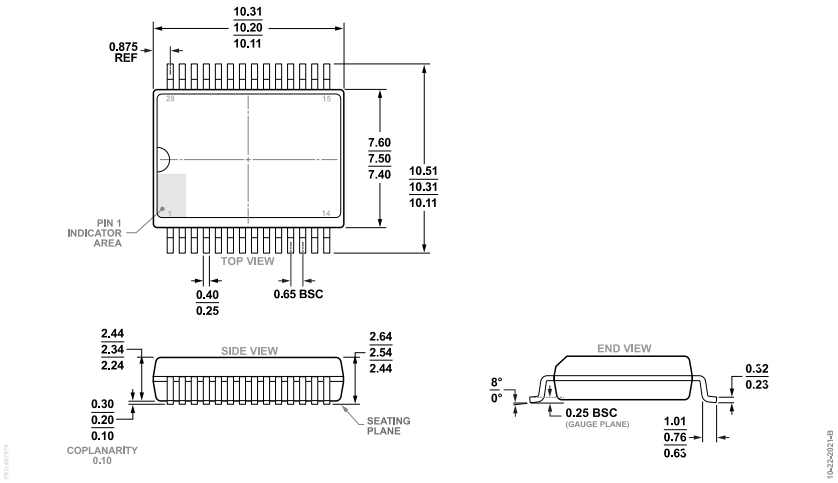

Figure 44. 28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP] (RN-28-1)
Dimensions shown in millimeters

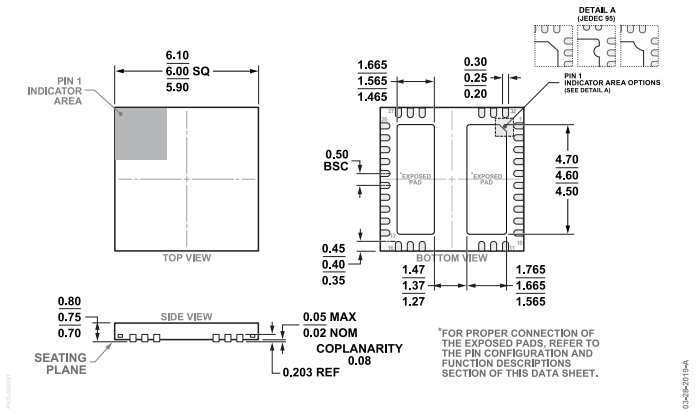

Figure 45. 32-Lead Lead Frame Chip Scale Package [LFCSP] 6 mm × 6 mm Body and 0.75 mm Package Height (CP-32-32)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADN4622BRNZ	−40°C to +125°C	28-Lead SOIC (Wide, Finer Pitch)	Tube, 46	RN-28-1
ADN4622BRNZ-RL	−40°C to +125°C	28-Lead SOIC (Wide, Finer Pitch)	Reel, 1000	RN-28-1
ADN4624BRNZ	−40°C to +125°C	28-Lead SOIC (Wide, Finer Pitch)	Tube, 46	RN-28-1
ADN4624BRNZ-RL	−40°C to +125°C	28-Lead SOIC (Wide, Finer Pitch)	Reel, 1000	RN-28-1
ADN4624BCPZ	−40°C to +125°C	32-Lead LFCSP (6 mm x 6 mm)	Tray, 490	CP-32-32
ADN4624BCPZ-RL	−40°C to +125°C	32-Lead LFCSP (6 mm x 6 mm)	Reel, 2500	CP-32-32

[1] Z = RoHS Compliant Part.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Model[1]	Description
EVAL-ADN4622EB1Z	ADN4622 SOIC_W_FP Evaluation Board
EVAL-ADN4624EB1Z	ADN4624 SOIC_W_FP Evaluation Board

[1] Z = RoHS Compliant Part.