35A Synchronous Step Down COT Controller

May 2018 Rev. 2.0.2

GENERAL DESCRIPTION

The XRP6141 is a synchronous step-down controller for point-of load supplies up to 35A. A wide 4.5V to 22V input voltage range allows for single supply operation from industry standard 5V, 12V and 19.6V rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XRP6141 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation hence simplifying circuit implementation and reducing overall component count. The control loop also provides exceptional line regulation and maintains constant operating frequency. A selectable power saving mode, allows the user to operate in discontinuous mode (DCM) at light current loads thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XRP6141 is available in RoHS compliant, green/halogen free space-saving 16-pin 3x3 QFN package.

APPLICATIONS

- **Networking and Communications**
- **Fast Transient Point-of-Loads**
- **Industrial and Medical Equipment**
- **Embedded High Power FPGA**

FEATURES

- **35A Capable Step Down Controller**
  - Wide Input Voltage Range
    - 5V to 22V Single Supply
    - 4.5V to 5.5V Low V_{IN}
  - Integrated high Current 2A/3A Drivers
  - 0.6V to 18V Adjustable Output Voltage
- **Proprietary Constant On-Time Control**
  - No Loop Compensation Required
  - Ceramic Output Cap. Stable operation
  - Programmable 200ns-2µs
  - Constant 200kHz-800kHz Frequency
  - Selectable CCM or CCM/DCM Operation
- **Programmable hiccup current limit with thermal compensation**
- **Precision Enable and Power-Good Flag**
- **Programmable Soft-start**
- **Integrated Bootstrap diode**
- **16-pin QFN Package**

TYPICAL APPLICATION DIAGRAM

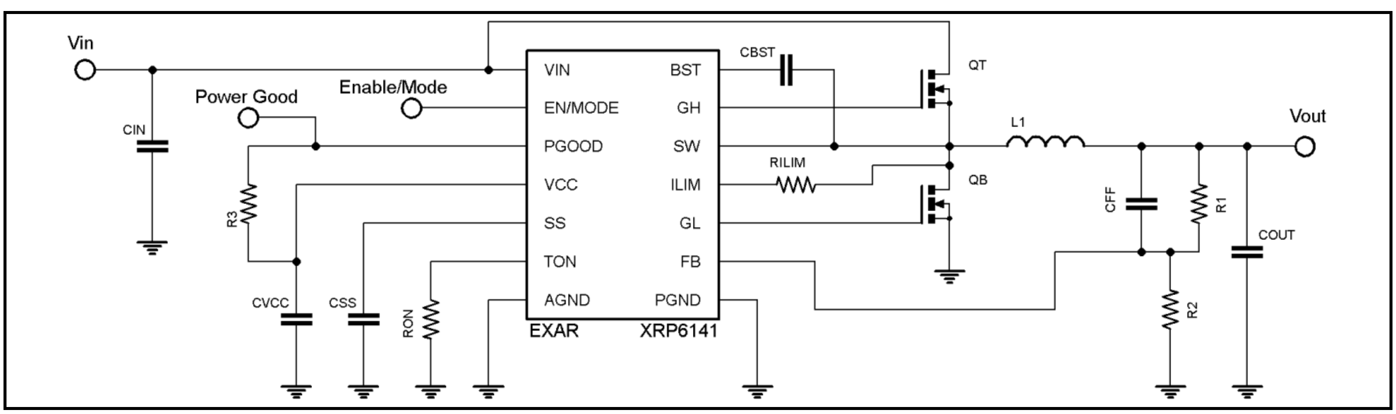


Fig. 1: XRP6141 Application Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{IN} .... -0.3V to 28V
V_{CC} .... -0.3V to 6.0V
BST .... -0.3V to 34V[2]
BST-SW .... -0.3V to 6V
SW, ILIM .... -5V to 28V[1,2]
GH .... -0.3V to BST+0.3V
GH-SW .... -0.3V to 6V
ALL other pins .... -0.3V to VCC+0.3V
Storage Temperature .... -65°C to 150°C
Junction Temperature .... 150°C
Power Dissipation .... Internally Limited
Lead Temperature (Soldering, 10 sec) .... 300°C
ESD Rating (HBM - Human Body Model) 2kV

OPERATING RATINGS

V_{IN} .... -0.3V to 22V
V_{CC} .... -0.3V to 5.5V
SW, ILIM .... -1V to 26V[1]
PGOOD, VCC, TON, SS, EN, GL, FB .... -0.3V to 5.5V
Switching Frequency .... 200kHz-800kHz[3]
Junction Temperature Range .... -40°C to 125°C

Note 1: SW pin's minimum DC range is -1V, transient is -5V for less than 50ns
Note 2: No external voltage applied
Note 3: Recommended

ELECTRICAL SPECIFICATIONS

Specifications are for Operating Junction Temperature of T_J = 25°C only; limits applying over the full Operating Junction Temperature range are denoted by a "•". Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 12V, BST=VCC, SW=GND=PGND=0V, CGH=CGL=3.3nF.

Parameter	Min.	Typ.	Max.	Units		Conditions
Power Supply Characteristics						
V_{IN}, Input Voltage Range	5	12	22	V	•	VCC regulating
	4.5	5.0	5.5			VCC tied to V_{IN}
I_{VIN}, V_{IN} supply current		0.7	2	mA	•	Not switching, V_{IN} = 12V, VFB = 0.7V
I_{VCC}, VCC Quiescent current		0.7	2	mA	•	Not switching, V_{CC} = V_{IN} = 5V, VFB = 0.7V
I_{VIN}, V_{IN} supply current		11		mA		F = 300kHz, RON = 108.8k, VFB = 0.58V
I_{OFF}, Shutdown current		0.1		µA		Enable = 0V, V_{IN} = 12V
Enable and Under-Voltage Lock-Out UVLO						
V_{IH_EN}, EN Pin Rising Threshold	1.8	1.9	2.0	V	•	
V_{EN_HYS}, EN Pin Hysteresis		50		mV		
V_{IH_EN}, EN Pin Rising Threshold for DCM/CCM operation	2.9	3.0	3.1	V	•	
V_{EN_HYS}, EN Pin Hysteresis		100		mV		
VCC UVLO start threshold, rising edge	4.00	4.25	4.50	V	•	
VCC UVLO Hysteresis		200		mV		
Reference voltage						
V_{REF}, Reference voltage	0.597	0.600	0.603	V		V_{IN} = 5V-22V → VCC regulating
	0.596		0.604	V		V_{IN} = 4.5V-5.5V → tie VCC to V_{IN}
	0.594	0.600	0.606	V	•	V_{IN} = 5V-22V → VCC regulating, V_{IN} = 4.5V-5.5V → tie VCC to V_{IN}
DC Line regulation		±0.1		%		CCM operation, closed loop, applies to any C_{OUT}
DC Load regulation		±0.25		%		CCM operation, closed loop, applies to any C_{OUT}

Parameter	Min.	Typ.	Max.	Units		Conditions
Programmable Constant On-Time						
On-Time 1	1855	2182	2509	ns	•	RON = 141.2kΩ, V_{IN} = 22V
f corresponding to On-Time 1	217	250	294	kHz		V_{IN} = 22V, V_{OUT} = 12V
Minimum Programmable On-Time		109		ns		RON = 7.059kΩ, V_{IN} = 22V
On-Time 2	170	200	230	ns	•	RON = 7.059kΩ, V_{IN} = 12V
f corresponding to On-Time 2	1618	1375	1196	kHz		V_{OUT} = 3.3V
f corresponding to On-Time 2	490	417	362	kHz		V_{OUT} = 1.0V
On-Time 3	391	460	529	ns	•	RON = 16.235kΩ, V_{IN} = 12V
Minimum Off-Time		250	350	ns	•	
Diode Emulation Mode						
Zero crossing threshold	-4	-1		mV		DC value measured during test
SoftStart						
SS Charge current	-14	-10	-6	µA	•	
SS Discharge current	1			mA	•	Fault present
VCC Linear Regulator (VCC should be tied to V_{IN}, for 4.5V≤V_{IN}≤5.5V)						
VCC Output Voltage	4.8	5.0	5.2	V	•	V_{IN} = 6V to 22V, Iload = 0 to 30mA
	4.51	4.7			•	V_{IN} = 5V, Iload = 0 to 20mA
Dropout Voltage		200	490	mV	•	I_{VCC} = 30mA
Power Good Output						
Power Good Threshold	-10	-7.5	-5	%		
Power Good Hysteresis		2	4	%		
Power Good Sink Current	1			mA		
Protection: OCP, OTP, Short-circuit						
Hiccup timeout		110		ms		
ILIM pin source current	45	50	55	µA		
ILIM current temperature coeff.		0.4		%/°C		
OCP comparator offset	-8	0	+8	mV	•	
Current limit blanking		100		ns		GL rising > 1V
Thermal shutdown threshold[1]		150		°C		Rising temperature
Thermal Hysteresis[1]		15		°C		
VSCTH Feedback pin short-circuit threshold	50	60	70	%	•	Percent of VREF, short circuit is active After PGOOD is up
Output Gate drivers						
GH Pull-Down Resistance		1.35	2.0	Ω		IGH = 200mA
GH Pull-up Resistance		1.8	2.8	Ω		IGH = 200mA
GL Pull-Down Resistance		1.35	1.9	Ω		IGL = 200mA
GL Pull-up Resistance		1.7	2.7	Ω		IGL = 200mA
GH and GL pull-down Resistance		50	---	kΩ		
GH and GL rise time		35	50	ns		10% to 90%
GH and GL fall time		30	40	ns		90% to 10%
GL to GH non-overlap time	20	30	60	ns		Measured GL falling edge = 1V to GH rising edge = 1V, BST = VCC, SW = 0V
GH to GL non-overlap time	15	20	40	ns		Measured GH falling edge = 1V to GL rising edge = 1V

Note 1: Guaranteed by design

BLOCK DIAGRAM

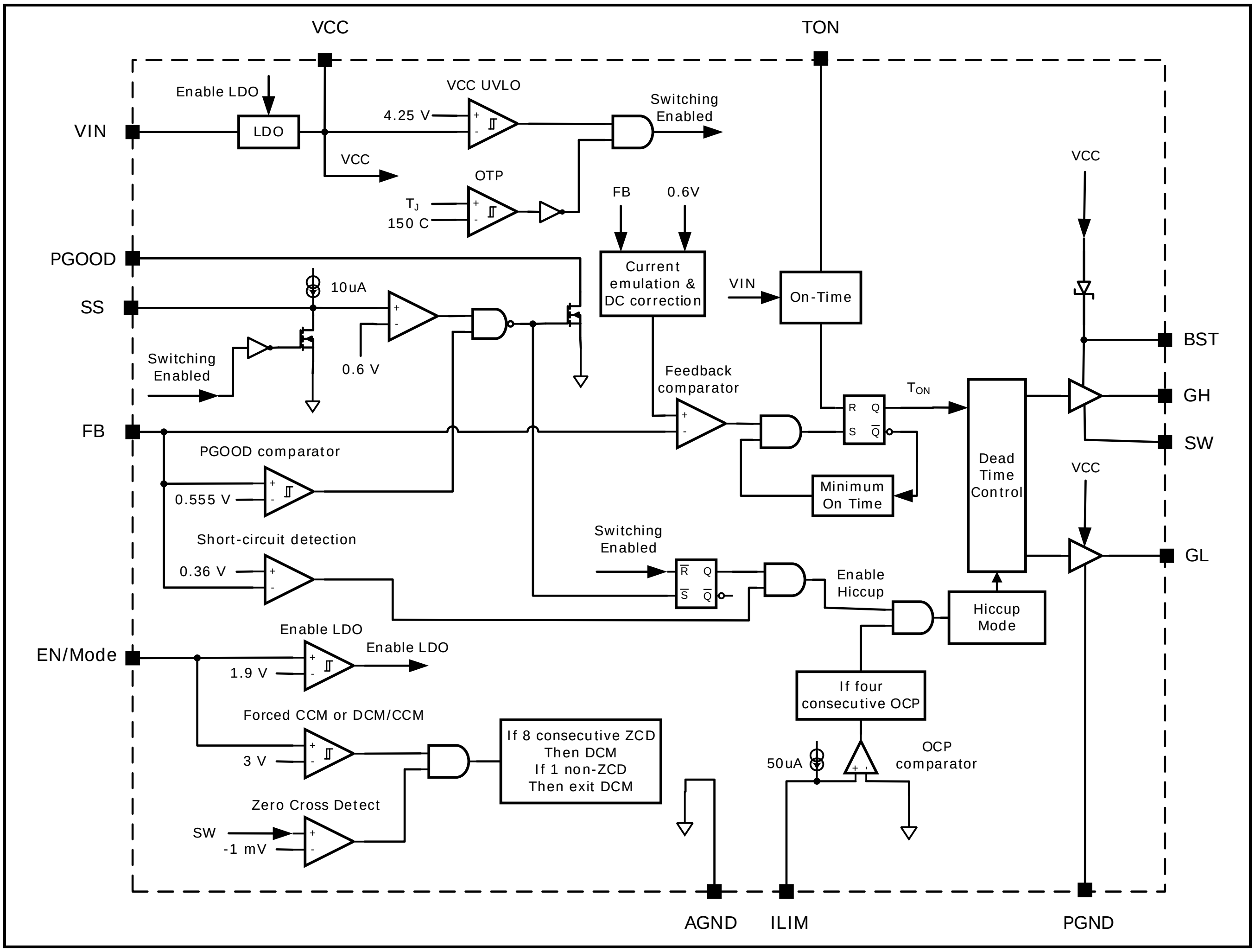


Fig. 2: XRP6141 Block Diagram

PIN ASSIGNMENT

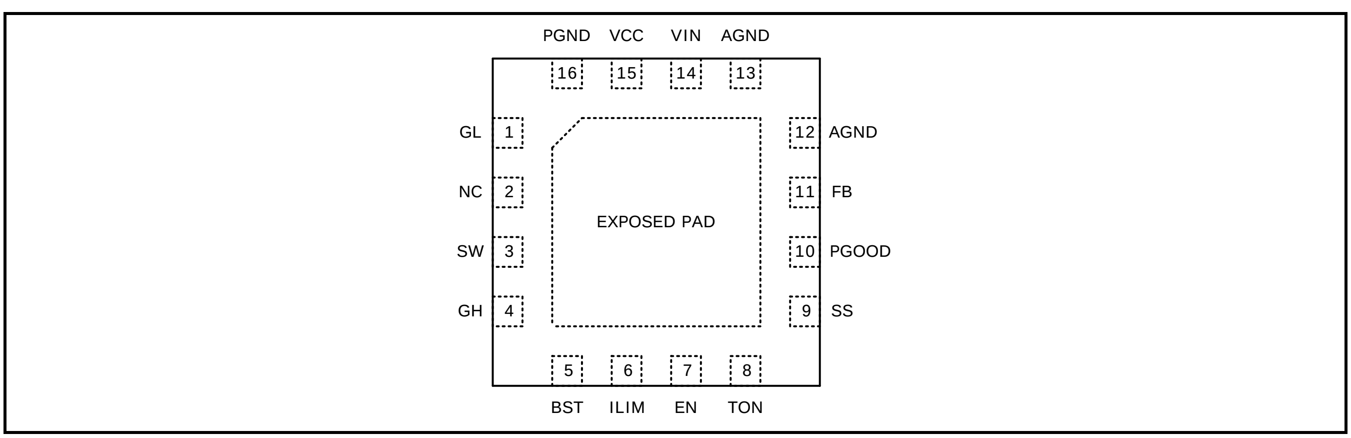


Fig. 3: XRP6141 Pin Assignment

PIN DESCRIPTION

Name	Pin Number	Description
GL	1	Driver output for Low-side N-channel synchronous MOSFET.
NC	2	Internally not connected. Leave this pin floating.
SW	3	Lower supply rail for high-side gate driver GH. Connect this pin to the junction between the two external N-channel MOSFETs.
GH	4	Driver output for high-side N-channel switching MOSFET.
BST	5	High-side driver supply pin. Connect a 0.1uF bootstrap capacitor between BST and SW.
ILIM	6	Over-current protection programming. Connect with a resistor to the Drain of the low-side MOSFET.
EN/MODE	7	Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V then the IC will operate in DCM or CCM depending on load.
TON	8	Constant on-time programming pin. Connect with a resistor to AGND.
SS	9	Soft-Start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10uA internal source current.
PGOOD	10	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
FB	11	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and GND in order to program V_{OUT}.
AGND	12, 13	Analog ground. Control circuitry of the IC is referenced to this pin.
VIN	14	IC supply input. Provides power to internal LDO.
VCC	15	The output of LDO. For operation using a 5V rail, VCC should be shorted to VIN.
PGND	16	Low side driver ground
Exposed Pad		Thermal pad for heat dissipation. Connect to AGND with a short trace.

ORDERING INFORMATION(1)

Part Number	Operating Temperature Range	Lead-Free	Package	Packing Method
XRP6141EL-F	$-40°C \le T_J \le +125°C$	Yes(2)	3x3mm QFN16	Tray
XRP6141ELTR-F				Tape & Reel
XRP6141EVB	XRP6141 Evaluation Board			

NOTES:

1. Refer to www.exar.com/XRP6141 for most up-to-date Ordering Information
2. Visit www.exar.com for additional information on Environmental Rating.

TYPICAL PERFORMANCE CHARACTERISTICS

All data taken at V_{IN} = 12V, V_{OUT}=1.2V, f=300kHz, T_A = 25°C, unless otherwise specified - Schematic and BOM from Application Information section of this datasheet.

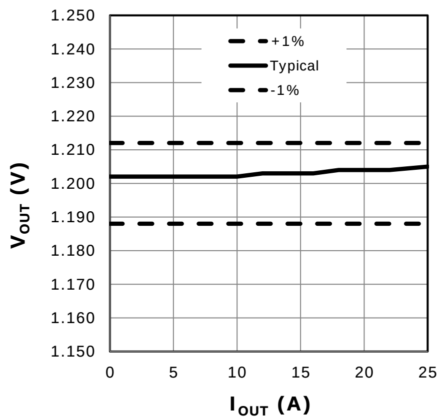


Fig. 4: Load regulation, V_{IN} = 12V

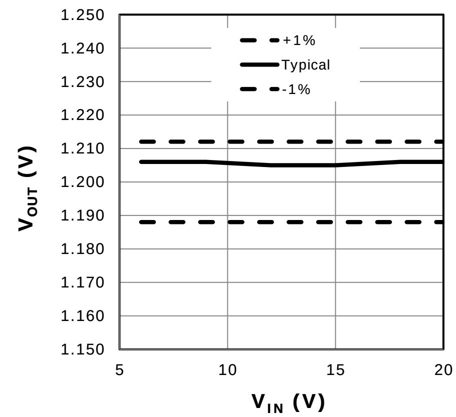


Fig. 5: Line regulation, I_{OUT} = 25A

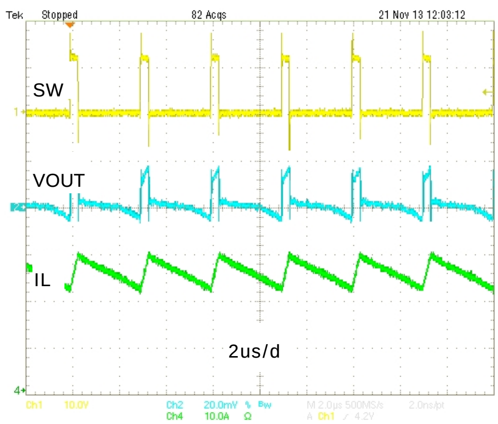


Fig. 6: V_{OUT} ripple is 22mV at 25A, $12V_{IN}$, $1.2V_{OUT}$

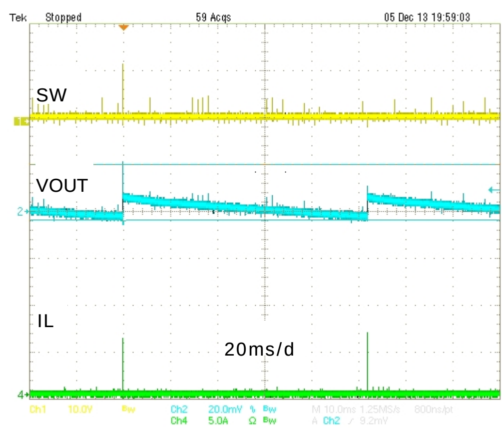


Fig. 7: V_{OUT} ripple is 22mV at 0A, DCM, $12V_{IN}$, $1.2V_{OUT}$

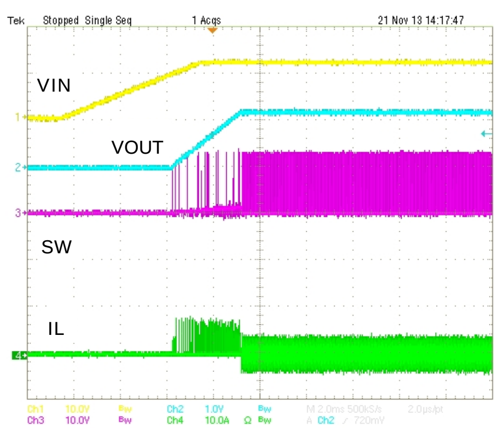


Fig. 8: Powerup, Forced CCM, I_{OUT} = 0A

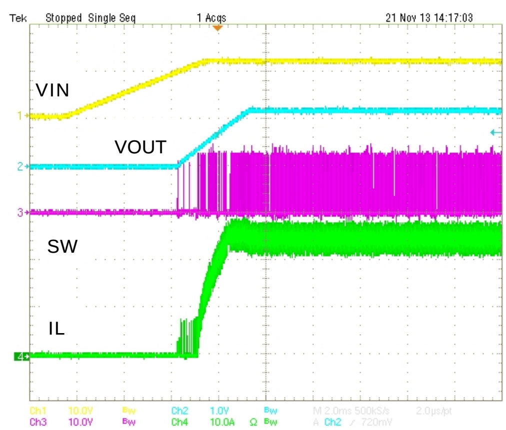


Fig. 9: Powerup, Forced CCM, I_{OUT} = 25A

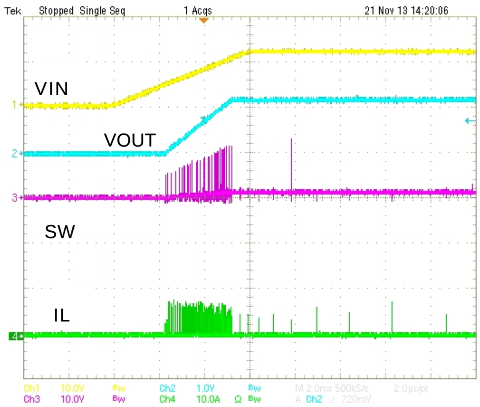


Fig. 10: Powerup, DCM/CCM, I_{OUT} = 0A

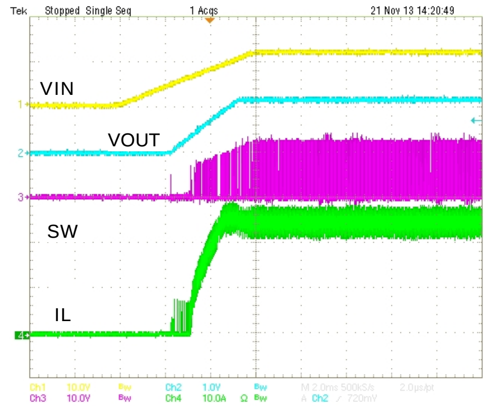


Fig. 11: Powerup, DCM/CCM, I_{OUT} = 25A

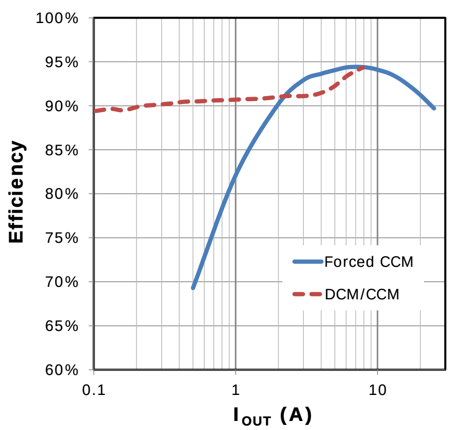


Fig. 12: Efficiency, $5V_{IN}$, $1.8V_{OUT}$, 0.47uH, 300kHz

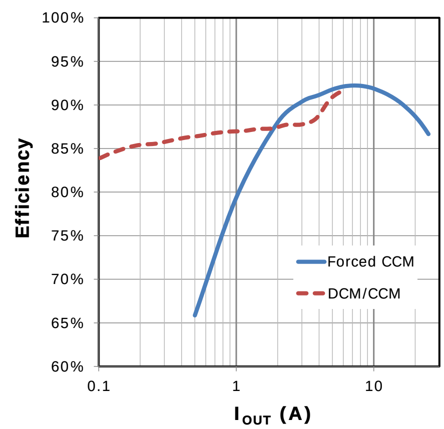


Fig. 13: Efficiency, $5V_{IN}$, $1.2V_{OUT}$, 0.47uH, 300kHz

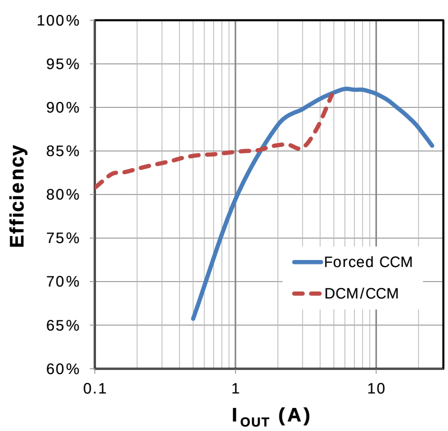


Fig. 14: Efficiency, $5V_{IN}$, $1.0V_{OUT}$, 0.47uH, 300kHz

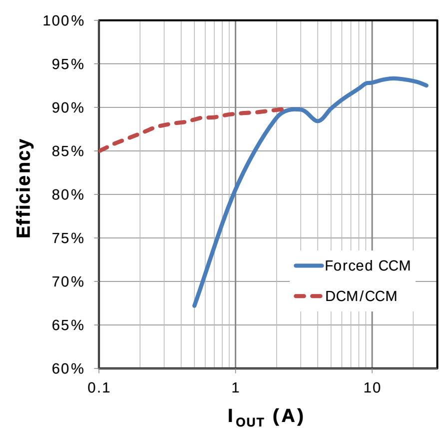


Fig. 15: Efficiency, $12V_{IN}$, $3.3V_{OUT}$, 1uH, 300kHz

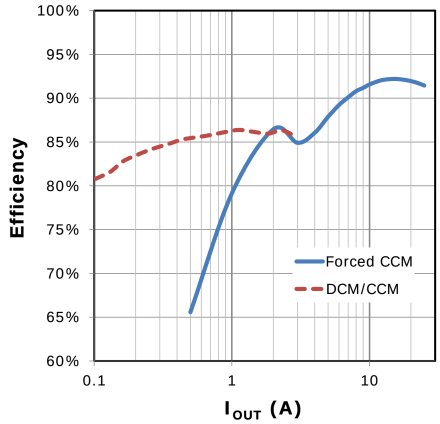


Fig. 16: Efficiency, $12V_{IN}$, $2.5V_{OUT}$, 1uH, 300kHz

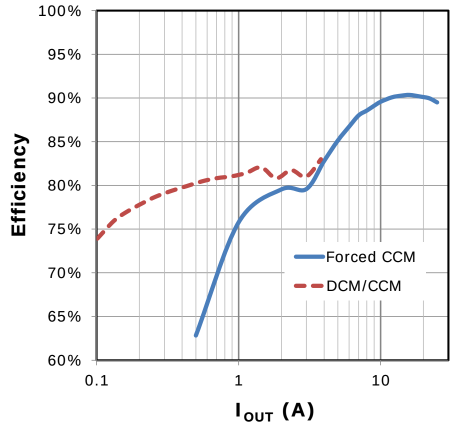


Fig. 17: Efficiency, $12V_{IN}$, $1.8V_{OUT}$, 1uH, 300kHz

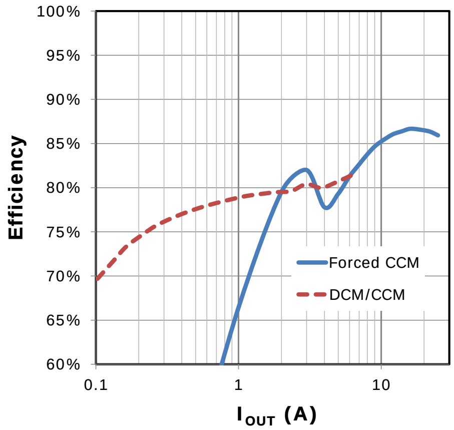


Fig. 18: Efficiency, $12V_{IN}$, $1.2V_{OUT}$, 0.47uH, 300kHz

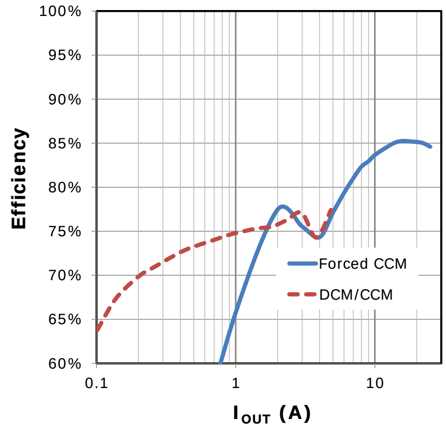


Fig. 19: Efficiency, $12V_{IN}$, $1.0V_{OUT}$, 0.47uH, 300kHz

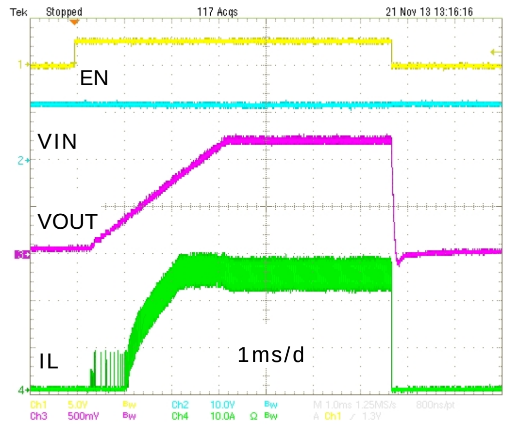


Fig. 20: Enable turn on/turn off, $12V_{IN}$, $1.2V_{OUT}$, 25A

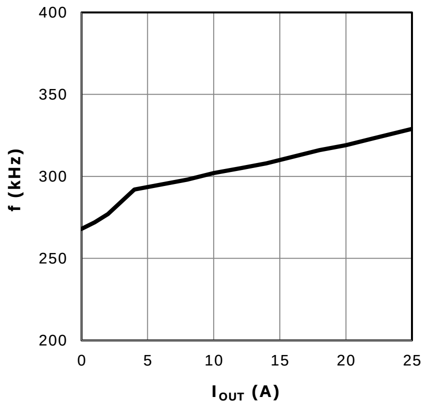


Fig. 22: frequency versu I_{OUT}, Forced CCM

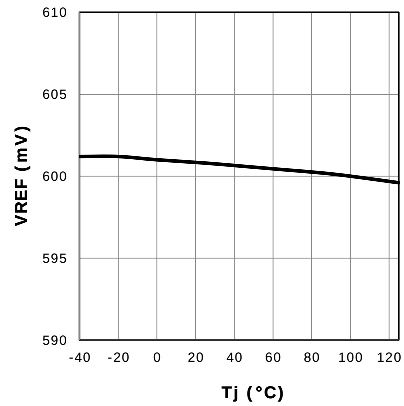


Fig. 23: VREF versus temperature

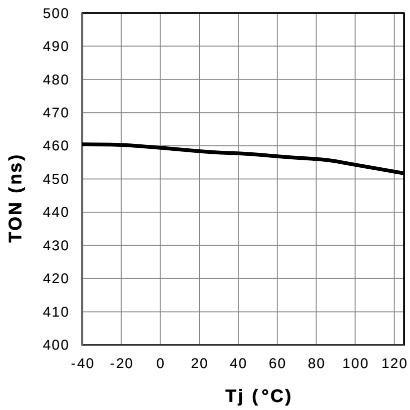


Fig. 24: On-Time versus temperature

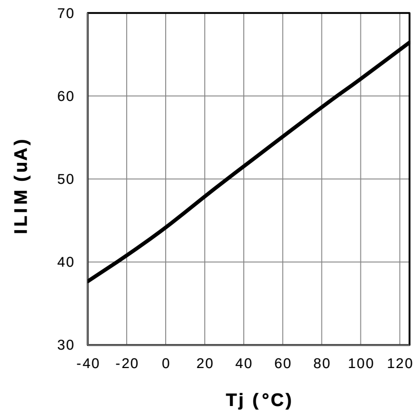


Fig. 25: ILIM versus temperature

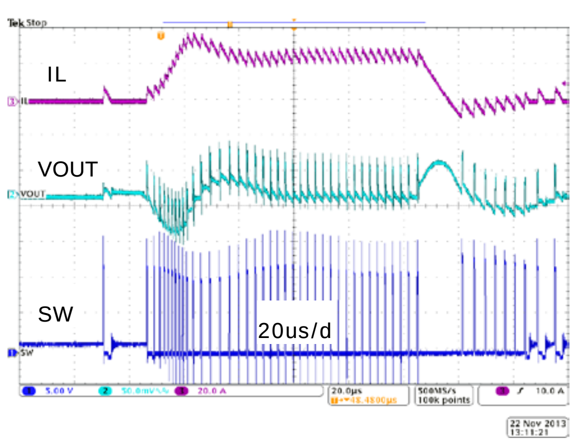


Fig. 26: Load step, DCM/CCM, 0A-25A-0A

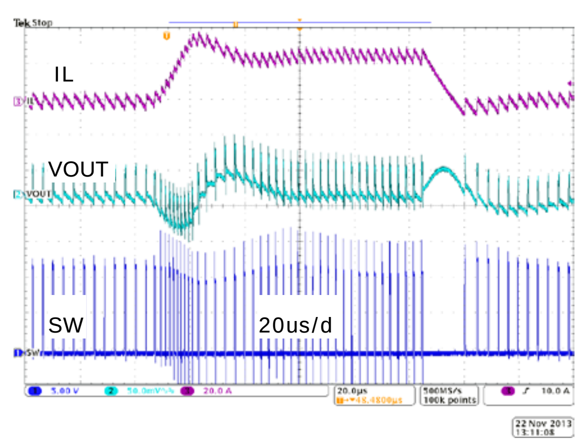


Fig. 27: Load step, Forced CCM, 0A-25A-0A

Detailed Operation

XRP6141 is a synchronous step-down proprietary emulated current-mode Constant On-Time (COT) controller. The on-time, which is programmed via RON, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control allows the use of ceramic output capacitors.

Each switching cycle begins with GH signal turning the high-side (switching) FET for a preprogrammed time. At the end of the on-time the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the minimum off-time the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When VFB drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable / Mode input (EN / MODE)

EN/MODE pin accepts a tri-level signal that is used to control turn on/off. It also selects between two modes of operation: 'Forced CCM' and 'DCM/CCM'. If EN is pulled below 1.9V, the controller shuts down. A voltage between 1.9V and 3.0V selects the Forced CCM mode which will run the converter in continuous conduction at all times. A voltage higher than 3.0V selects the DCM/CCM mode which will run the converter in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the controller to operate in Forced CCM, a voltage between 1.9V and 3.0V must be applied to the EN/MODE pin. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in figure 28 can be used to generate the required voltage. Note that at V_{IN} of 5.5V to 22V the nominal Zener voltage is 4.0V to 5.0V respectively. Therefore, for V_{IN} in the range of 5.5V to 22V, the circuit shown in figure 28 will generate voltage at the EN/MODE pin required for Forced CCM.

Selecting the DCM / CCM Mode

In order to set the controller operation to DCM/CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to the EN/MODE pin. In applications where an external control signal is not available, EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4V. If V_{IN} varies over a wide range, the circuit shown in figure 29 can be used to generate the required voltage.

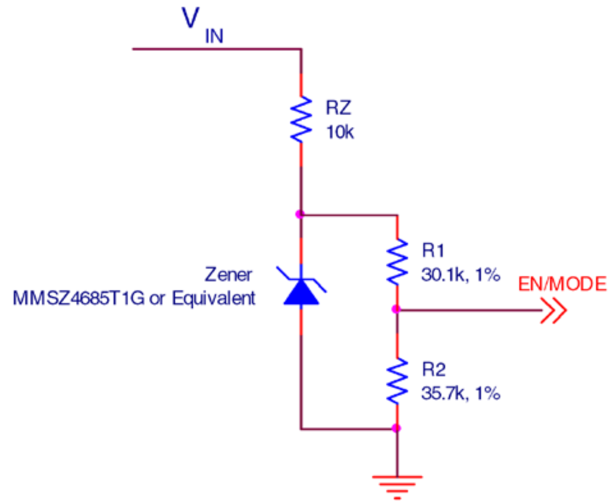


Figure 28. Selecting Forced CCM by deriving EN/MODE from V_{IN}

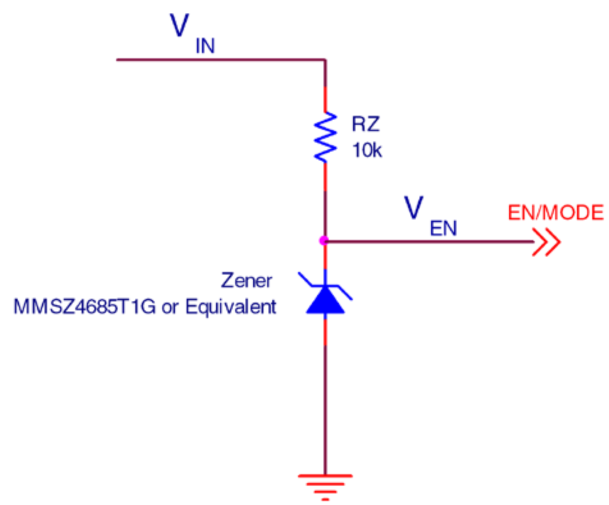


Figure 29. Selecting DCM/CCM by deriving EN/MODE from V_{IN}

Programming the On-Time

The on-time TON is programmed via resistor RON according to following equation:

$$TON = \frac{(3.4E-10) \times RON}{VIN}$$

The required TON for a given application is calculated from:

$$TON = \frac{VOUT}{VIN \times f}$$

Note that switching frequency f will increase somewhat, as a function of increasing load current and increasing losses (see figure 22).

OVER-CURRENT PROTECTION (OCP)

If load current exceeds the programmed over-current I_{OCP} for four consecutive switching cycles, then IC enters hiccup mode of operation. In hiccup the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The IC will remain in hiccup mode until load current is reduced below the programmed I_{OCP}. In order to program over-current protection use the following equation:

$$RLIM = \frac{(IOCP \times RDS) + 8mV}{ILIM}$$

Where:

RLIM is resistor value for programming I_{OCP}

I_{OCP} is the over-current value to be programmed

RDS is the MOSFET rated on resistance

8mV is the OCP comparator offset

I_{LIM} is the internal current that generates the necessary OCP comparator threshold (use 45uA)

Note that I_{LIM} has a positive temperature coefficient of 0.4%/°C. This is meant to roughly match and compensate for positive temperature coefficient of the synchronous FET. In order for this feature to be effective the temperature rise of the IC should approximately match the temperature rise of the FET.

SHORT-CIRCUIT PROTECTION (SCP)

If the output voltage drops below 60% of its programmed value, the IC will enter hiccup mode. Hiccup will persist until short-circuit is removed. SCP circuit becomes active after PGOOD asserts high.

OVER-TEMPERATURE PROTECTION (OTP)

OTP triggers at a nominal die temperature of 150°C. The gate of switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

PROGRAMMING THE OUTPUT VOLTAGE

Use an external voltage divider as shown in figure 1 to program the output voltage VOUT.

$$R1 = R2 \times \left(\frac{VOUT}{0.6} - 1\right)$$

R2 recommended range is 2kΩ to 10kΩ.

PROGRAMMING THE SOFT-START

Place a capacitor CSS between the SS and GND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance CSS from the following equation:

$$CSS = TSS \times \frac{10uA}{0.6V}$$

FEED-FORWARD CAPACITOR (C_{FF})

A feed-forward capacitor (C_{FF}) may be necessary depending on the Equivalent Series Resistance (ESR) of C_{OUT}. If only ceramic output capacitors are used then a C_{FF} is necessary. Calculate C_{FF} from:

$$CFF = \frac{1}{2 \times \pi \times R1 \times 7 \times fLC}$$

where:

R1 is the resistor that C_{FF} is placed in parallel with

f_{LC} is the frequency of the output filer double pole

f_{LC} must be less than 15kHz when using ceramic C_{OUT}. If necessary, increase C_{OUT} and/or L in order to meet this constraint.

When using capacitors with higher ESR such as Panasonic TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of the output LC double pole f_{LC} should be less than 10kHz.
2. The frequency of ESR zero $f_{ZERO,ESR}$ should be at least five times larger than f_{LC}.

Note that if $f_{ZERO,ESR}$ is less than 5 x f_{LC}, then it is recommended to set the f_{LC} at less than 2kHz. C_{FF} is still not required.

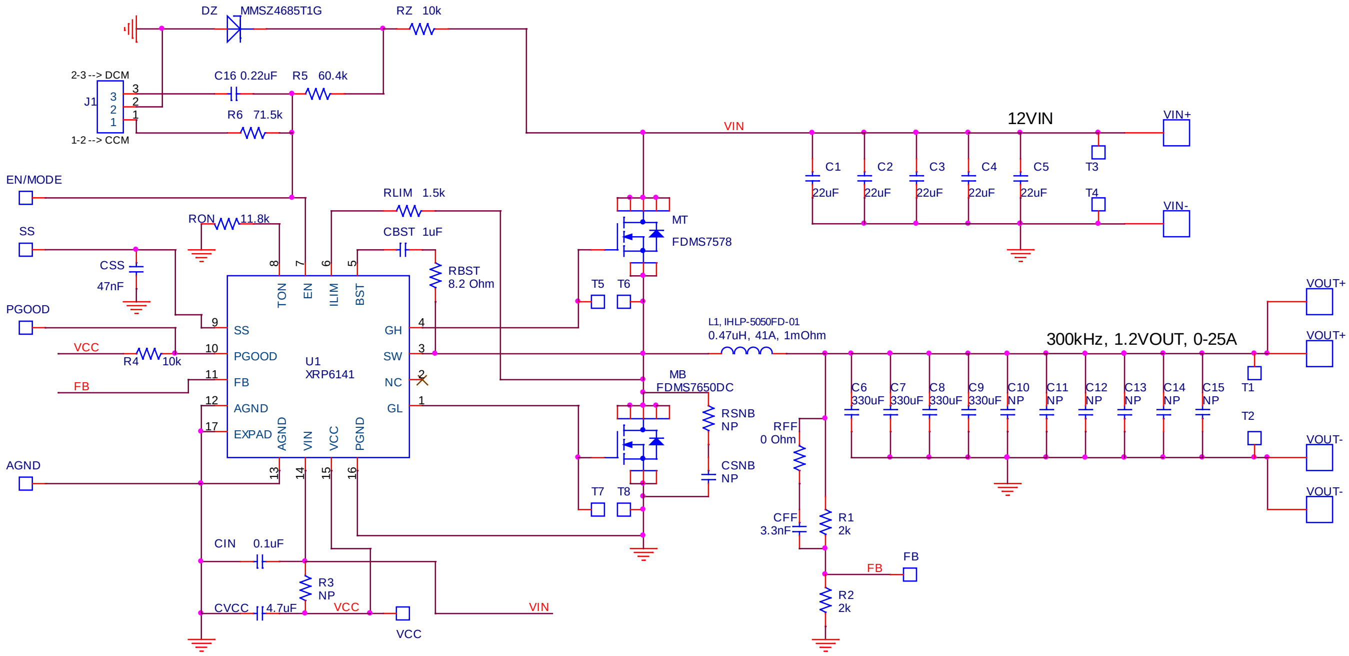
FEED-FORWARD RESISTOR (R_{FF})

Poor PCB layout and/or extremely fast switching FETs can cause switching noise at the output and may couple to the FB pin via C_{FF}. Excessive noise at FB will cause poor load regulation. To solve this problem place a resistor R_{FF} in series with C_{FF}. R_{FF} value up to 2% of R1 is acceptable.

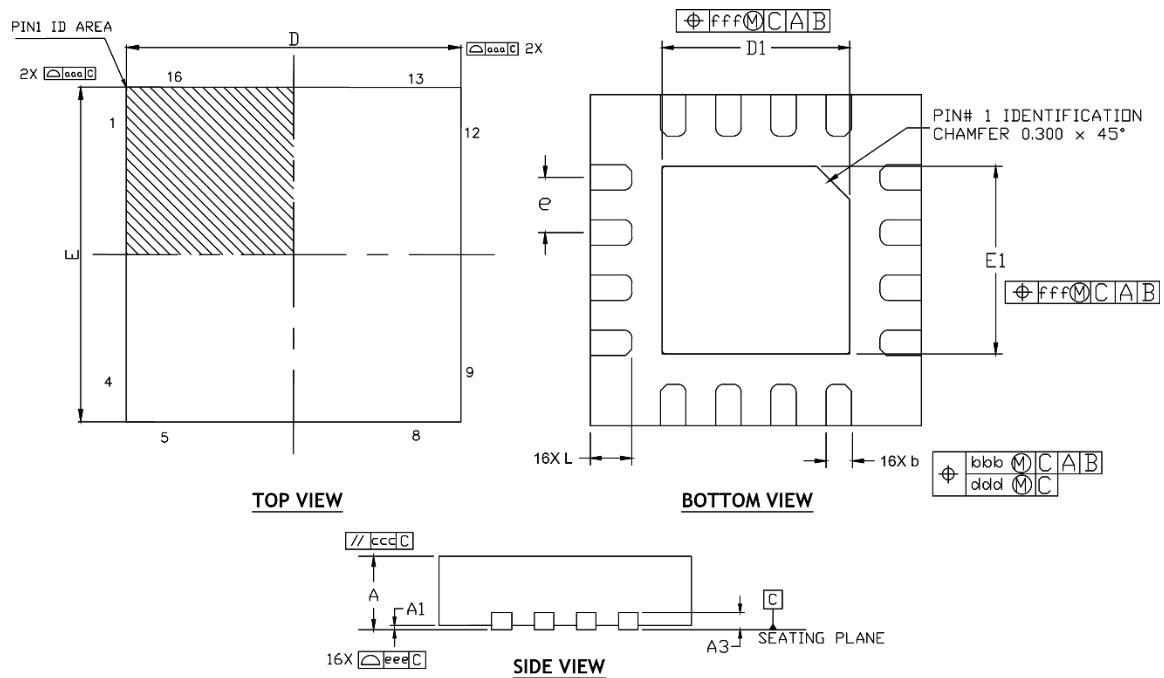
MAXIMUM ALLOWABLE VOLTAGE RIPPLE AT FB PIN

Note that the steady-state voltage ripple at feedback pin ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the controller to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV then C_{OUT} should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

Applications Circuit



MECHANICAL DIMENSIONS — 16 PIN 3X3 QFN



DIMENSION TABLE			
SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20Ref	
b	0.18	0.25	0.30
D		3.00 BSC	
E		3.00 BSC	
e		0.50 BSC	
D1	1.50	1.65	1.80
E1	1.50	1.65	1.80
L	0.20	0.30	0.40
K	0.20	–	–
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
N		16	

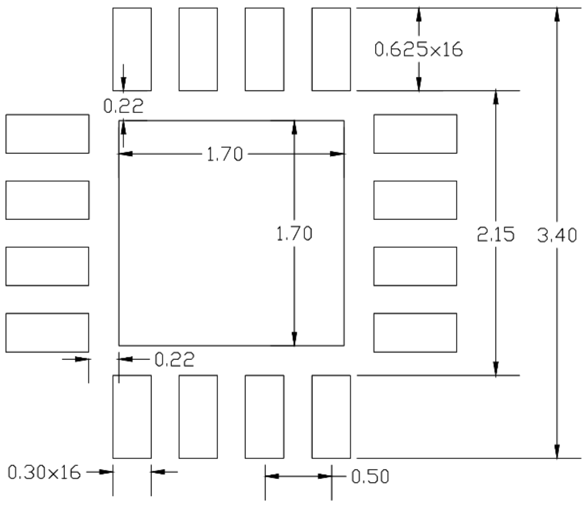
TERMINAL DETAILS

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCE PER JEDEC MO-220.

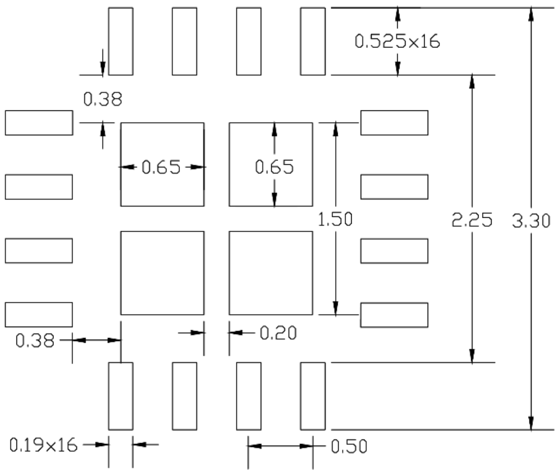
Drawing No.: POD- 00000138

Revision: A

RECOMMENDED LAND PATTERN AND STENCIL



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

Drawing No.: POD- 00000138

Revision: A

REVISION HISTORY

Revision	Date	Description
1.0.0	12/16/2013	Initial release
1.0.1	12/20/2013	Specification improvement
2.0.0	7/31/2005	Modified Functional Block Diagram, Application Circuit, Feed-Forward Capacitor; added “Selecting the Forced CCM Mode”, “Selecting the DCM/CCM Mode”, “Feed-Forward Resistor”, “Maximum Allowable Voltage Ripple at FB Pin” sections.
2.0.1	11/23/2015	Change VCC Linear Regulator Dropout Voltage from 200mV min and 300mV typ to 200mV typ
2.0.2	5/24/2018	Update to MaxLinear logo. Update format and Ordering Information table. Added Revision History.

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