To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR
2SK4080

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4080 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 9.0 mΩ MAX. (V_{GS} = 10 V, I_D = 24 A)
- Low Q_{GD}: Q_{GD} = 6.3 nC TYP.
- 4.5 V drive available

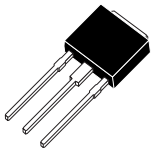
ORDERING INFORMATION

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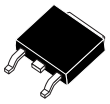
PART NUMBER	PACKAGE
2SK4080(1)-S27-AY Note	TO-251 (MP-3-b)
2SK4080-ZK-E1-AY Note	TO-252 (MP-3ZK)
2SK4080-ZK-E2-AY Note	TO-252 (MP-3ZK)

Note Pb-free (This product does not contain Pb in external electrode.)

(TO-251)



(TO-252)



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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±48	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±144	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	29	W
Total Power Dissipation	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	21	A
Single Avalanche Energy Note2	E_{AS}	44.1	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

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Date Published March 2007 NS CP(K)
Printed in Japan

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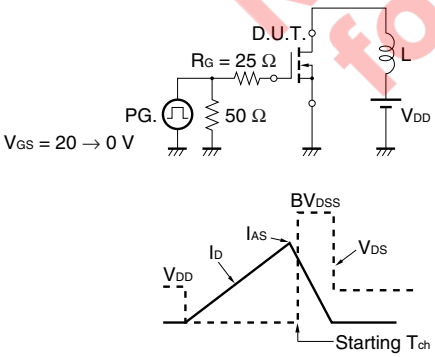
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 12 A	7	14		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 24 A		7.0	9.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 24 A		10.2	15	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		1670		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		290		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		150		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V		10		ns
Rise Time	t_r	I_D = 30 A		5.3		ns
Turn-off Delay Time	$t_{d(off)}$	V_{GS} = 12 V		42		ns
Fall Time	t_f	R_G = 3 Ω		6.1		ns
Total Gate Charge	Q_{G1}	V_{DD} = 15 V, V_{GS} = 12 V, I_D = 30 A		32		nC
	Q_{G2}	V_{DD} = 15 V, V_{GS} = 4.5 V, I_D = 30 A		13		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 15 V		4.6		nC
Gate to Drain Charge	Q_{GD}	I_D = 30 A		6.3		nC
Gate Resistance	R_G			2.4		Ω
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 30 A, V_{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 30 A, V_{GS} = 0 V		29		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		23		nC

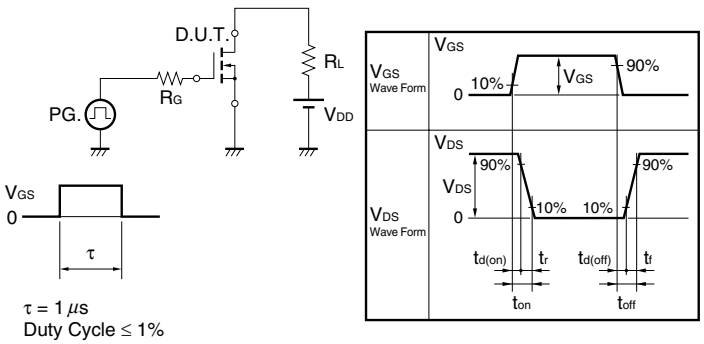
Note Pulsed

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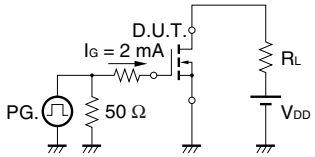
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



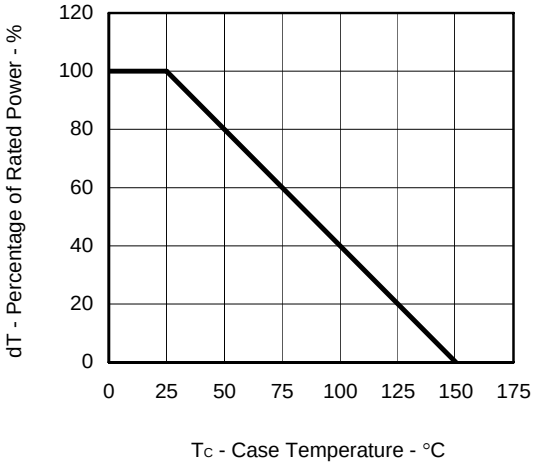
TEST CIRCUIT 3 GATE CHARGE



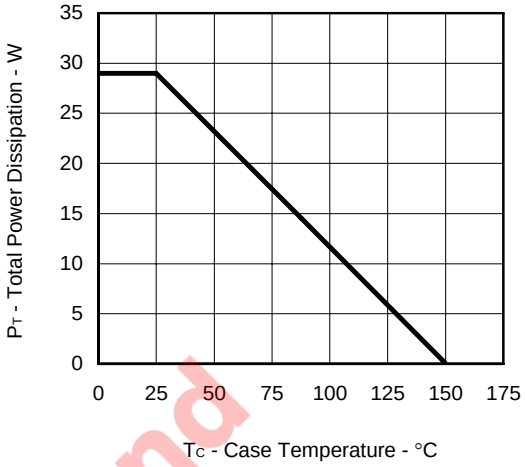
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TYPICAL CHARACTERISTICS (T_A = 25°C)

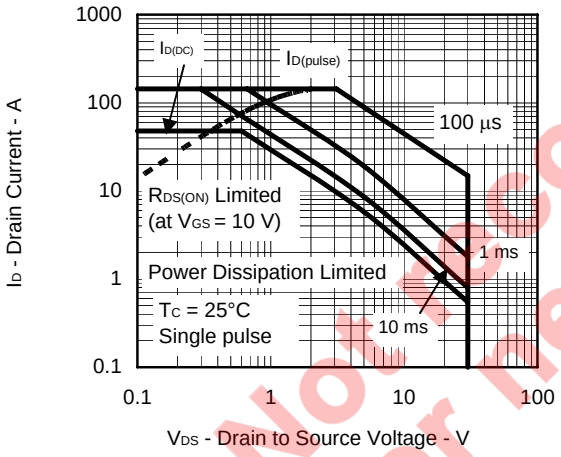
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



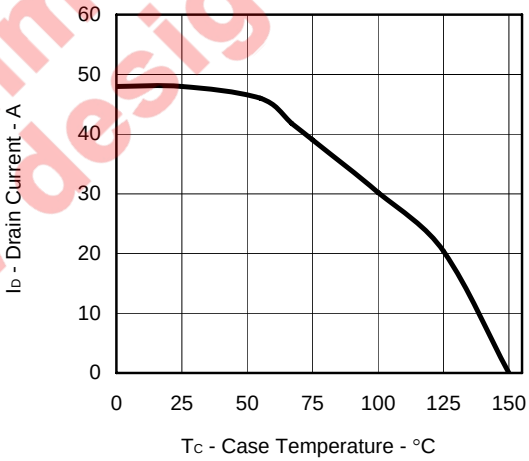
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



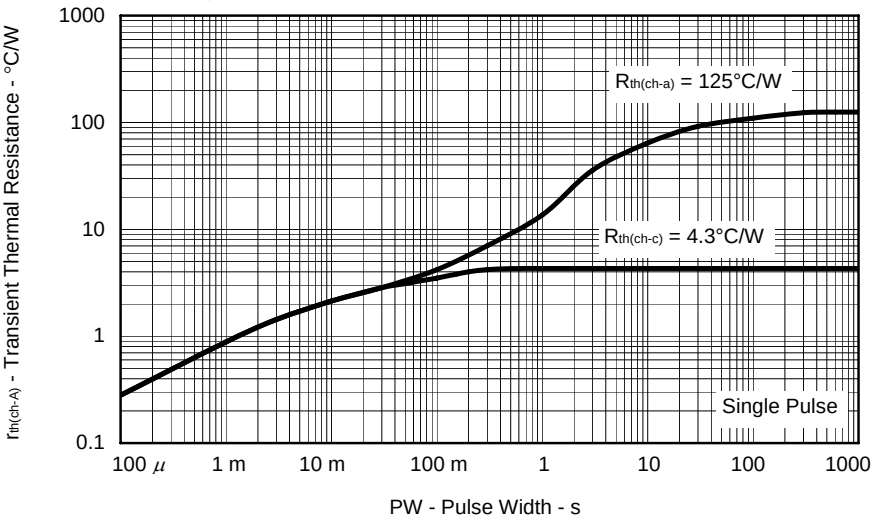
FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. CASE TEMPERATURE



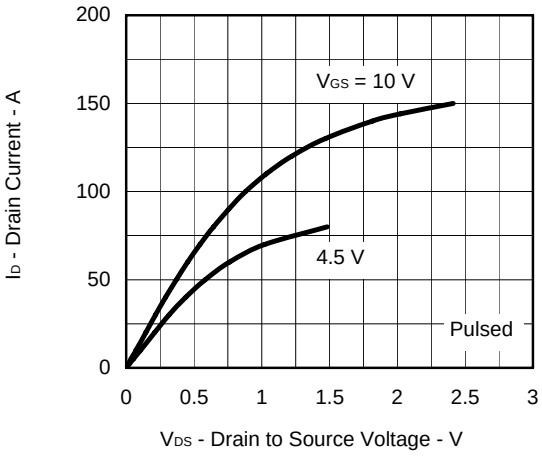
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



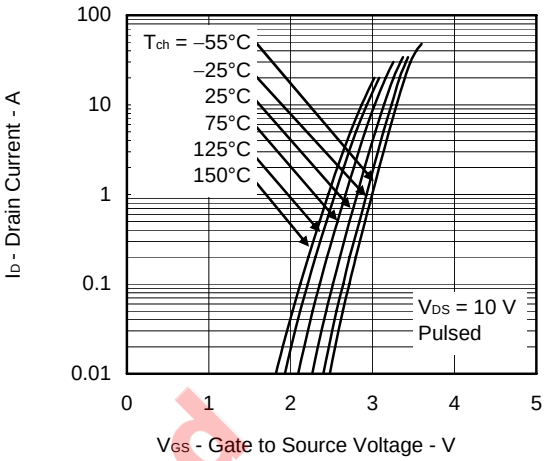
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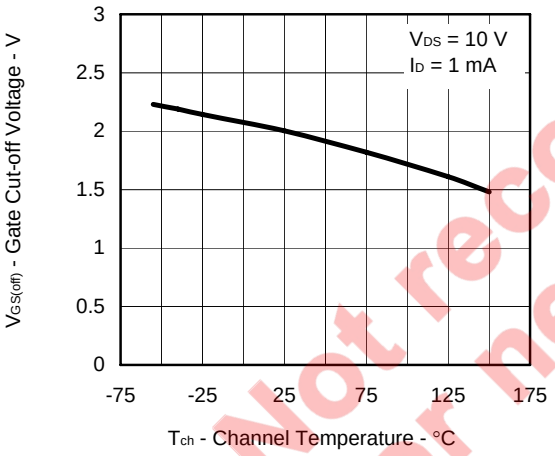
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



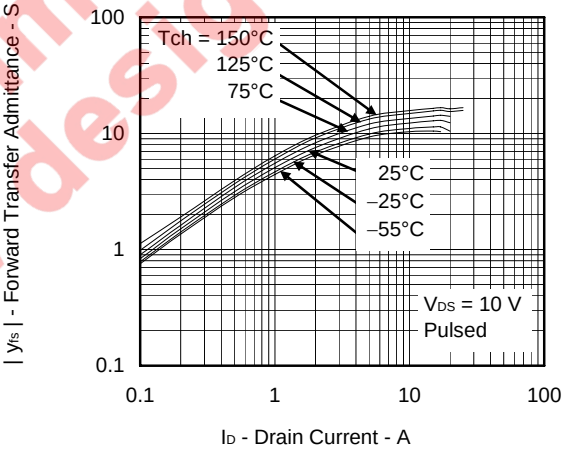
FORWARD TRANSFER CHARACTERISTICS



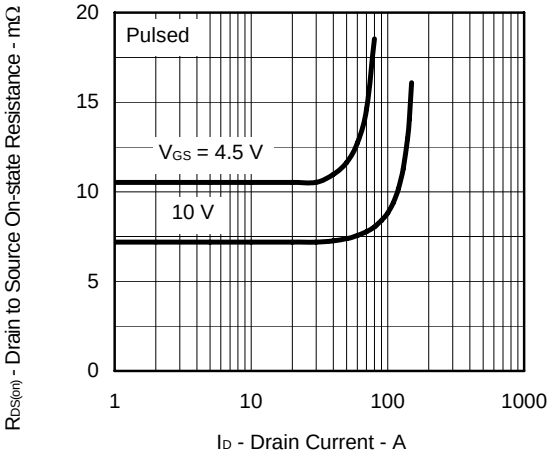
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



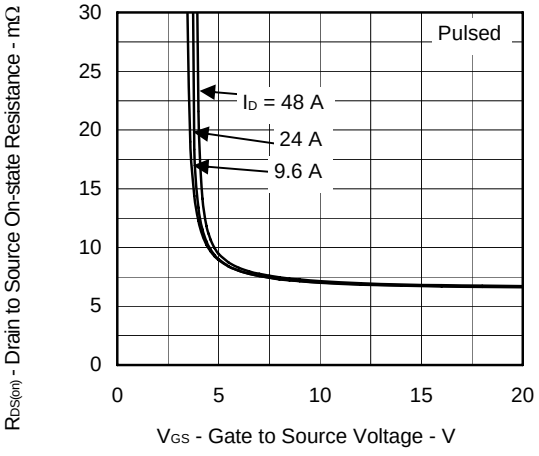
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



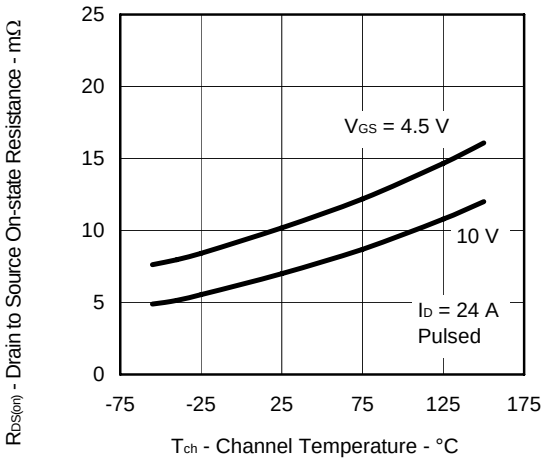
DRAIN TO SOURCE ON-STATERESISTANCE vs.
GATE TO SOURCE VOLTAGE



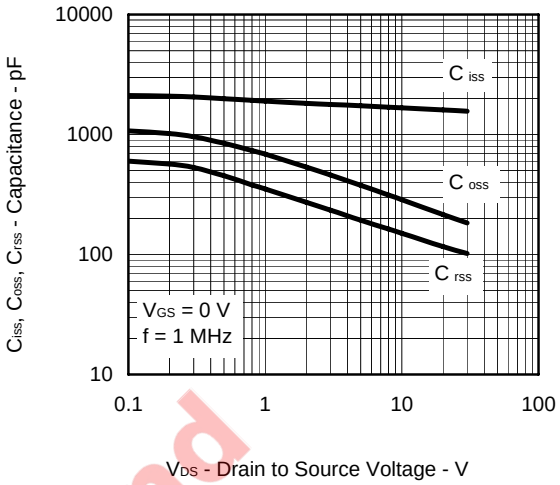
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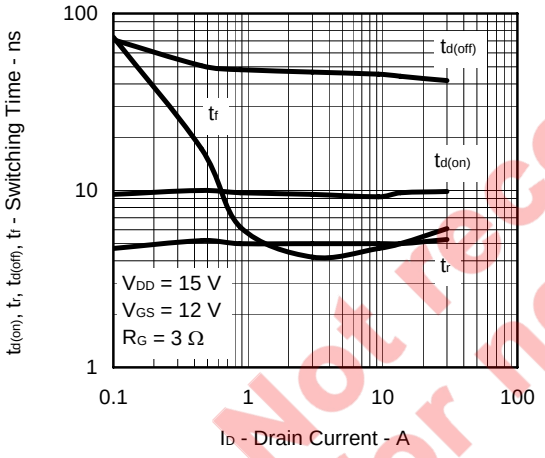
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



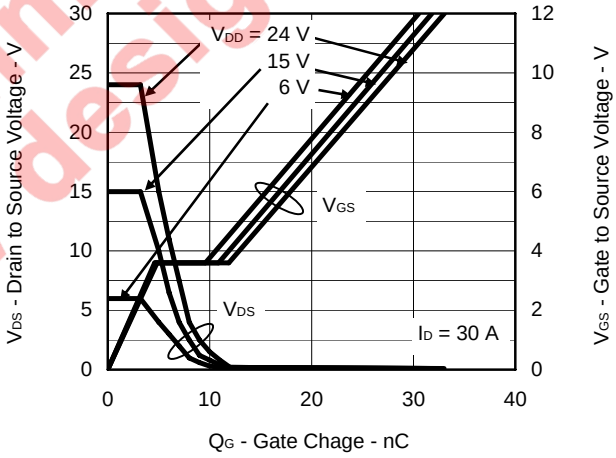
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



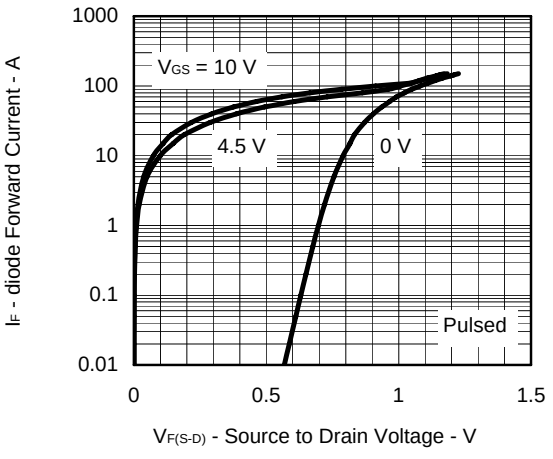
SWITCHING CHARACTERISTICS



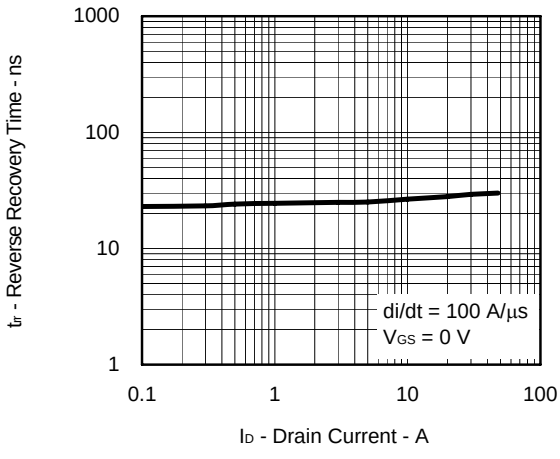
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



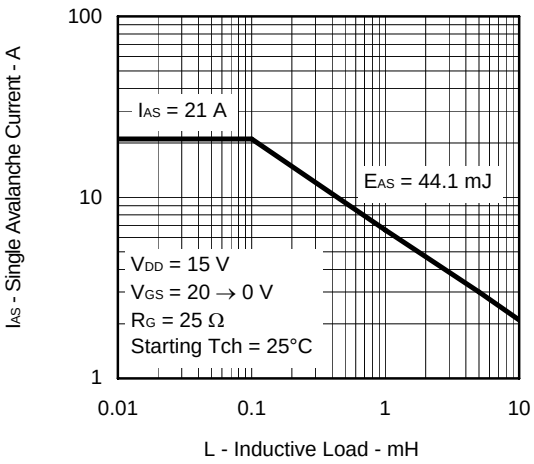
REVWESE RECOVERY TIME vs. DRAIN CURRENT



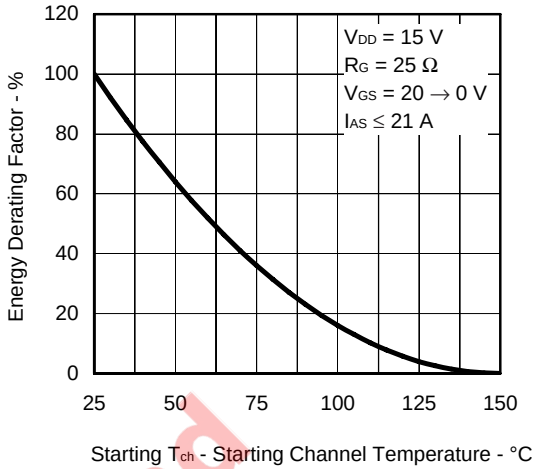
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SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR

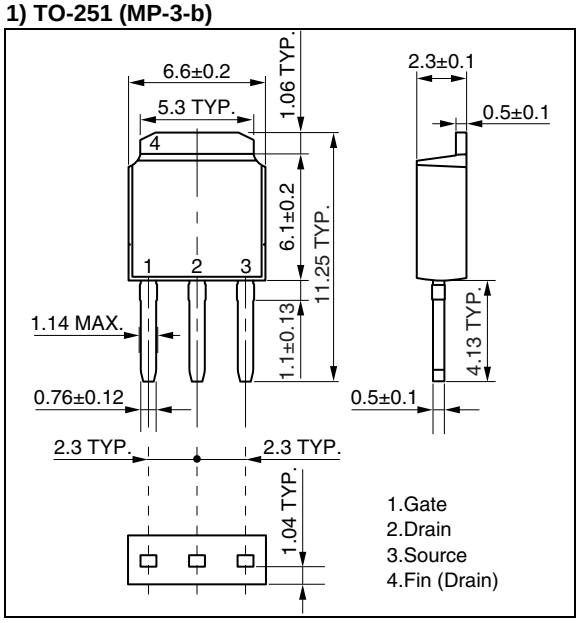


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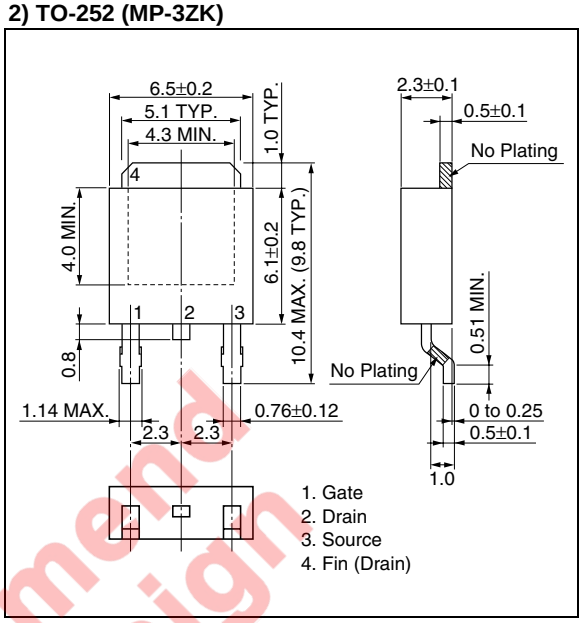
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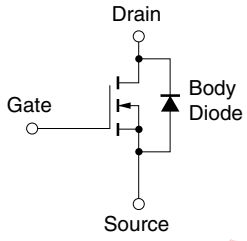
<R> **1) TO-251 (MP-3-b)**



2) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



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Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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