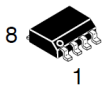
CAN FD Transceiver, High Speed
NCV7357



SOIC−8
D SUFFIX
CASE 751−07

DFNW8
MW SUFFIX
CASE 507AB

Description

The NCV7357 CAN FD transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7357 is an addition to the CAN high−speed transceiver family complementing NCV7344 CAN stand−alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc.

The NCV7357 guarantees additional timing parameters to ensure robust communication at data rates beyond 1 Mbps to cope with CAN flexible data rate requirements (CAN FD). These features make the NCV7357 an excellent choice for all types of HS−CAN networks, in nodes that require only a basic CAN capability.

Features

- Compliant with ISO 11898−2:2016
- CAN FD Timing Specified up to 5 Mbps
- V_{IO} Pin on NCV7357−3 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- Low Current, Listen Only Silent Mode
- Low Electromagnetic Emission (EME) and High Electromagnetic Immunity
- Very Low EME without Common−mode (CM) Choke
- No Disturbance of the Bus Lines with an Unpowered Node
- Transmit Data (TxD) Dominant Timeout Function
- Under All Supply Conditions the Chip Behaves Predictably
- Very High ESD Robustness of Bus Pins, >8 kV System ESD Pulses
- Thermal Protection
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- Bus Pins Protected Against Transients in an Automotive Environment
- These are Pb−free Devices

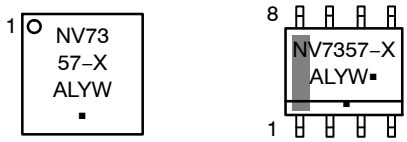
Quality

- Wettable Flank Package for Enhanced Optical Inspection
- AEC−Q100 Grade 0 Qualified and PPAP Capable

Typical Applications

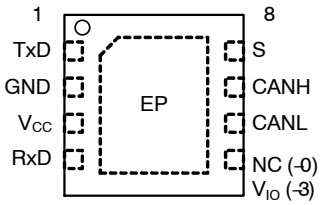
- Automotive
- Industrial Networks

MARKING DIAGRAM

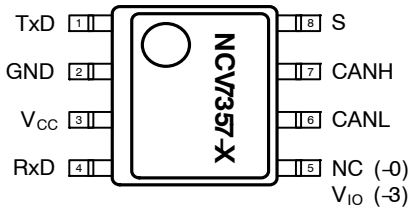


NV7357−X = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN ASSIGNMENT



NCV7357MWx
(Top View)



NCV7357D1x
(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 11 of this data sheet.

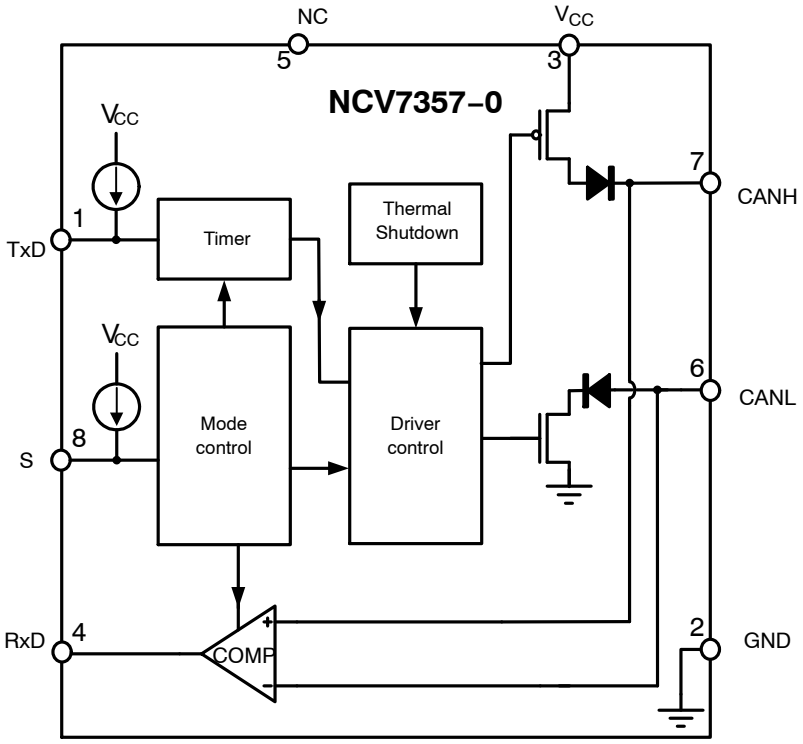


Figure 1. NCV7357−0 Block Diagram

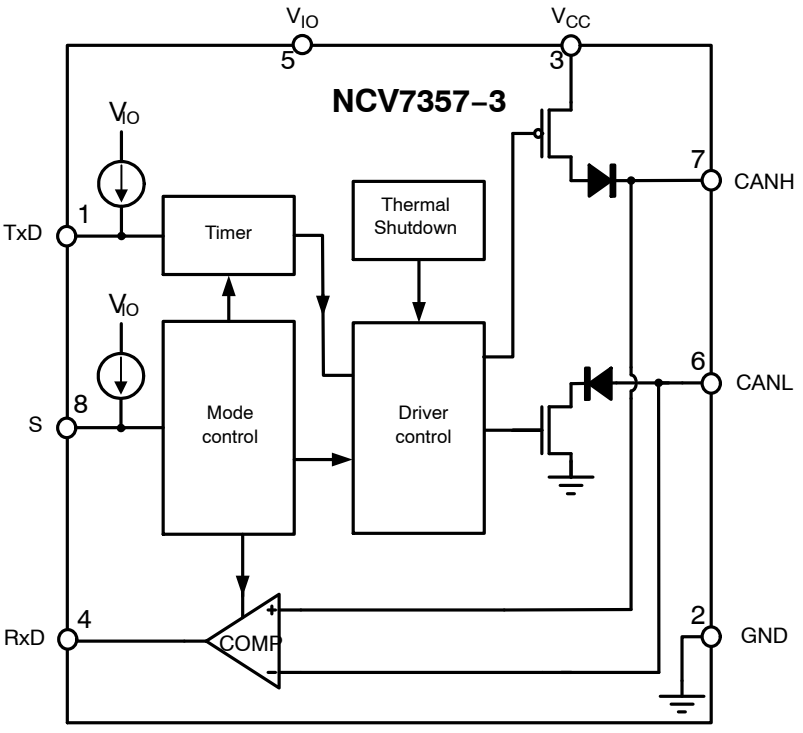


Figure 2. NCV7357−3 Block Diagram

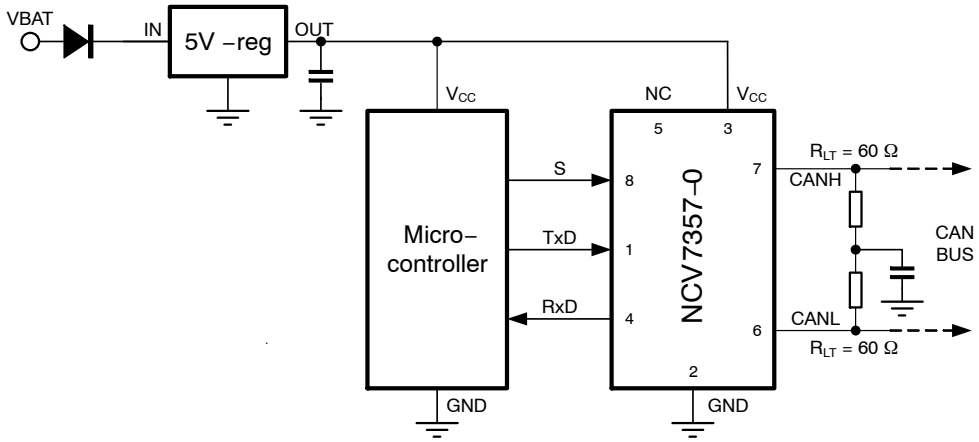


Figure 3. Application Diagram NCV7357−0

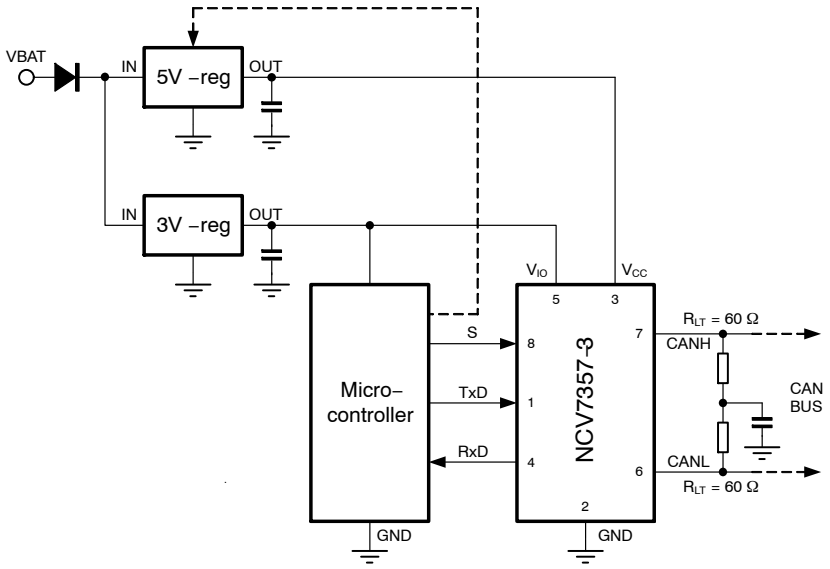


Figure 4. Application Diagram NCV7357−3

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD	Transmit data input; low input → dominant driver; internal pull−up current
2	GND	Ground
3	V_{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter → low output
5 5	NC V_{IO}	Not connected. On NCV7357−0 only Digital Input / Output pins supply voltage. On NCV7357−3 only
6	CANL	Low−level CAN bus line (low in dominant mode)
7	CANH	High−level CAN bus line (high in dominant mode)
8	S	Silent mode control input; internal pull−up current
	EP	Exposed Pad. Recommended to connect to GND or left floating in application (DFNW8 package only).

FUNCTIONAL DESCRIPTION

High speed CAN FD transceiver

NCV7357 implements high−speed physical layer CAN FD transceiver compatible with ISO11898−2, implementing following optional features or alternatives:

- Extended bus load range
- Transmit dominant timeout, long
- Support of bit rates up to 5 Mbps
- Normal Bus biasing

Operating Modes

NCV7357 provides two modes of operation as illustrated in Table 2. These modes are selectable through pin S.

Table 2. OPERATING MODES

Pin S	Mode	Pin TxD	BUS	Pin RxD
Low	Normal	0	Dominant	0
		1	Recessive	1
High	Silent	X	Dominant (1)	0
		X	Recessive	1

1. CAN BUS driven by another transceiver on the BUS
2. 'X' = don't care

Power−off

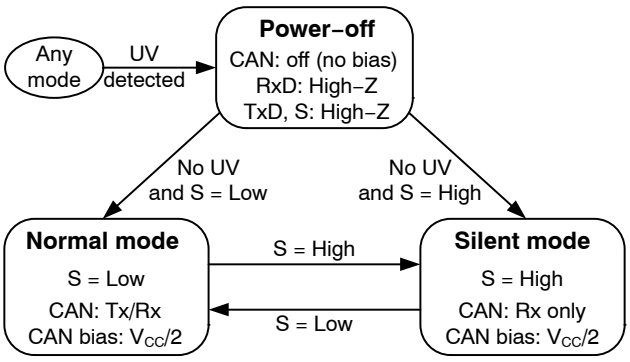
This virtual mode is entered as soon as the V_{CC} or V_{IO} undervoltage condition is detected. The internal logic is reset and the transceiver is disabled. CAN bus pins are kept floating. As soon as both V_{CC} and V_{IO} voltages rise above corresponding undervoltage recovery thresholds, the device proceeds to Normal or Silent mode, depending on S pin state.

Normal Mode

In the normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give low EME.

Silent Mode

In the silent mode, the transmitter is disabled. The bus pins are in recessive state independent of TxD input. Transceiver listens to the bus and provides data to controller, but controller is prevented from sending any data to the bus.



Notes:
NCV7357−0
UV detected: $V_{CC} < V_{UVDVCC}$
No UV: $V_{CC} > V_{UVDVCC}$

NCV7357−3
UV detected: $V_{CC} < V_{UVDVCC}$ and/or $V_{IO} < V_{UVDVIO}$
No UV: $V_{CC} > V_{UVDVCC}$ and $V_{IO} > V_{UVDVIO}$

Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds $T_{J(sd)}$ value. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off−state resets when the temperature decreases below the shutdown threshold and pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

TxD Dominant Timeout Function

A TxD dominant timeout timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant timeout time $t_{dom(TxD)}$ defines the minimum possible bit rate to 17 kbps.

Fail Safe Features

A current−limiting circuit protects the transmitter output stage from damage caused by accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

Detection of undervoltage on supply pin (V_{CC} or V_{IO}) causes switching off device. After supply voltage is recovered TxD pin must be first released to high to allow sending dominant bits again.

The pins CANH and CANL are protected from automotive electrical transients (according to ISO 7637; see

Figure 7). Pins TxD and S are biased internally should the input become disconnected. Pins TxD, S and RxD will be floating, preventing reverse supply should the VCC supply be removed.

V_{IO} Supply Pin

The V_{IO} pin (available only on NCV7357−3 version) should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. See Figure 4.

ABSOLUTE MAXIMUM RATINGS

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SUP}	Supply voltage V_{CC}, V_{IO}		−0.3	+6.0	V
V_{CANH}	DC voltage at pin CANH	0 < V_{CC} < 5.5 V; no time limit	−42	+42	V
V_{CANL}	DC voltage at pin CANL	0 < V_{CC} < 5.5 V; no time limit	−42	+42	V
$V_{CANH\ -\ CANL}$	DC voltage between CANH and CANL		−42	+42	V
V_{IN}	DC voltage at pin TxD, S		−0.3	+6.0	V
V_{OUT}	DC voltage at pin RxD		−0.3	V_{SUP} + 0.3	V
V_{esdHBM}	Electrostatic discharge voltage at all pins, Component HBM	(Note 3)	−6	+6	kV
V_{esdCDM}	Electrostatic discharge voltage at all pins, Component CDM	(Note 4)	−750	+750	V
V_{esdIEC}	Electrostatic discharge voltage at pins CANH and CANL, System HBM (Note 6)	(Note 5)	−8	+8	kV
V_{schaff}	Voltage transients, pins CANH, CANL. Test Pulses According to ISO7637−2, Class C (Note 6)	test pulses 1	−100		V
		test pulses 2a		+75	V
		test pulses 3a	−150		V
		test pulses 3b		+100	V
Latch−up	Static latch−up at all pins	(Note 7)		150	mA
T_{stg}	Storage temperature		−55	+150	°C
T_J	Maximum junction temperature		−40	+170	°C
MSL_{SOIC}	Moisture sensitivity level for SOIC−8		2		−
MSL_{DFN}	Moisture sensitivity level for DFNW8		1		−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA−JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor
4. Standardized charged device model ESD pulses when tested according to AEC−Q100−011
5. System human body model electrostatic discharge (ESD) pulses in accordance to IEC 61000−4−2. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND
6. Results were verified by external test house
7. Static latch−up immunity: Static latch−up protection level when tested according to EIA/JESD78

Table 4. THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal characteristics SOIC−8 (Note 8) Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 9) Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 10)	 $R_{\theta JA}$ $R_{\theta JA}$	 131 81	 °C/W °C/W
Thermal characteristics DFNW8 (Note 8) Thermal Resistance Junction−to−Air, Free air, 1S0P PCB (Note 9) Thermal Resistance Junction−to−Air, Free air, 2S2P PCB (Note 10)	 $R_{\theta JA}$ $R_{\theta JA}$	 125 58	 °C/W °C/W

8. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters
9. Values based on test board according to EIA/JEDEC Standard JESD51−3, signal layer with 10% trace coverage
10. Values based on test board according to EIA/JEDEC Standard JESD51−7, signal layers with 10% trace coverage

Table 5. ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive currents flow into the respective pin)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{CC})						
V_{CC}	Power supply voltage	(Note 11)	4.75	5.0	5.25	V
I_{CC}	Supply current in Normal mode	Dominant; V_{TxD} = Low	30	45	55	mA
		Recessive; V_{TxD} = High	2.0	5.0	10	mA
		Normal mode, Dominant; V_{TxD} = 0 V; one of bus wires shorted −3 V ≤ (V_{CANH}, V_{CANL}) ≤ +18 V	2.0	–	105	mA
I_{CCS}	Supply current in silent mode NCV7357−3 version		0.1	–	1.3	mA
	Supply current in silent mode NCV7357−0 version		0.1	–	1.5	mA
V_{UVDVCC}	Undervoltage detection on V_{CC} pin		3.5	4.0	4.3	V
V_{IO} SUPPLY VOLTAGE (Pin V_{IO}) Only for NCV7357−3 version						
V_{IO}	Supply voltage on pin V_{IO}		2.8	–	5.5	V
I_{IOS}	Supply current on pin V_{IO} in silent mode	V_{TxD} = VIO	–	120	200	μA
I_{IONM}	Supply current on pin V_{IO} during normal mode	Dominant; V_{TxD} = Low	–	700	900	μA
		Recessive; V_{TxD} = High	–	460	600	
V_{UVDVIO}	Undervoltage detection voltage on V_{IO} pin		2.0	2.3	2.6	V
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH}	High−level input voltage	Output recessive	2.0	–	–	V
V_{IL}	Low−level input voltage	Output dominant	−0.3	–	0.8	V
I_{IH}	High−level input current	V_{TxD} = V_{CC} / V_{IO}	−5.0	0	5.0	μA
I_{IL}	Low−level input current	V_{TxD} = 0 V	−300	−150	−75	μA
C_i	Input capacitance	(Note 12)	–	5	10	pF
TRANSMITTER DATA INPUT (Pin S)						
V_{IH}	High−level input voltage	Silent mode	2.0	–	–	V
V_{IL}	Low−level input voltage	Normal mode	−0.3	–	0.8	V
I_{IH}	High−level input current	V_S = V_{CC} / V_{IO}	−1.0	0	1.0	μA
I_{IL}	Low−level input current	V_S = 0 V	−15	–	−1.0	μA
C_i	Input capacitance	(Note 12)	–	5	10	pF

Table 5. ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive currents flow into the respective pin)

RECEIVER DATA OUTPUT (Pin RxD)

I_{OH}	High−level output current	Normal mode $V_{RxD} = V_{CC} / V_{IO} - 0.4$ V	−8.0	−3.0	−1.0	mA
I_{OL}	Low−level output current	V_{RxD} = 0.4 V	1.0	6.0	12	mA

CAN TRANSMITTER (PINS CANH AND CANL)

$V_{o(dom)(CANH)}$	Dominant output voltage at pin CANH	Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 50 Ω < R_{LT} < 65 Ω	2.75	3.5	4.5	V
$V_{o(dom)(CANL)}$	Dominant output voltage at pin CANL	Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 50 Ω < R_{LT} < 65 Ω	0.5	1.5	2.25	V
$V_{o(rec)}$	Recessive output voltage at pins CANH and CANL	Normal or Silent mode; V_{TxD} = High or V_{TxD} = Low and $t > t_{dom(TxD)}$; no load	2.0	2.5	3.0	V
$V_{o(dom)(diff)}$	Differential dominant output voltage ($V_{CANH} - V_{CANL}$)	Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; 45 Ω < R_{LT} < 65 Ω	1.5	2.25	3.0	V
$V_{o(dom)(diff)\_ARB}$		Normal mode; V_{TxD} = Low; $t < t_{dom(TxD)}$; R_{LT} = 2 240 Ω (Note 12)	1.5	–	5.0	V
$V_{o(rec)(diff)}$	Differential recessive output voltage ($V_{CANH} - V_{CANL}$)	Normal or Silent mode; V_{TxD} = High or V_{TxD} = Low and $t > t_{dom(TxD)}$; no load	−50	0	+50	mV
$V_{o(dom)(sym)}$	Dominant output voltage driver symmetry $V_{o(dom)(sym)} = V_{o(CANH)(dom)} + V_{o(CANL)(dom)}$	TxD = square wave up to 1 MHz; C_{ST} = 4.7 nF	0.9	1.0	1.1	V_{CC}
$I_{o(sc)(CANH)}$	Short circuit output current at pin CANH in dominant	Normal mode; TxD = Low, $t < t_{dom(TxD)}$; −3 V ≤ V_{CANH} ≤ +18 V	−100	−70	+1.0	mA
$I_{o(sc)(CANL)}$	Short circuit output current at pin CANL in dominant	Normal mode; TxD = Low, $t < t_{dom(TxD)}$; −3 V ≤ V_{CANL} ≤ +36 V	−1.0	+70	+100	mA
$I_{o(sc)(rec)}$	Short circuit output current at pins CANH and CANL in recessive	Normal or Silent mode; TxD = High, −27 V < V_{CANH}, V_{CANL} < +32 V	−5.0	–	+5.0	mA

CAN RECEIVER (Pins CANH and CANL)

$I_{LEAK(off)}$	Input leakage current	0 Ω < R(V_{CC} to GND) < 1 MΩ V_{CANH} = V_{CANL} = 5 V	−5.0	0	+5.0	μA
		V_{CC} = V_{IO} = 0 V V_{CANH} = V_{CANL} = 5 V	−5.0	0	+5.0	μA
$V_{i(rec)(diff)\_NM}$	Differential input voltage range recessive state	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	−3.0	–	0.5	V
$V_{i(dom)(diff)\_NM}$	Differential input voltage range dominant state	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	0.9	–	8.0	V
$V_{i(th)(diff)\_NM}$	Differential receiver threshold voltage voltage	Normal or Silent mode; −12 V ≤ V_{CANH}, V_{CANL} ≤ +12 V; no load	0.5	–	0.9	V
$V_{i(th)(diff)\_NM\_E}$		Normal or Silent mode; extended, −30 V ≤ V_{CANH}, V_{CANL} ≤ +35 V; no load	0.4	–	1.0	V
$R_{i(cm)}$	Common−mode input resistance at pins CANH and CANL	−2 V ≤ V_{CANH}, V_{CANL} ≤ +7 V	15	25	37	kΩ

Table 5. ELECTRICAL CHARACTERISTICS (V_{CC} = 4.75 V to 5.25 V; V_{IO} = 2.8 V to 5.5 V; for typical values T_A = 25°C, for min/max values T_J = −40 to +150°C; R_{LT} = 60 Ω, C_{RxD} = 15 pF; unless otherwise noted. All voltages are referenced to GND (pin 2). Positive currents flow into the respective pin)

$R_{i(cm)(m)}$	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL}$ = + 5 V	−1	0	+1	%
$R_{i(diff)}$	Differential input resistance	$R_{i(diff)} = R_{i(cm)(CANH)} + R_{i(cm)(CANL)}$ −2 V ≤ V_{CANH}, V_{CANL} ≤ +7 V	25	50	75	kΩ
C_i	Input capacitance at pins CANH and CANL	V_{TxD} = High; (Note 12)	–	7.5	20	pF
$C_{i(diff)}$	Differential input capacitance	V_{TxD} = High; (Note 12)	–	3.75	10	pF
TIMING CHARACTERISTICS (see Figure 5, Figure 6 and Figure 8)						
$t_{d(TxD-BUSon)}$	Propagation delay TxD to bus active	Normal mode (Note 13)	–	75	–	ns
$t_{d(TxD-BUSoff)}$	Propagation delay TxD to bus inactive	Normal mode (Note 13)	–	85	–	ns
$t_{d(BUSon-RxD)}$	Propagation delay bus active to RxD	Normal or Silent mode (Note 13)	–	24	–	ns
$t_{d(BUSoff-RxD)}$	Propagation delay bus inactive to RxD	Normal or Silent mode (Note 13)	–	32	–	ns
t_{pd_dr}	Propagation delay TxD to RxD dominant to recessive transition	Normal mode (Note 13)	50	100	210	ns
t_{pd_rd}	Propagation delay TxD to RxD recessive to dominant transition	Normal mode (Note 13)	50	120	210	ns
$t_{d(s-nm)}$	Operating mode change delay	Silent mode to Normal mode	5.0	11	50	μs
$t_{dom(TxD)}$	TxD dominant timeout	Normal mode; V_{TxD} = Low	1.0	–	10	ms
$t_{bit(RxD)}$	Bit time on RxD pin	$t_{bit(TxD)}$ = 500 ns (Note 13)	400	–	550	ns
		$t_{bit(TxD)}$ = 200 ns (Note 13)	120	–	220	ns
$t_{bit(Vi(diff))}$	Bit time on bus (CANH − CANL pin)	$t_{bit(TxD)}$ = 500 ns (Note 13)	435	–	530	ns
		$t_{bit(TxD)}$ = 200 ns (Note 13)	155	–	210	ns
Δt_{rec}	Receiver timing symmetry $\Delta t_{rec} = t_{bit(RxD)} - t_{bit(Vi(diff))}$	$t_{bit(TxD)}$ = 500 ns (Note 13)	−65	–	40	ns
		$t_{bit(TxD)}$ = 200 ns (Note 13)	−45	–	15	ns
THERMAL SHUTDOWN						
$T_{J(sd)}$	Shutdown junction temperature	Junction temperature rising	160	180	200	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. In the range between V_{UVDVCC} and 4.75 V and from 5.25 V to 6 V the chip is fully functional; some parameters may be outside of the specification
12. Values based on design and characterization, not tested in production
13. C_{LT} = 100 pF, C_{ST} not present, C_{RxD} = 15 pF

MEASUREMENTS SETUPS AND DEFINITIONS

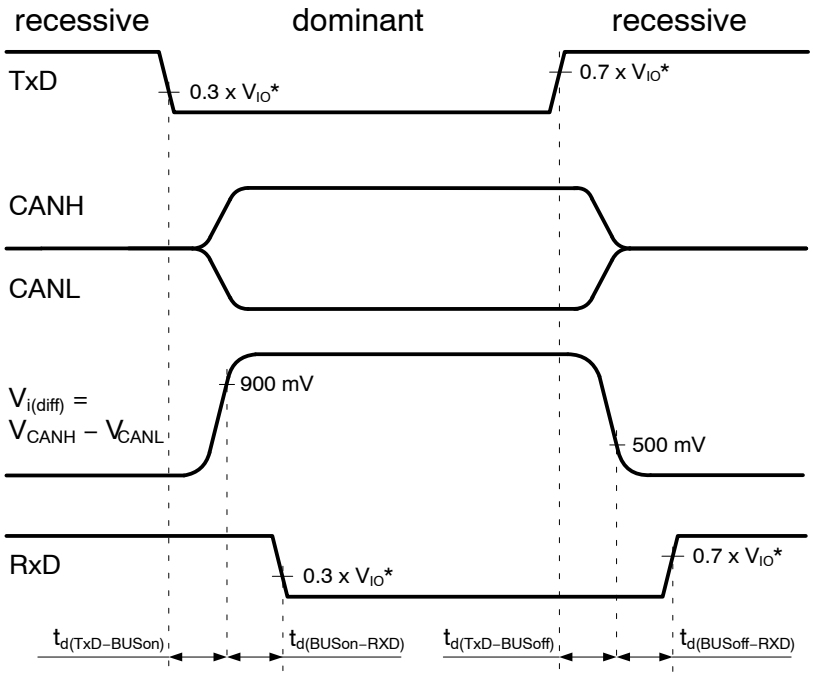


Figure 5. Transceiver Timing Diagram − Propagation Delays

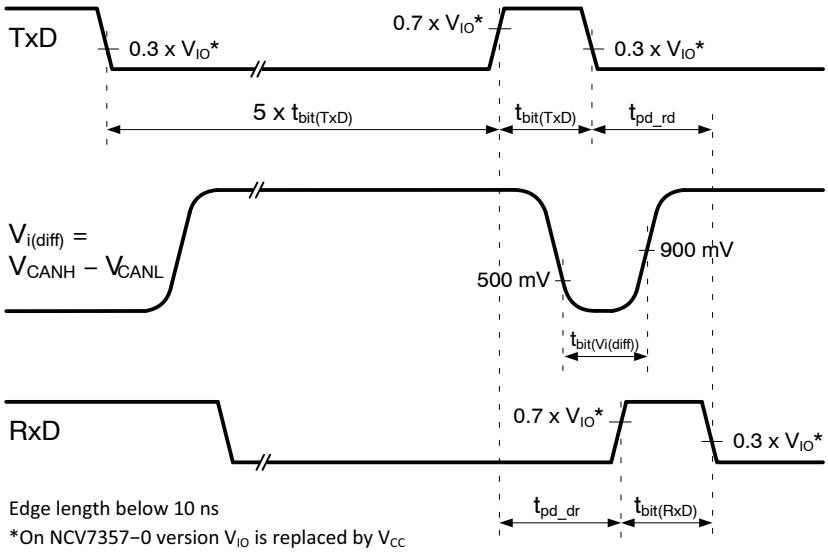


Figure 6. Transceiver Timing Diagram − Loop Delay and Recessive Bit Time

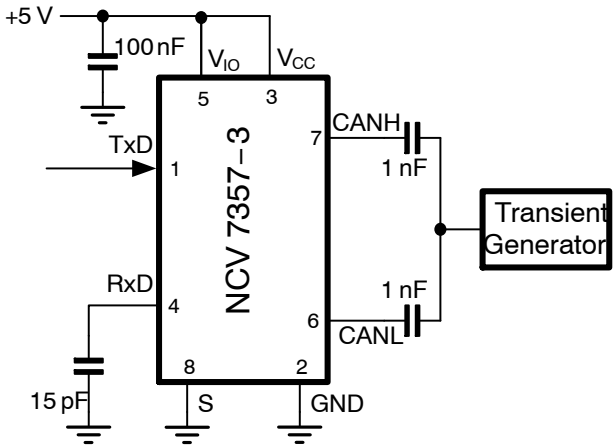


Figure 7. Test Circuit for Automotive Transients

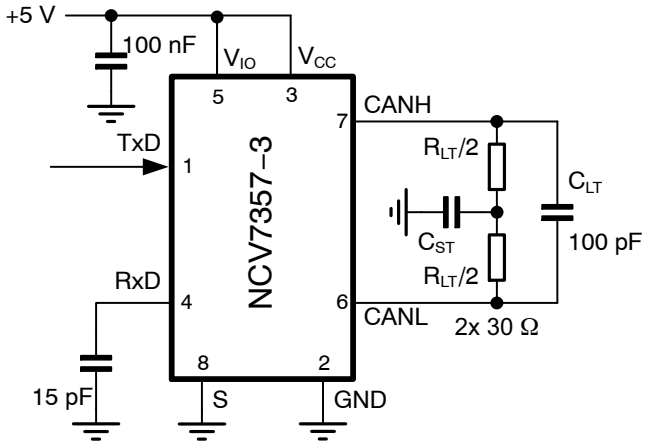


Figure 8. Test Circuit for Timing Characteristics

Table 6. ISO 11898−2:2016 Parameter Cross−Reference Table

ISO 11898−2:2016 Specification		NCV7357 Datasheet
Parameter	**Notation**	**Symbol**
DOMINANT OUTPUT CHARACTERISTICS		
Single ended voltage on CAN_H	V_{CAN_H}	$V_{o(dom)(CANH)}$
Single ended voltage on CAN_L	V_{CAN_L}	$V_{o(dom)(CANL)}$
Differential voltage on normal bus load	V_{Diff}	$V_{o(dom)(diff)}$
Differential voltage on effective resistance during arbitration	V_{Diff}	$V_{o(dom)(diff)\_ARB}$
Differential voltage on extended bus load range (optional)	V_{Diff}	$V_{o(dom)(diff)}$
DRIVER SYMMETRY		
Driver symmetry	V_{SYM}	$V_{o(dom)(sym)}$
DRIVER OUTPUT CURRENT		
Absolute current on CAN_H	I_{CAN_H}	$I_{o(SC)(CANH)}$
Absolute current on CAN_L	I_{CAN_L}	$I_{o(SC)(CANL)}$
RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING ACTIVE		
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{o(rec)}$
Single ended output voltage on CAN_L	V_{CAN_L}	$V_{o(rec)}$
Differential output voltage	V_{Diff}	$V_{o(rec)(diff)}$
RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING INACTIVE		
Single ended output voltage on CAN_H	V_{CAN_H}	NA
Single ended output voltage on CAN_L	V_{CAN_L}	NA
Differential output voltage	V_{Diff}	NA
OPTIONAL TRANSMIT DOMINANT TIMEOUT		
Transmit dominant timeout, long	t_{dom}	$t_{dom(TxD)}$
Transmit dominant timeout, short	t_{dom}	NA
STATIC RECEIVER INPUT CHARACTERISTICS, BUS BIASING ACTIVE/ INACTIVE		
Recessive state differential input voltage range	V_{Diff}	$V_{i(rec)(diff)\_NM}$
Dominant state differential input voltage range	V_{Diff}	$V_{i(dom)(diff)\_NM}$
RECEIVER INPUT RESISTANCE		
Differential internal resistance	R_{Diff}	$R_{i(diff)}$
Single ended internal resistance	R_{CAN_H} R_{CAN_L}	$R_{i(cm)}$ $R_{i(cm)}$
RECEIVER INPUT RESISTANCE MATCHING		
Matching a of internal resistance	m_R	$R_{i(cm)(m)}$
IMPLEMENTATION LOOP DELAY REQUIREMENT		
Loop delay	t_{Loop}	t_{pd_rd} t_{pd_dr}
OPTIONAL IMPLEMENTATION DATA SIGNAL TIMING REQUIREMENTS FOR USE WITH BIT RATES ABOVE 1 MBIT/S AND UP TO 2 MBIT/S		
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit(Bus)}$	$t_{bit(Vi(diff))}$
Received recessive bit width @ 2 Mbit/s	$t_{Bit(RXD)}$	$t_{bit(RxD)}$
Receiver timing symmetry @ 2 Mbit/s	Δt_{Rec}	Δt_{rec}
OPTIONAL IMPLEMENTATION DATA SIGNAL TIMING REQUIREMENTS FOR USE WITH BIT RATES ABOVE 2 MBIT/S AND UP TO 5 MBIT/S		
Transmitted recessive bit width @ 5 Mbit/s	$t_{Bit(Bus)}$	$t_{bit(Vi(diff))}$
Transmitted recessive bit width @ 5 Mbit / s	$t_{Bit(RXD)}$	$t_{bit(RxD)}$

Received recessive bit width @ 5 Mbit / s	Δt_{Rec}	Δt_{rec}

MAXIMUM RATINGS OF V_{CAN_H}, V_{CAN_L} AND V_{DIFF}

Maximum rating V_{Diff}	V_{Diff}	$V_{CANH - CANL}$
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	V_{CANH} V_{CANL}
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H} V_{CAN_L}	NA

MAXIMUM LEAKAGE CURRENTS ON CAN_H AND CAN_L, UNPOWERED

Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	$I_{LEAK(off)}$

BUS BIASING CONTROL TIMINGS

CAN activity filter time, long	t_{Filter}	NA
CAN activity filter time, short	t_{Filter}	NA
Wake−up timeout, short	t_{Wake}	NA
Wake−up timeout, long	t_{Wake}	NA
Timeout for bus inactivity (Required for selective wake−up implementation only)	$t_{Silence}$	NA
Bus Bias reaction time (Required for selective wake−up implementation only)	t_{Bias}	NA

Table 7. ORDERING INFORMATION

Part Number	Description	Temperature Range	Package	Shipping
NCV7357D10R2G	High Speed CAN FD Transceiver	−40°C to +150°C	SOIC 150 8 GREEN (Matte Sn, JEDEC MS−012) (Pb−Free)	3000 / Tape & Reel
NCV7357D13R2G	High Speed CAN FD Transceiver with V_{IO} pin			3000 / Tape & Reel
NCV7357MW0R2G	High Speed CAN FD Transceiver	−40°C to +150°C	DFNW8 Wettable Flank (Pb−Free)	3000 / Tape & Reel
NCV7357MW3R2G	High Speed CAN FD Transceiver with V_{IO} pin			3000 / Tape & Reel

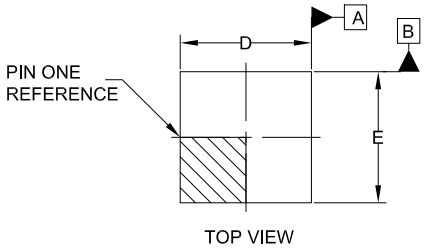
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

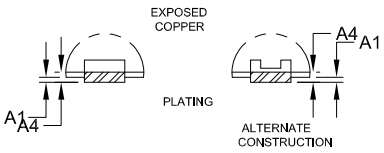
SCALE 2:1

DFNW8 3x3, 0.65P
CASE 507AB
ISSUE E

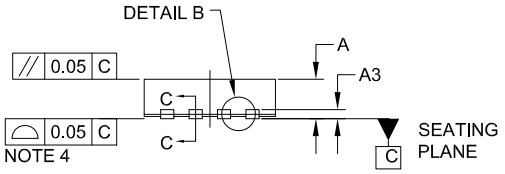
DATE 02 JUL 2021



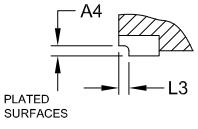
TOP VIEW



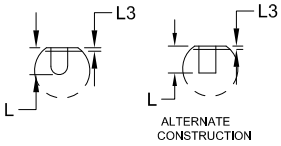
DETAIL B



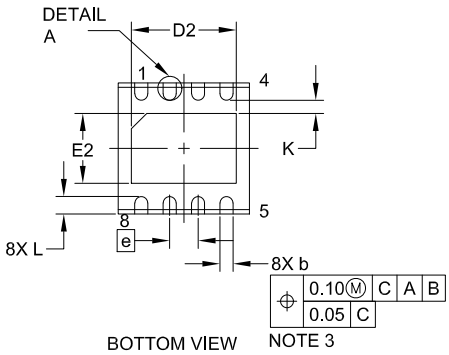
SIDE VIEW



SECTION C-C



DETAIL A



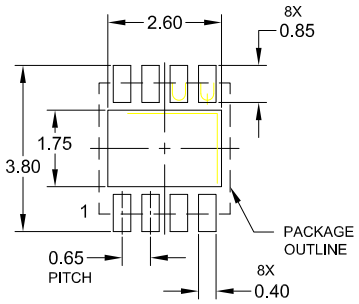
BOTTOM VIEW

NOTE 3

NOTES:

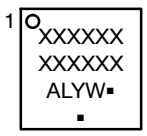
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	—	---	0.05
A3		0.20 REF	
A4	0.10	---	—
b	0.25	0.30	0.35
D	2.95	3.00	3.05
D2	2.30	2.40	2.50
E	2.95	3.00	3.05
E2	1.50	1.60	1.70
e		0.65 BSC	
K		0.30 REF	
L	0.35	0.40	0.45
L3	0.00	0.05	0.10



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

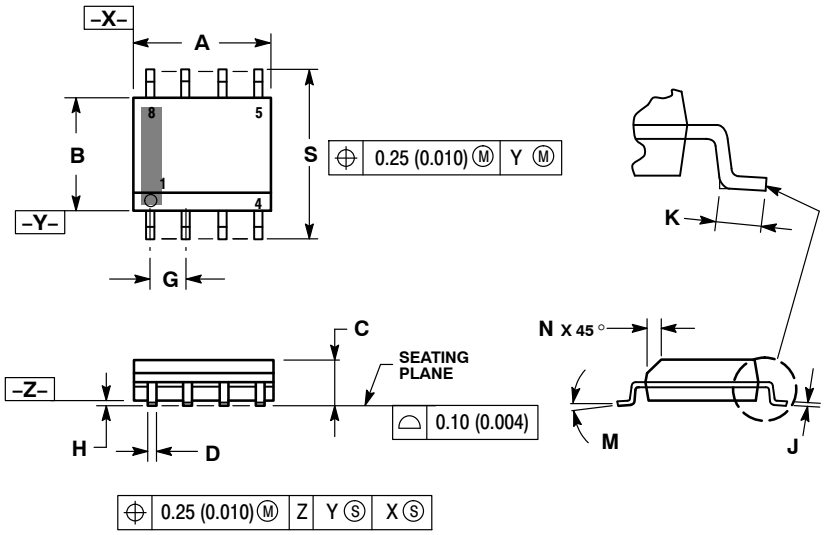
DOCUMENT NUMBER:	**98AON14978G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DFNW8 3x3, 0.65P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

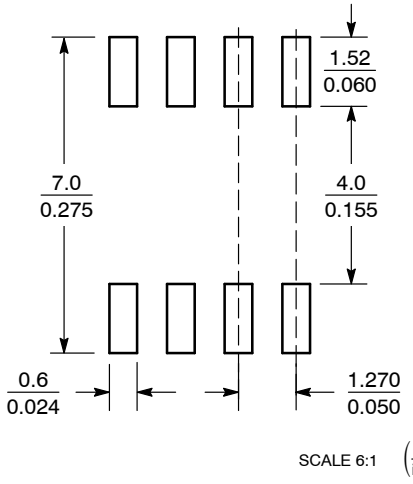
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

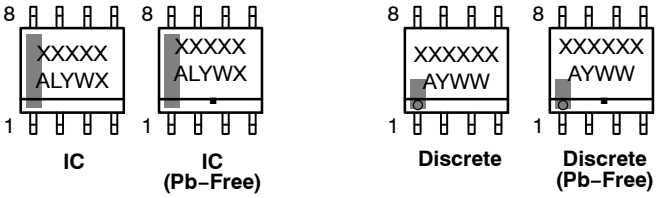
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

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