EDO DRAM

MT4C1M16E5 – 1 Meg x 16, 5V
MT4LC1M16E5 – 1 Meg x 16, 3.3V

For the latest data sheet, please refer to the Micron Web site: www.micron.com/products/datasheets/sdramds.html

FEATURES

- JEDEC- and industry-standard x16 timing, functions, pinouts, and packages
- High-performance CMOS silicon-gate process
- Single power supply (+3.3V ±0.3V or 5V ±10%)
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR), HIDDEN; optional self refresh (S)
- BYTE WRITE access cycles
- 1,024-cycle refresh (10 row, 10 column addresses)
- Extended Data-Out (EDO) PAGE MODE access
- 5V-tolerant inputs and I/Os on 3.3V devices

OPTIONS / MARKING

- Voltages[1]
  - 3.3V — LC
  - 5V — C
- Refresh Addressing
  - 1,024 (1K) rows — E5
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- Timing
  - 50ns access — -5
  - 60ns access — -6
- Refresh Rates
  - Standard Refresh (16ms period) — None
  - Self Refresh (128ms period) — S[2]
- Operating Temperature Range
  - Commercial (0°C to +70°C) — None
  - Extended (-20°C to +80°C) — ET

Part Number Example:
MT4LC1M16E5TG-6

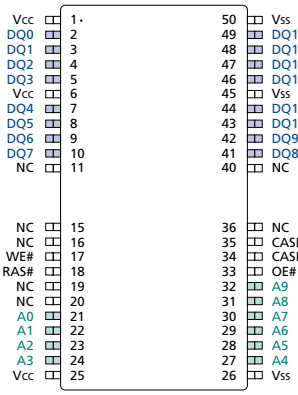
NOTE: 1. The third field distinguishes the low voltage offering: LC designates Vcc = 3.3V and C designates Vcc = 5V.
2. Available only on MT4LC1M16E5 (3.3V)

KEY TIMING PARAMETERS

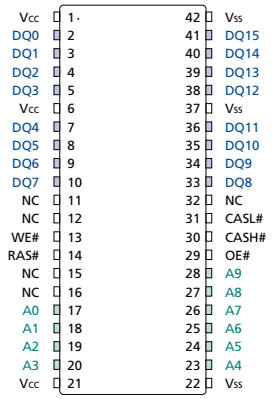
SPEED	tRC	tRAC	tPC	tAA	tCAC	tCAS
-5	84ns	50ns	20ns	25ns	15ns	8ns
-6	104ns	60ns	25ns	30ns	17ns	10ns

PIN ASSIGNMENT (Top View)

44/50-Pin TSOP



42-Pin SOJ



NOTE: The "#" symbol indicates signal is active LOW.

1 MEG x 16 EDO DRAM PART NUMBERS

PART NUMBER	Vcc	REFRESH	PACKAGE	REFRESH
MT4LC1M16E5DJ-x	3.3V	1K	400-SOJ	Standard
MT4LC1M16E5DJ-xS	3.3V	1K	400-SOJ	Self
MT4LC1M16E5TG-x	3.3V	1K	400-TSOP	Standard
MT4LC1M16E5TG-xS	3.3V	1K	400-TSOP	Self
MT4C1M16E5DJ-x	5V	1K	400-SOJ	Standard
MT4C1M16E5TG-x	5V	1K	400-TSOP	Standard

NOTE: "-x" indicates speed grade marking under timing options.

GENERAL DESCRIPTION

The 1 Meg x 16 is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x16 configuration. The 1 Meg x 16 has both BYTE WRITE and WORD WRITE access cycles via two CAS# pins (CASL# and CASH#). These function like a single CAS# found on other DRAMs in that either CASL# or CASH# will generate an internal CAS#.

The CAS# function and timing are determined by the first CAS# (CASL# or CASH#) to transition LOW and the last CAS# to transition back HIGH. Using only one

GENERAL DESCRIPTION (continued)

of the two signals results in a BYTE WRITE cycle. CASL# transitioning LOW selects an access cycle for the lower byte (DQ0-DQ7), and CASH# transitioning LOW selects an access cycle for the upper byte (DQ8-DQ15).

Each bit is uniquely addressed through the 20 address bits during READ or WRITE cycles. These are entered 10 bits (A0-A9) at a time. RAS# is used to latch the first 10 bits and CAS#, the latter 10 bits. The CAS# function also determines whether the cycle will be a refresh cycle (RAS# ONLY) or an active cycle (READ, WRITE or READ-WRITE) once RAS# goes LOW.

The CASL# and CASH# inputs internally generate a CAS# signal that functions like the single CAS# input on other DRAMs. The key difference is each CAS# input (CASL# and CASH#) controls its corresponding eight DQ inputs during WRITE accesses. CASL# controls DQ0-DQ7, and CASH# controls DQ8-DQ15. The two CAS# controls give the 1 Meg x 16 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS# (CASL# or CASH#), whichever occurs last. An EARLY WRITE occurs when WE is taken LOW prior to either CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE falls after CAS# (CASL# or CASH#) was taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z, regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O. Pin direction is controlled by OE# and WE#.

The 1 Meg x 16 DRAM must be refreshed periodically in order to retain stored data.

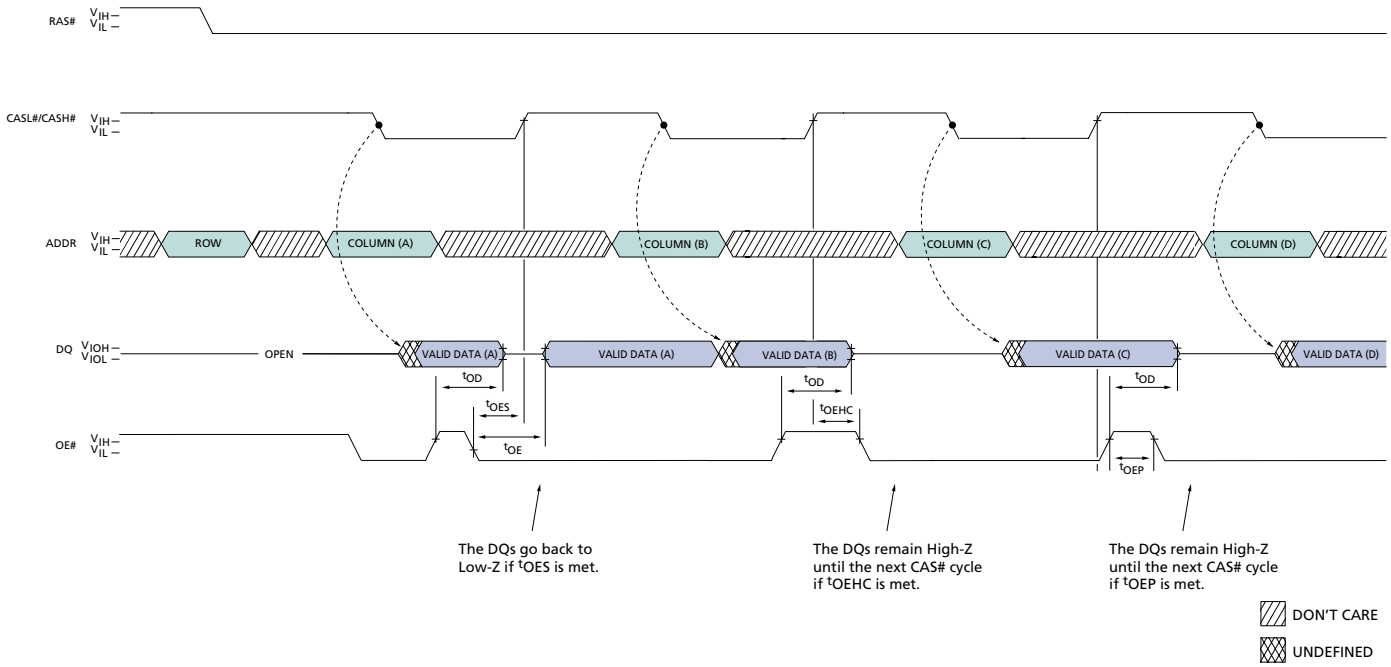


Figure 1
OE# Control of DQs

PAGE ACCESS

Page operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The page cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the page mode of operation, i.e., closes the page.

EDO PAGE MODE

The 1 Meg x 16 provides EDO PAGE MODE, which is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# returns HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z (refer to Figure 1). WE# can also perform the function of disabling the output drivers under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last.

BYTE ACCESS CYCLE

The BYTE WRITEs and BYTE READs are determined by the use of CASL# and CASH#. Enabling CASL# selects a lower BYTE access (DQ0-DQ7). Enabling CASH# selects an upper BYTE access (DQ8-DQ15). Enabling both CASL# and CASH# selects a WORD WRITE cycle.

The 1 Meg x 16 may be viewed as two 1 Meg x 8 DRAMs that have common input controls, with the exception of the CAS# inputs. Figure 3 illustrates the BYTE WRITE and WORD WRITE cycles.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte are not allowed during the same cycle.

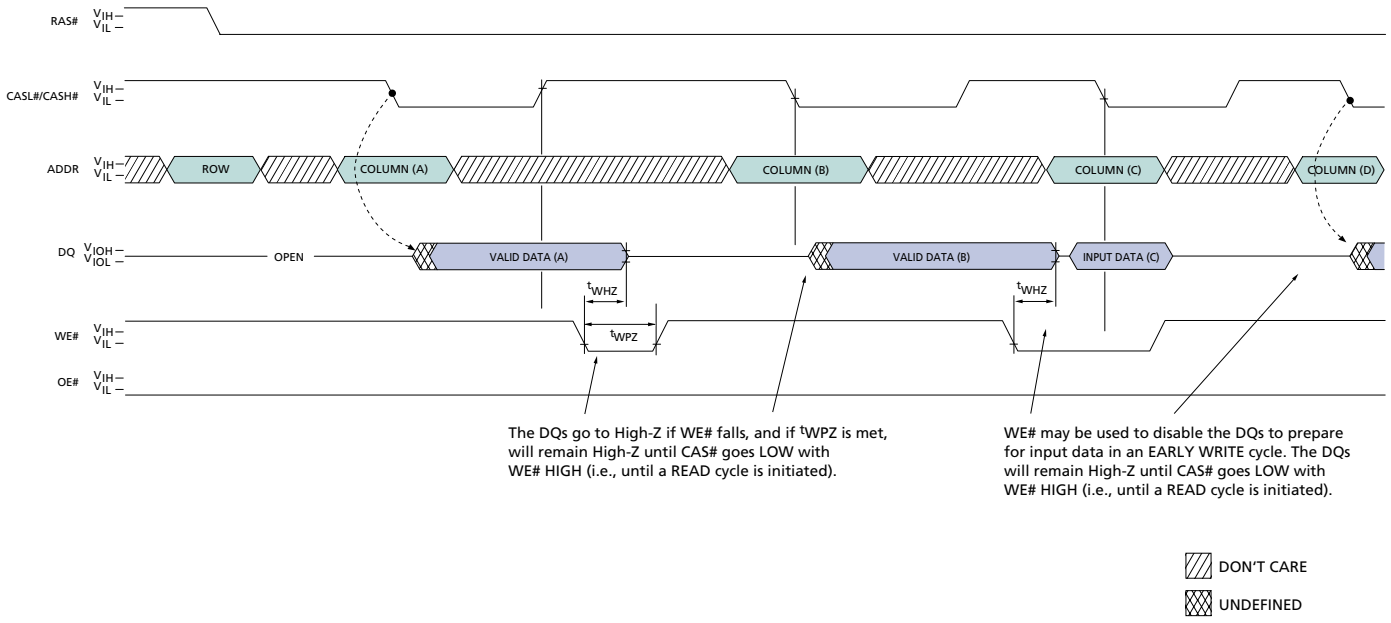


Figure 2
WE# Control of DQs

However, an EARLY WRITE on one byte and a LATE WRITE on the other byte, after a CAS# precharge has been satisfied, are permissible.

DRAM REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all 1,024 combinations of RAS# addresses are executed within ^{t}REF (MAX), regardless of sequence. The CBR, EXTENDED and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.

An optional self refresh mode is available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified ^{t}RASS. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms, or 125µs per row, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all 1,024 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

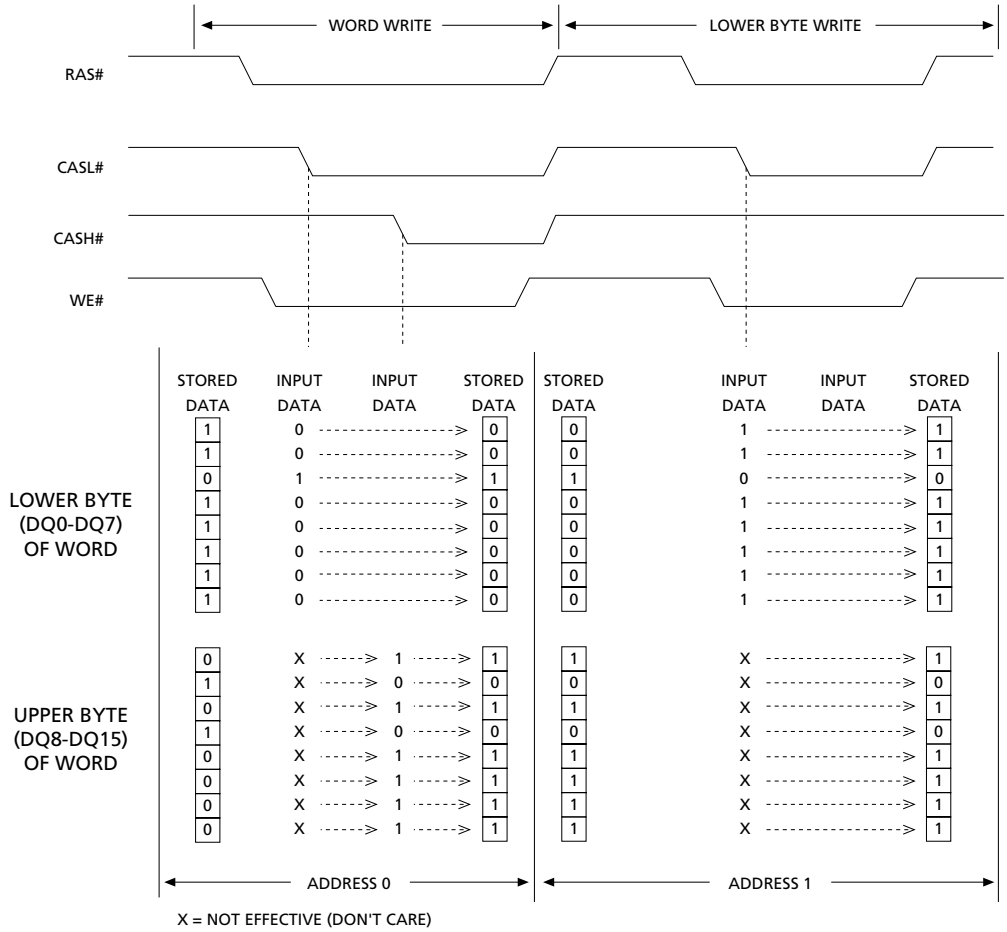
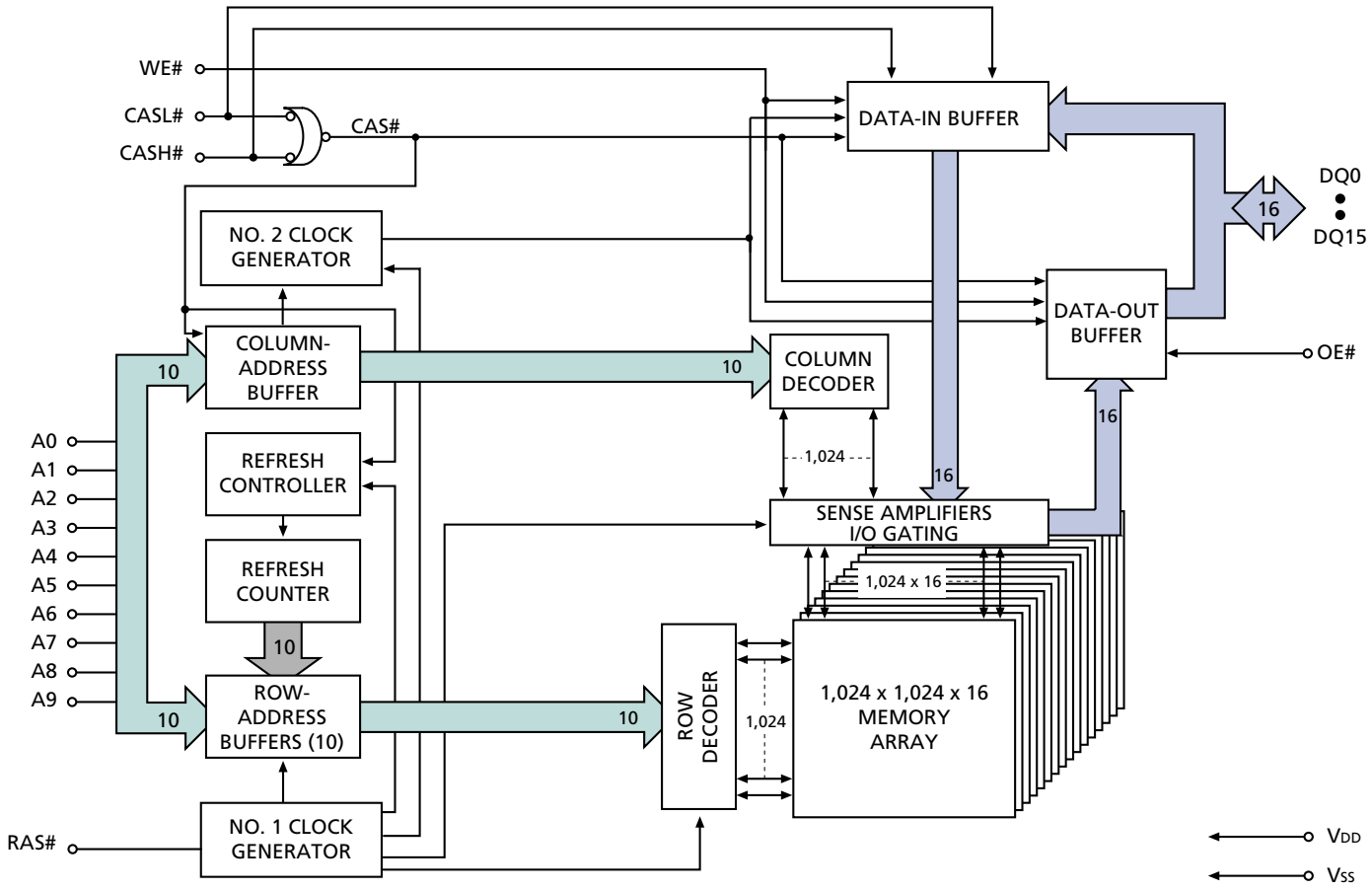


Figure 3
WORD and BYTE WRITE Example

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS}
- 3.3V ..... -1V to +4.6V
- 5V ..... -1V to +7V

Voltage on NC, Inputs or I/O Pins Relative to Vss:
- 3.3V ..... -1V to +5.5V
- 5V ..... -1V to +7V

Operating Temperature
- T_A (commercial) ..... 0°C to +70°C
- T_A (extended) ..... -20°C to +80°C

Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1; notes appear on pages 10-11)

PARAMETER/CONDITION	SYMBOL	3.3V		5V		UNITS	NOTES
		MIN	MAX	MIN	MAX		
SUPPLY VOLTAGE	V_{CC}	3.0	3.6	4.5	5.5	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V_{IH}	2.0	5.5	2.4	V_{CC} + 1	V	
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V_{IL}	-1.0	0.8	-0.5	0.8	V	
INPUT LEAKAGE CURRENT: Any input at V_{IN} ($0V \le V_{IN} \le V_{IH}$[MAX]); All other pins not under test = 0V	I_I	-2	2	-2	2	µA	4
OUTPUT HIGH VOLTAGE: I_{OUT} = -2mA(3.3V), -5mA(5V)	V_{OH}	2.4	–	2.4	–	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 2mA(3.3V), 4.2mA(5V)	V_{OL}	–	0.4	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V_{OUT} ($0V \le V_{OUT} \le 5.5V$); DQ is disabled and in High-Z state	I_{OZ}	-5	5	-5	5	µA	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 8; notes appear on pages 10-11); (V_{CC}[MIN] ≤ V_{CC} ≤ V_{CC}[MAX])

PARAMETER/CONDITION	SYMBOL	SPEED	3.3V	5V	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I_{CC1}	ALL	1	2	mA	
STANDBY CURRENT: CMOS (non-"S" version only) (RAS# = CAS# = other inputs = V_{DD} - 0.2V)	I_{CC2}	ALL	500	500	µA	
STANDBY CURRENT: CMOS ("S" version only) (RAS# = CAS# = other inputs = V_{DD} - 0.2V)	I_{CC2}	ALL	150	150	µA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC3}	-5 -6	180 170	190 180	mA	6
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{CC4}	-5 -6	140 130	150 140	mA	6
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{CC5}	-5 -6	180 170	190 180	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC6}	-5 -6	180 170	180 170	mA	7, 9
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^{t}RAS (MIN); WE# = V_{DD} - 0.2V; A0-A10, OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open); ^{t}RC = 125µs	I_{CC7}	ALL	300	300	µA	7, 9
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# ≥ $^{t}RASS$ (MIN) and CAS# held LOW; WE# = V_{DD} - 0.2V; A0-A10, OE# and D_{IN} = V_{DD} - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	ALL	300	300	µA	7, 9

CAPACITANCE

(Notes: 1, 2, 3, 5, 8; notes appear on pages 10-11)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Addresses	C_{I1}	5	pF	
Input Capacitance: RAS#, CASL#,CASH#, WE#, OE#	C_{I2}	7	pF	
Input/Output Capacitance: DQ	C_{IO}	7	pF	

AC ELECTRICAL CHARACTERISTICS

(Notes: 2, 3, 9, 10, 11, 12; notes appear on pages 10-11); (V_{CC}[MIN] ≤ V_{CC} ≤ V_{CC}[MAX])

AC CHARACTERISTICS		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		25		30	ns	
Column-address setup to CAS# precharge	^tACH	12		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		ns	
Column-address setup time	^tASC	0		0		ns	25
Row-address setup time	^tASR	0		0		ns	25
Column address to WE# delay time	^tAWD	42		49		ns	13
Access time from CAS#	^tCAC		13		15	ns	14, 25
Column-address hold time	^tCAH	8		10		ns	25
CAS# pulse width	^tCAS	8	10,000	10	10,000	ns	27
CAS# LOW to "Don't Care" during Self Refresh	^tCHD	15		15		ns	
CAS# hold time (CBR Refresh)	^tCHR	8		10		ns	7, 26
Last CAS# going LOW to first CAS# to return HIGH	^tCLCH	5		5		ns	28
CAS# to output in Low-Z	^tCLZ	0		0		ns	26
Data output hold after next CAS# LOW	^tCOH	3		3		ns	
CAS# precharge time	^tCP	8		10		ns	15, 30
Access time from CAS# precharge	^tCPA		28		35	ns	26
CAS# to RAS# precharge time	^tCRP	5		5		ns	26
CAS# hold time	^tCSH	38		45		ns	26
CAS# setup time (CBR Refresh)	^tCSR	5		5		ns	7, 25
CAS# to WE# delay time	^tCWD	28		35		ns	13, 25
WRITE command to CAS# lead time	^tCWL	8		10		ns	26
Data-in hold time	^tDH	8		10		ns	16, 25
Data-in setup time	^tDS	0		0		ns	16, 25
Output disable	^tOD	0	12	0	15	ns	
Output enable	^tOE		12		15	ns	17
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		ns	18
OE# HIGH hold from CAS# HIGH	^tOEHC	5		10		ns	18
OE# HIGH pulse width	^tOEP	5		5		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		ns	
Output buffer turn-off delay	^tOFF	0	12	0	15	ns	20, 26

AC ELECTRICAL CHARACTERISTICS (continued)

(Notes: 2, 3, 9, 10, 11, 12; notes appear on pages 10-11); (Vcc[MIN] ≤ Vcc ≤ Vcc[MAX])

AC CHARACTERISTICS		-5		-6			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
OE# setup prior to RAS# during HIDDEN REFRESH cycle	tORD	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	tPC	20		25		ns	31
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	47		56		ns	31
Access time from RAS#	tRAC		50		60	ns	19
RAS# to column-address delay time	tRAD	9		12		ns	21
Row address hold time	tRAH	9		10		ns	
RAS# pulse width	tRAS	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	tRASP	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	tRASS	100		100		µs	
Random READ or WRITE cycle time	tRC	84		104		ns	
RAS# to CAS# delay time	tRCD	11		14		ns	22, 25
READ command hold time (referenced to CAS#)	tRCH	0		0		ns	23, 27
READ command setup time	tRCS	0		0		ns	25
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (1,024 cycles) S version	tREF		128		128	ms	
RAS# precharge time	tRP	30		40		ns	
RAS# to CAS# precharge time	tRPC	5		5		ns	
RAS# precharge time exiting Self Refresh	tRPS	90		105		ns	
READ command hold time (referenced to RAS#)	tRRH	0		0		ns	23
RAS# hold time	tRSH	13		15		ns	32
READ-WRITE cycle time	tRWC	116		140		ns	
RAS# to WE# delay time	tRWD	67		79		ns	13
WRITE command to RAS# lead time	tRWL	13		15		ns	
Transition time (rise or fall)	tT	2	50	2	50	ns	
WRITE command hold time	tWCH	8		10		ns	32
WRITE command hold time (referenced to RAS#)	tWCR	38		45		ns	
WE# command setup time	tWCS	0		0		ns	13, 25
Output disable delay from WE#	tWHZ	0	12	0	15	ns	
WRITE command pulse width	tWP	5		5		ns	
WE# pulse to disable at CAS# HIGH	tWPZ	10		10		ns	
WE# hold time (CBR Refresh)	tWRH	8		10		ns	
WE# setup time (CBR Refresh)	tWRP	8		10		ns	

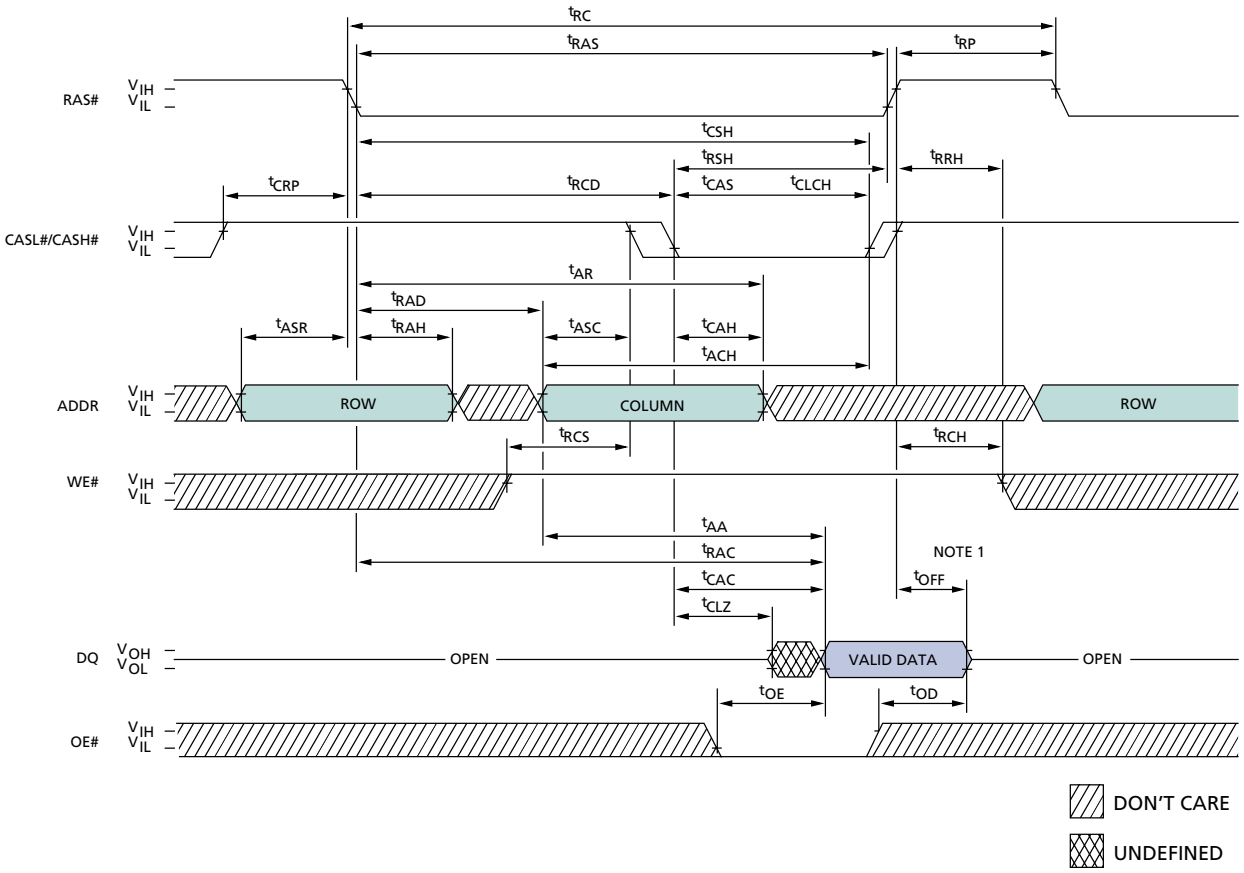
NOTES

1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^oC \le T_A \le 70^oC$ for commercial) and ($-20^oC \le T_A \le 80^oC$ for extended) is ensured.
3. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled. V_{DD} = +3.3V; f = 1 MHz.
9. AC characteristics assume ^tT = 2.5ns.
10. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
11. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates and 100pF; and V_{OL} = 0.8V and V_{OH} = 2V.
13. ^tWCS, ^tRWD, ^tAWD, and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tWCS < {}^tWCS$ (MIN) and $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
14. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^tCP.
16. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If OE# is tied permanently LOW, LATE WRITE, or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^tOEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
19. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of RAS# or CAS#, whichever occurs last.
21. The ^tRAD (MAX) limit is no longer specified. ^tRAD (MAX) was specified as a reference point only. If ^tRAD was greater than the specified ^tRAD (MAX) limit, then access time was controlled exclusively by ^tAA (^tRAC and ^tCAC no longer applied). With or without the ^tRAD (MAX) limit, ^tAA, ^tRAC, and ^tCAC must always be met.
22. The ^tRCD (MAX) limit is no longer specified. ^tRCD (MAX) was specified as a reference point only. If ^tRCD was greater than the specified ^tRCD (MAX) limit, then access time was controlled exclusively by ^tCAC (^tRAC [MIN] no longer applied). With or without the ^tRCD limit, ^tAA and ^tCAC must always be met.
23. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
24. The first CAS#x edge to transition LOW.
25. Output parameter (DQx) is referenced to corresponding CAS# input; DQ0-DQ7 by CASL# and DQ8-DQ15 by CASH#.

NOTES (continued)

26. Each CAS#x must meet minimum pulse width.
27. The last CAS#x edge to transition HIGH.
28. Last falling CAS#x edge to first rising CAS#x edge.
29. Last rising CAS#x edge to first falling CAS#x edge.
30. Last rising CAS#x edge to next cycle's last rising CAS#x edge.
31. Last CAS#x to go LOW.
32. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

READ CYCLE



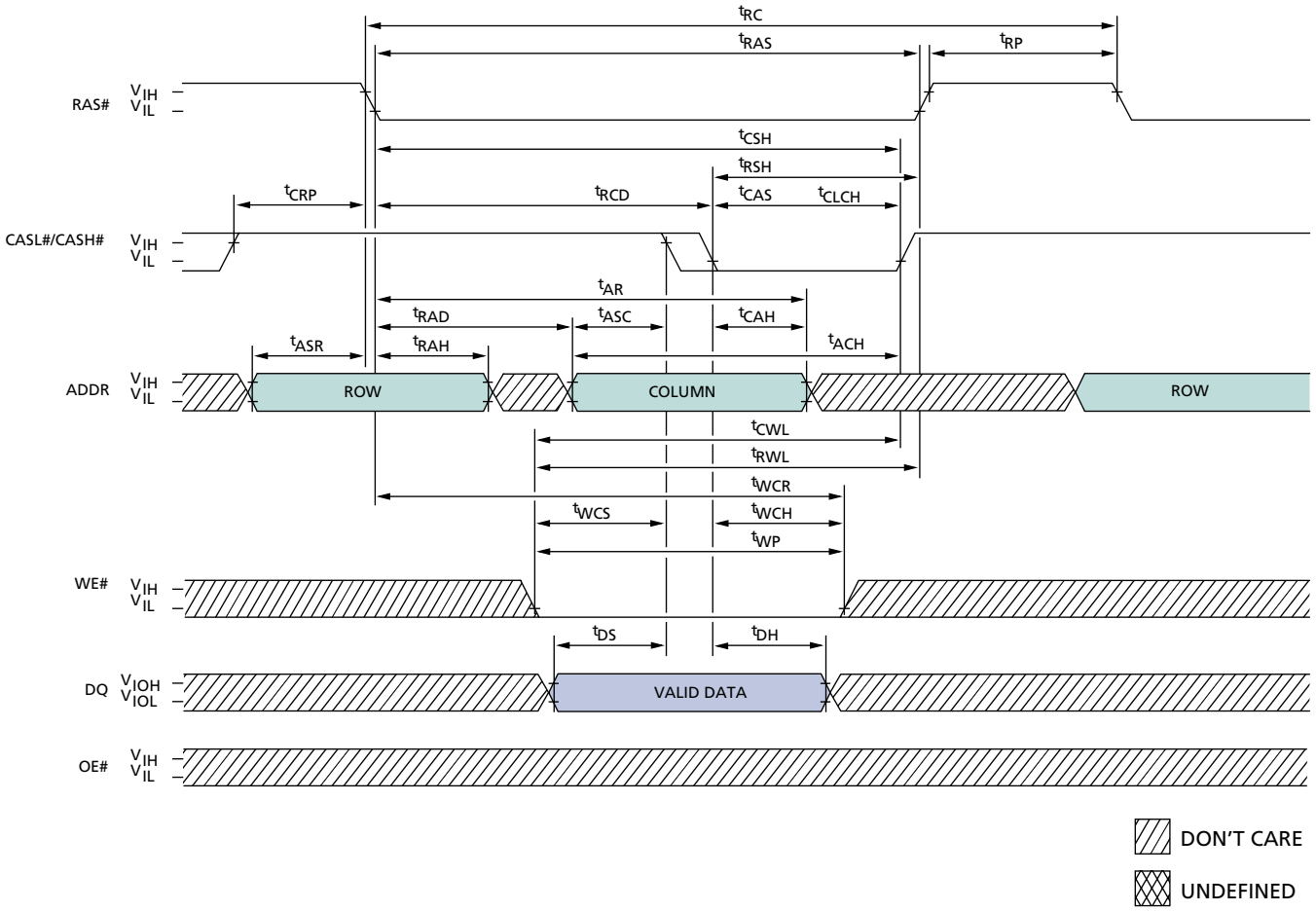
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

NOTE: 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE

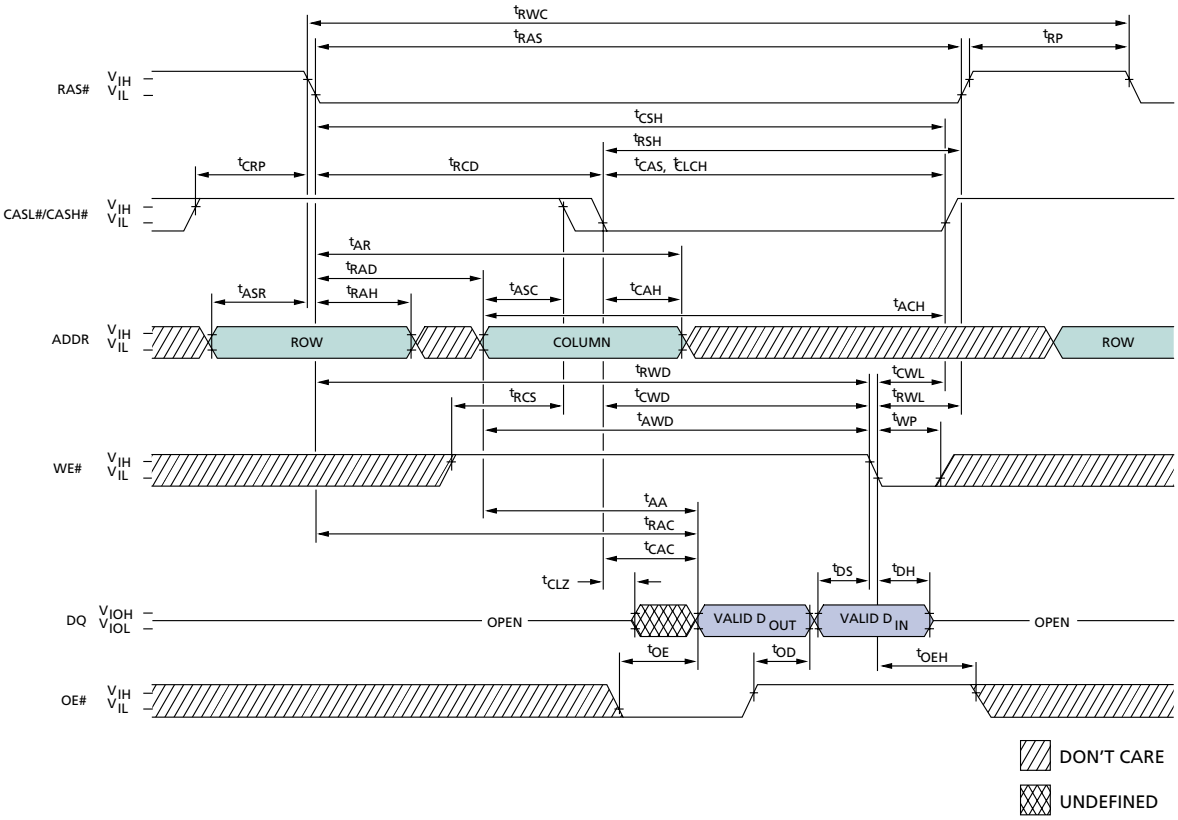


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

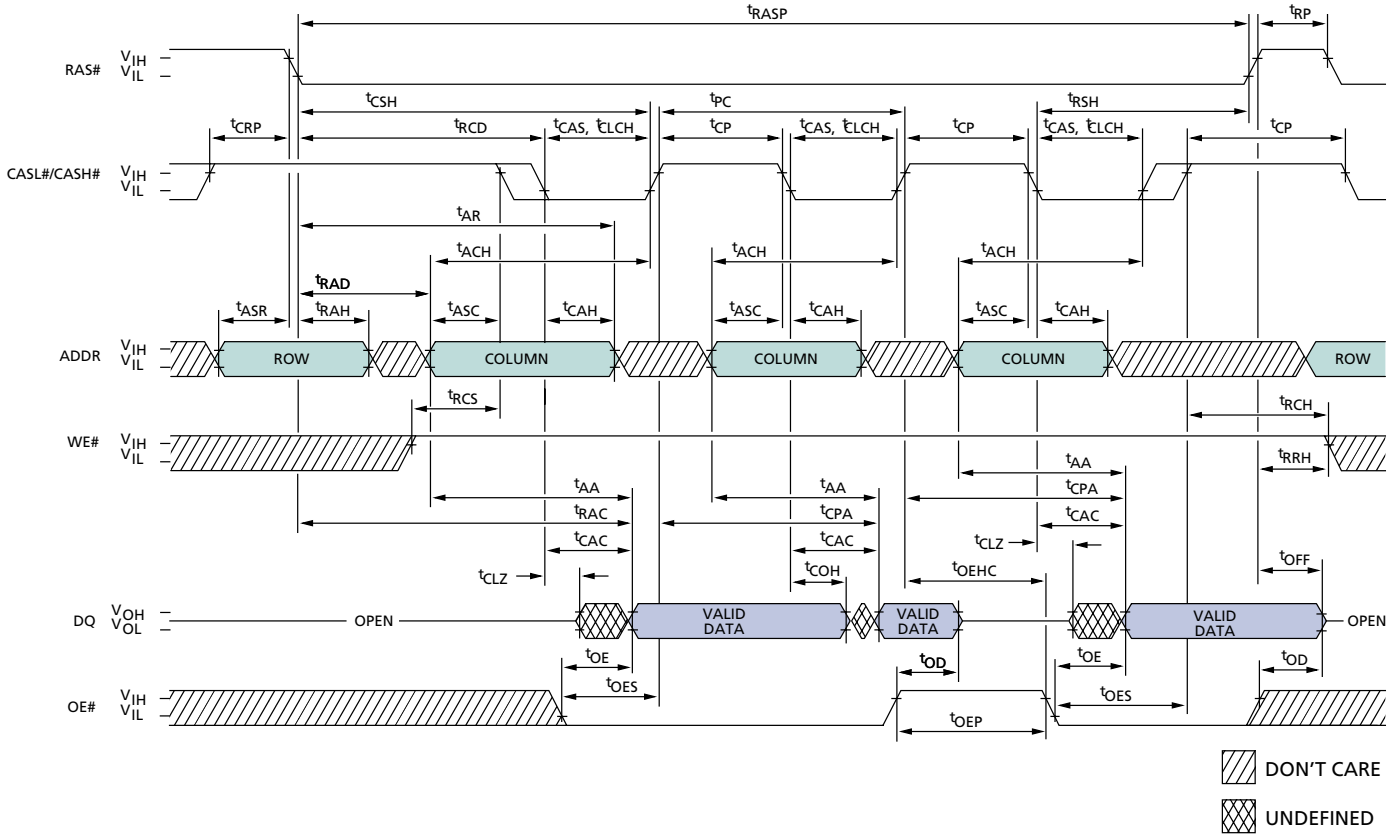


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tAWD	42		49		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWC	116		140		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

EDO-PAGE-MODE READ CYCLE

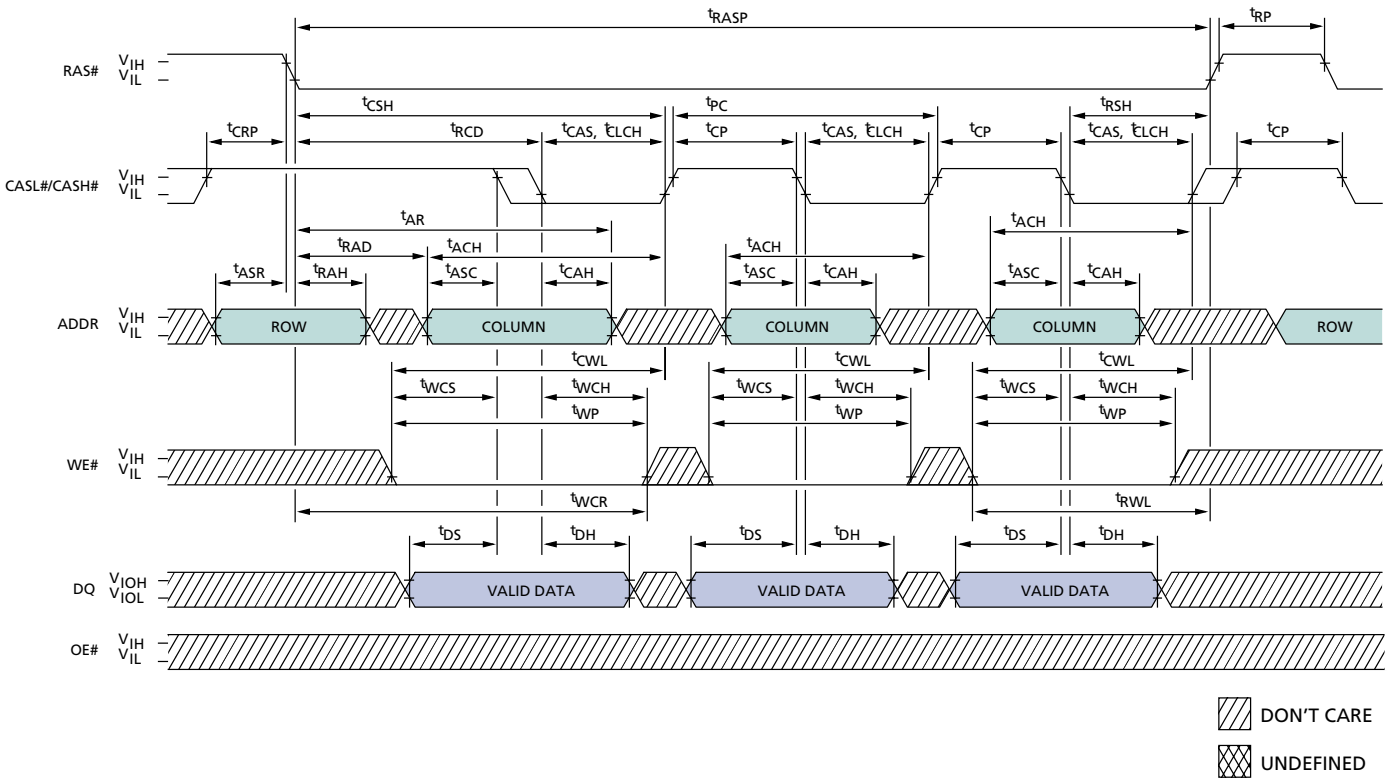


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		1ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EDO-PAGE-MODE EARLY WRITE CYCLE



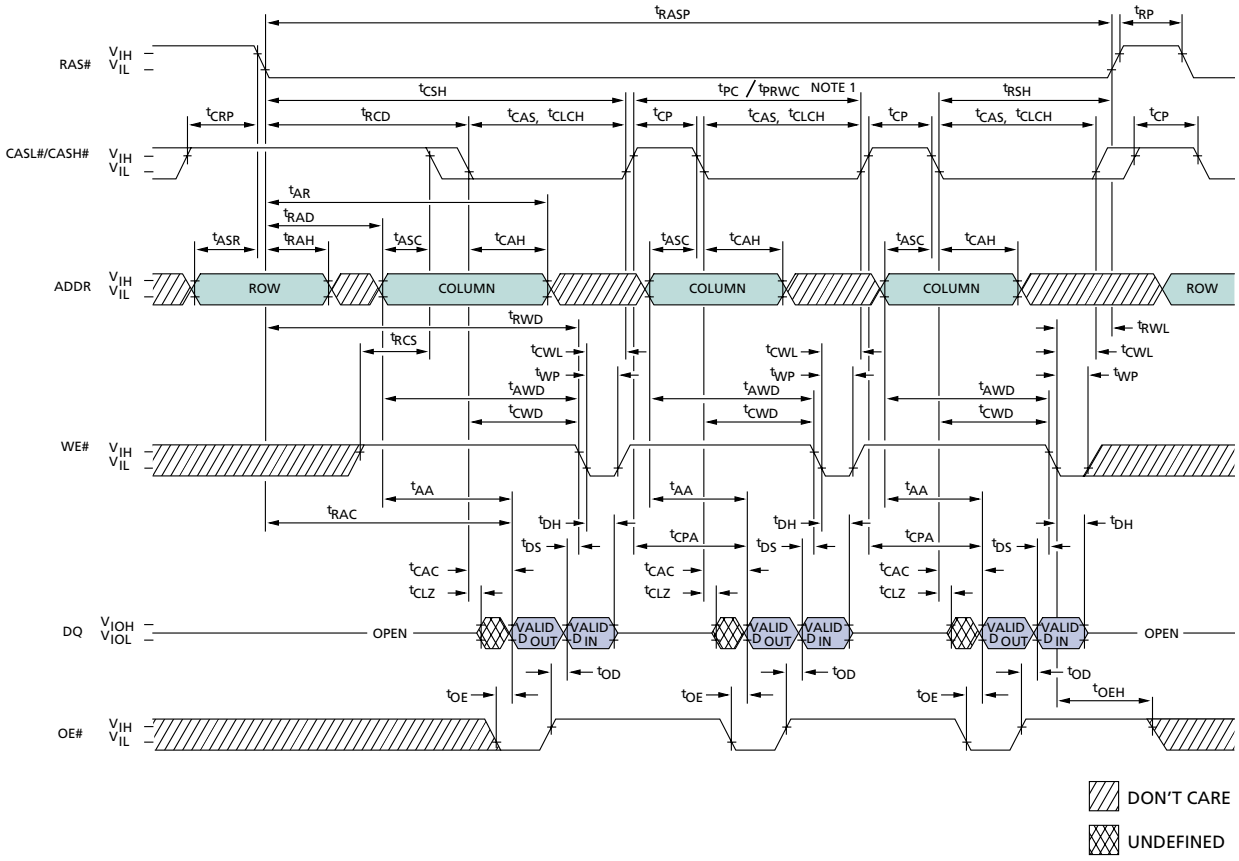
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tPC	20		25		ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	38		45		ns
tWCS	0		0		ns
tWP	5		5		ns

EDO-PAGE-MODE READ-WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)



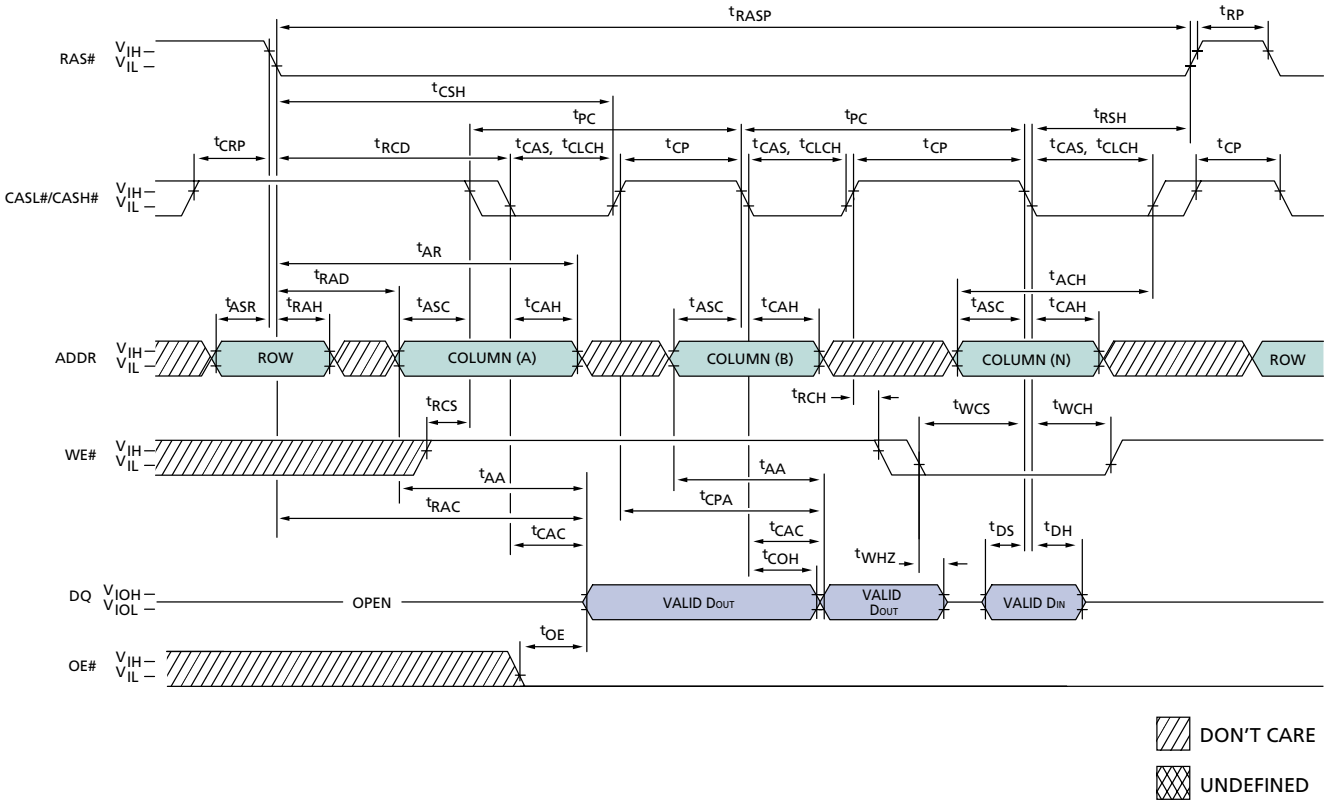
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tOD	0	12	0	15	ns
tOE		12		15	ns
tOEH	8		10		ns
tPC	20		25		ns
tPRWC	47		56		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

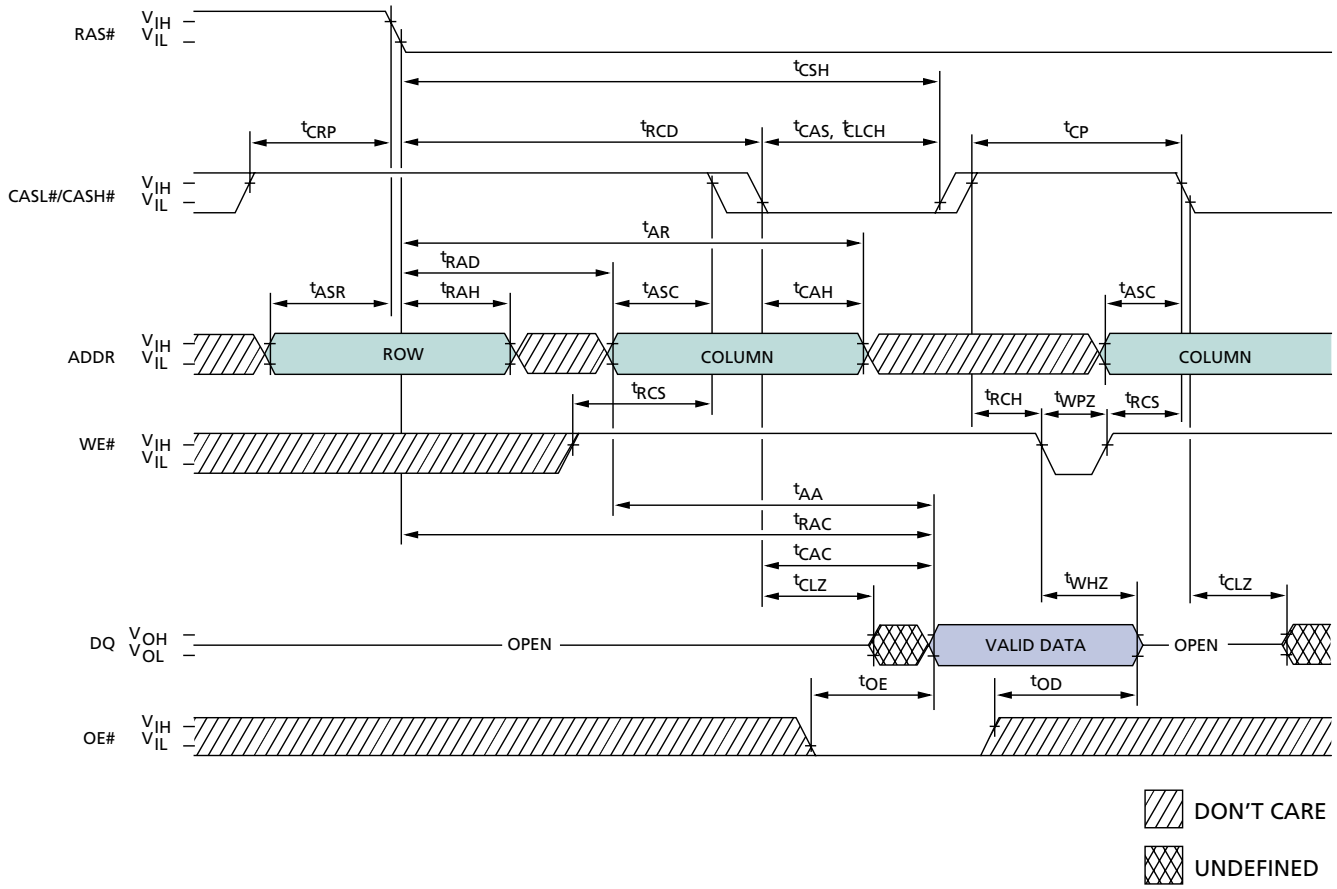


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tDS	0		0		ns
tOE		12		15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns

READ CYCLE
(with WE#-controlled disable)

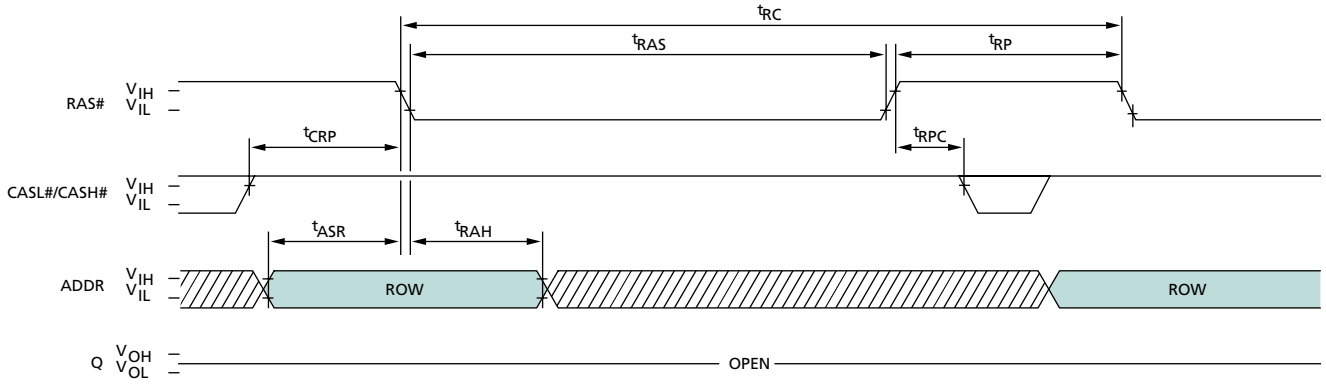


TIMING PARAMETERS

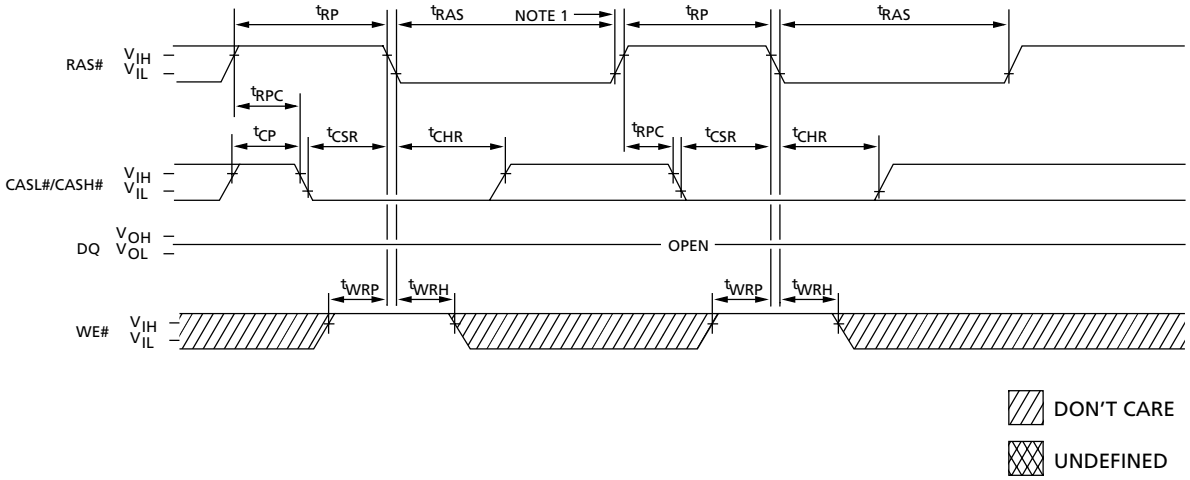
SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLCH	5		5		ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	12	0	15	ns
tWPZ	10		10		ns

RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



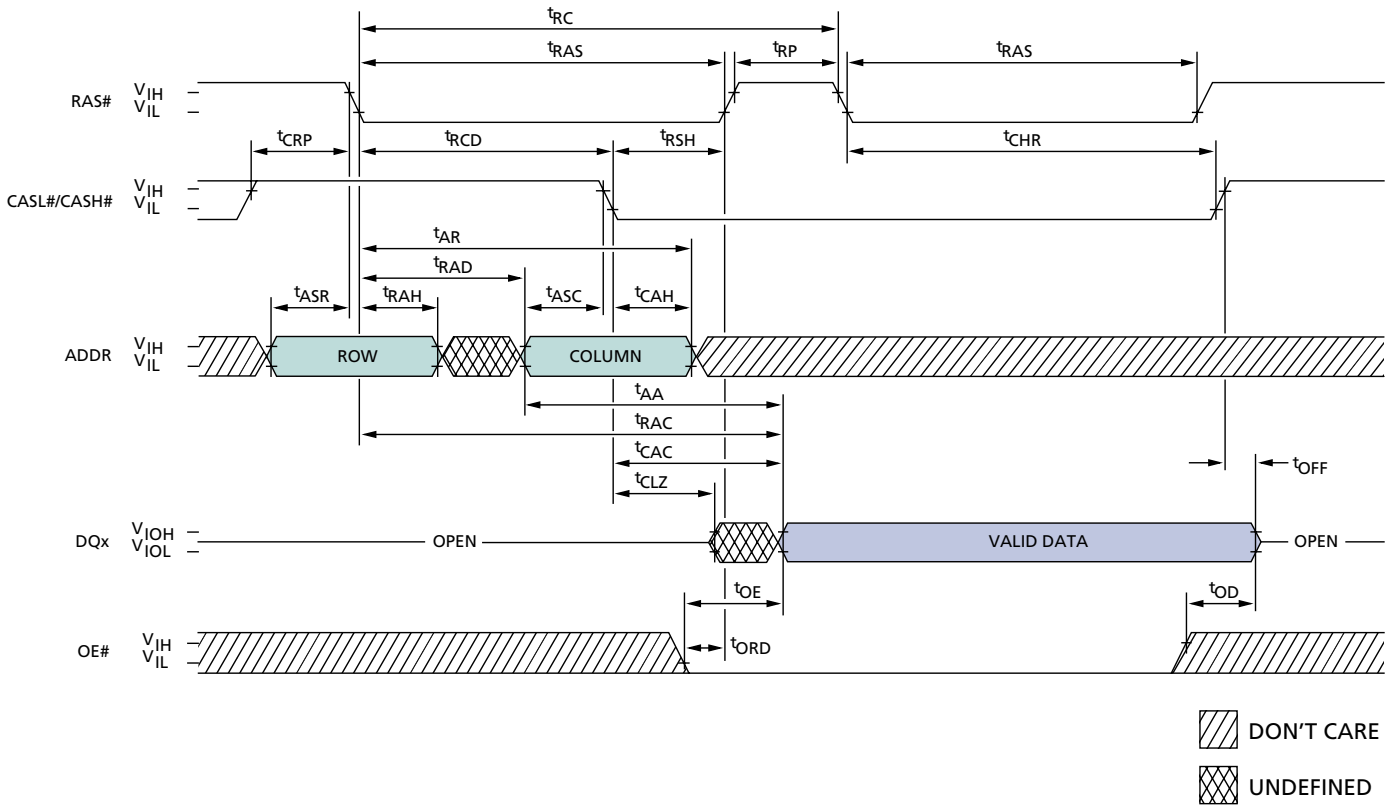
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tASR	0		0		ns
tCHR	8		10		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSR	5		5		ns
tRAH	9		10		ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRAS	50	10,000	60	10,000	ns
tRC	84		104		ns
tRP	30		40		ns
tRPC	5		5		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTE: 1. End of first CBR REFRESH cycle.

HIDDEN REFRESH CYCLE
(WE# = HIGH; OE# = LOW)

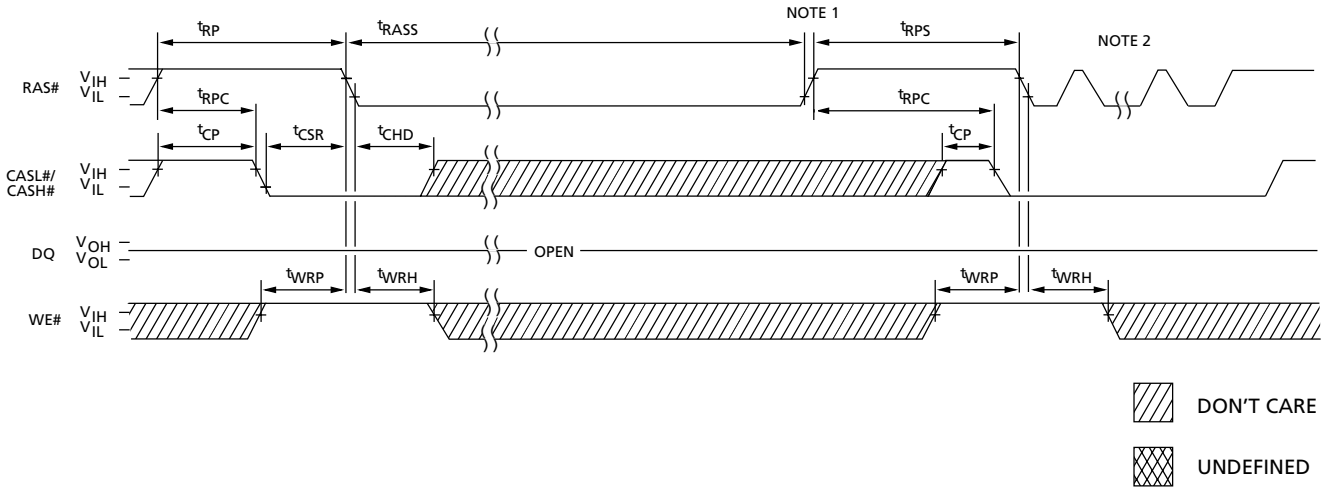


TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR	8		10		ns
tCLZ	0		0		ns
tCRP	5		5		ns
tOD	0	12	0	15	ns

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tOE		12		15	ns
tOFF	0	12	0	15	ns
tORD	0		0		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRAS	50	10,000	60	10,000	ns
tRCD	11		14		ns
tRP	30		40		ns
tRSH	13		15		ns

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



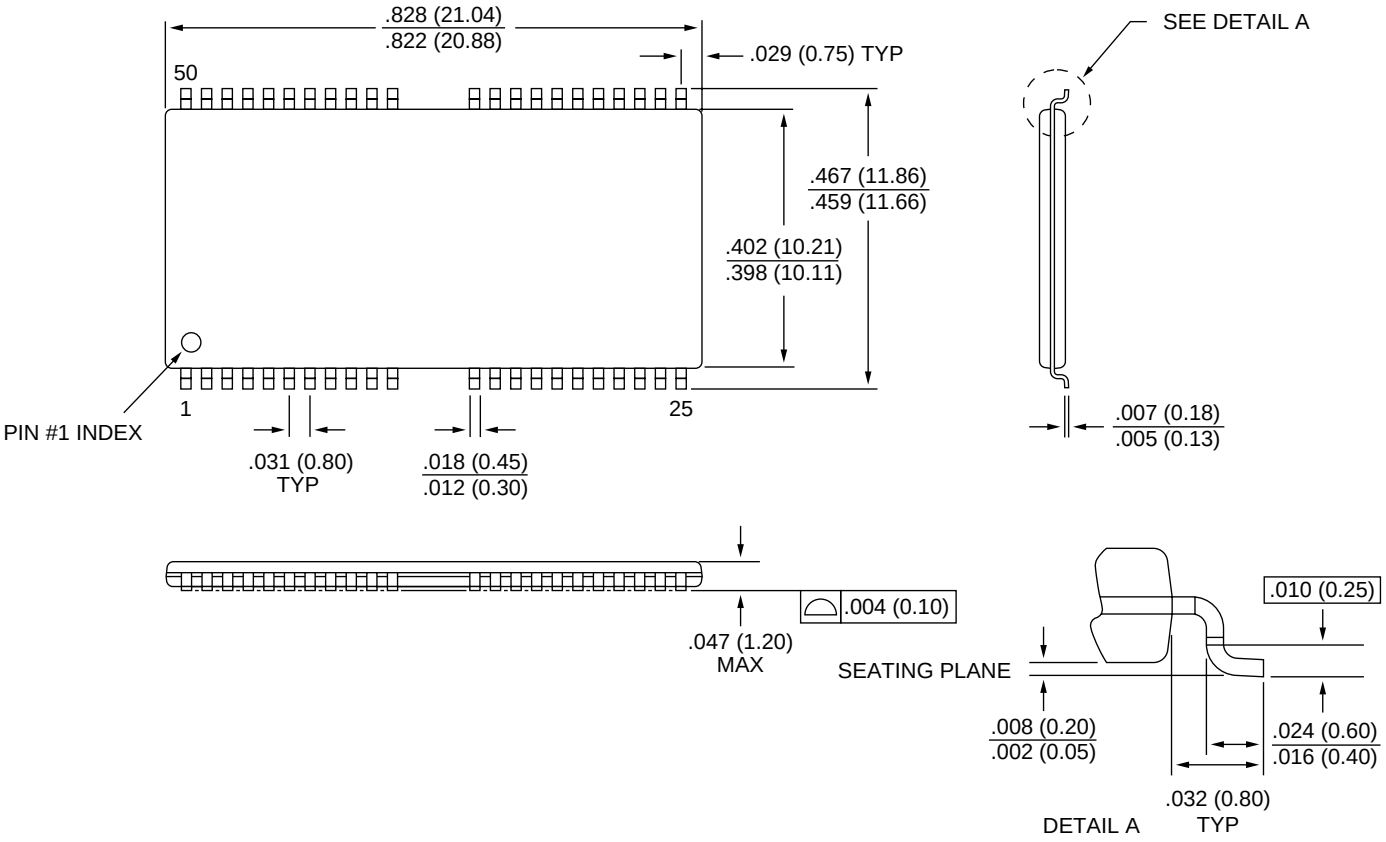
TIMING PARAMETERS

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tCHD	15		15		ns
tCLCH	5		5		ns
tCP	8		10		ns
tCSR	5		5		ns
tRASS	100		100		µs

SYMBOL	-5 MIN	-5 MAX	-6 MIN	-6 MAX	UNITS
tRP	30		40		ns
tRPC	5		5		ns
tRPS	90		105		ns
tWRH	8		10		ns
tWRP	8		10		ns

NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

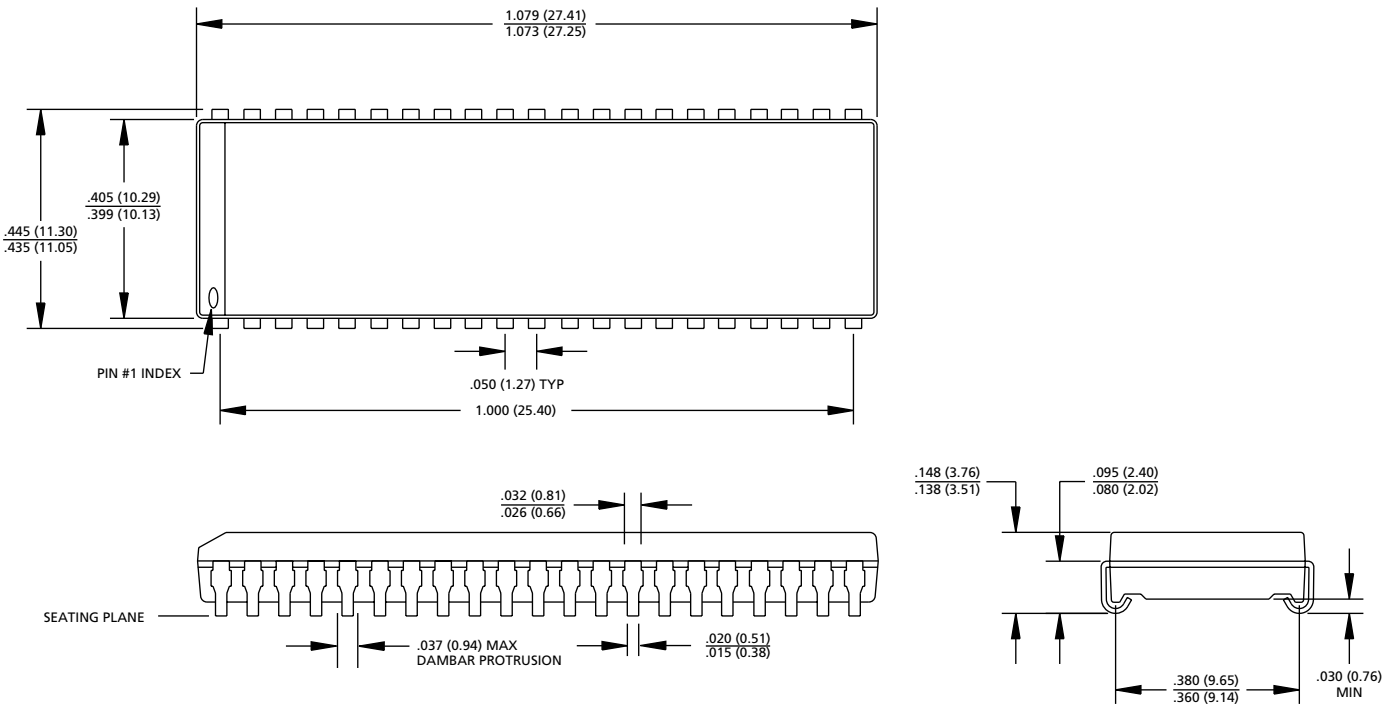
44/50-PIN PLASTIC TSOP (400 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

42-PIN PLASTIC SOJ (400 mil)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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