ZL40219

# Precision 1:8 LVDS Fanout Buffer with On-Chip Input Termination

Data Sheet

April 2014

## Features

### Inputs/Outputs

- Accepts differential or single-ended input
  - LVPECL, LVDS, CML, HCSL, LVCMOS
- On-chip input termination and biasing for AC coupled inputs
- Eight precision LVDS outputs
- Operating frequency up to 750 MHz

### Power

- Options for 2.5 V or 3.3 V power supply
- Current consumption of 112 mA
- On-chip Low Drop Out (LDO) Regulator for superior power supply rejection

### Performance

- Ultra low additive jitter of 135 fs RMS

**Ordering Information**

| | | |
|---|---|---|
| ZL40219LDG1 | 32 Pin QFN | Trays |
| ZL40219LDF1 | 32 Pin QFN | Tape and Reel |

Matte Tin
Package size: 5 x 5 mm

**-40°C to +85°C**

## Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired communications: OTN, SONET/SDH, GE, 10 GE, FC and 10G FC
- PCI Express generation 1/2/3 clock distribution
- Wireless communications
- High performance microprocessor clock distribution

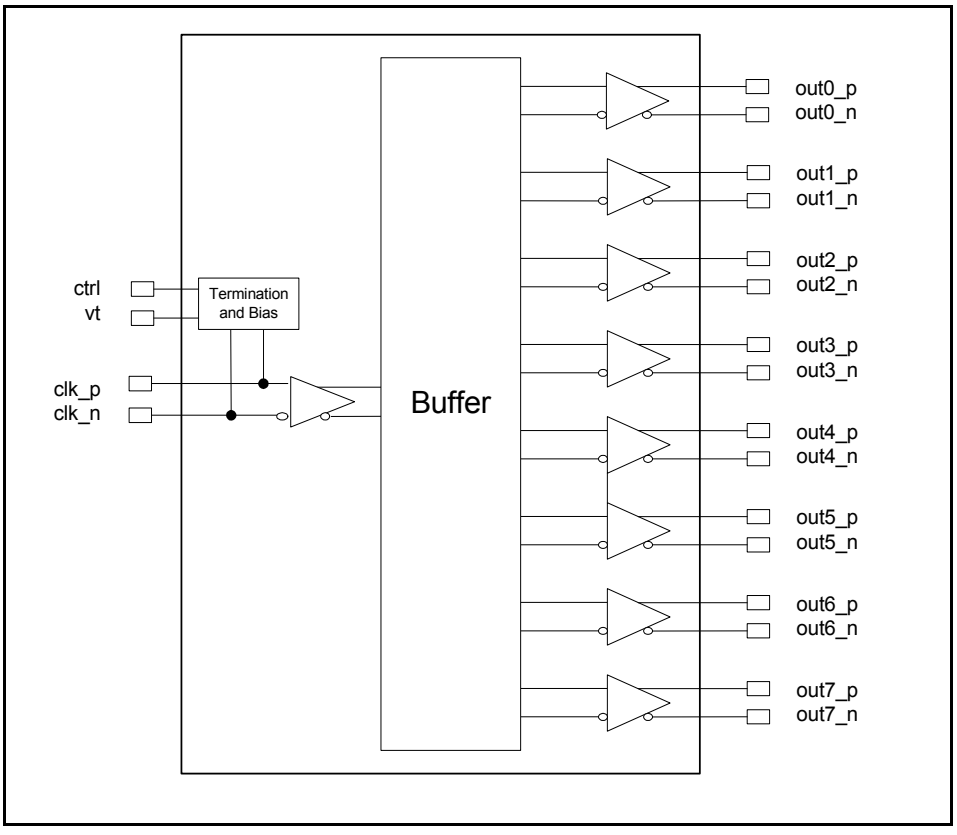



**Figure 1 - Functional Block Diagram**

# Table of Contents

# List of Figures

## Change Summary

Below are the changes from the February 2013 issue to the April 2014 issue:

| Page | Item | Change |
|---|---|---|
| 1 | Applications | Added PCI Express clock distribution. |
| 6 | Pin Description | Added exposed pad to Pin Description. |
| 8 | Figure 4 and Figure 5 | Removed 22 Ohm series resistors from Figure 4 and 5. These resistors are not required; however there is no impact to performance if the resistors are included. |
| 16 | Power supply filtering | Corrected typo of 0.3 ohm to 0.15 ohm. |
| 18 | Figure 19 | Clarification of $V_{ID}$ and $V_{OD}$. |

Below are the changes from the November 2012 issue to the February 2013 issue:

| Page | Item | Change |
|---|---|---|
| 8 | Figure 4 | Changed text to indicate the circuit is not recommended for VDD_driver=2.5V. |
| 12 | Figure 12 | Changed gate values to +/+ on the left and -/- on the right. |

## 1.0 Package Description

The device is packaged in a 32 pin QFN

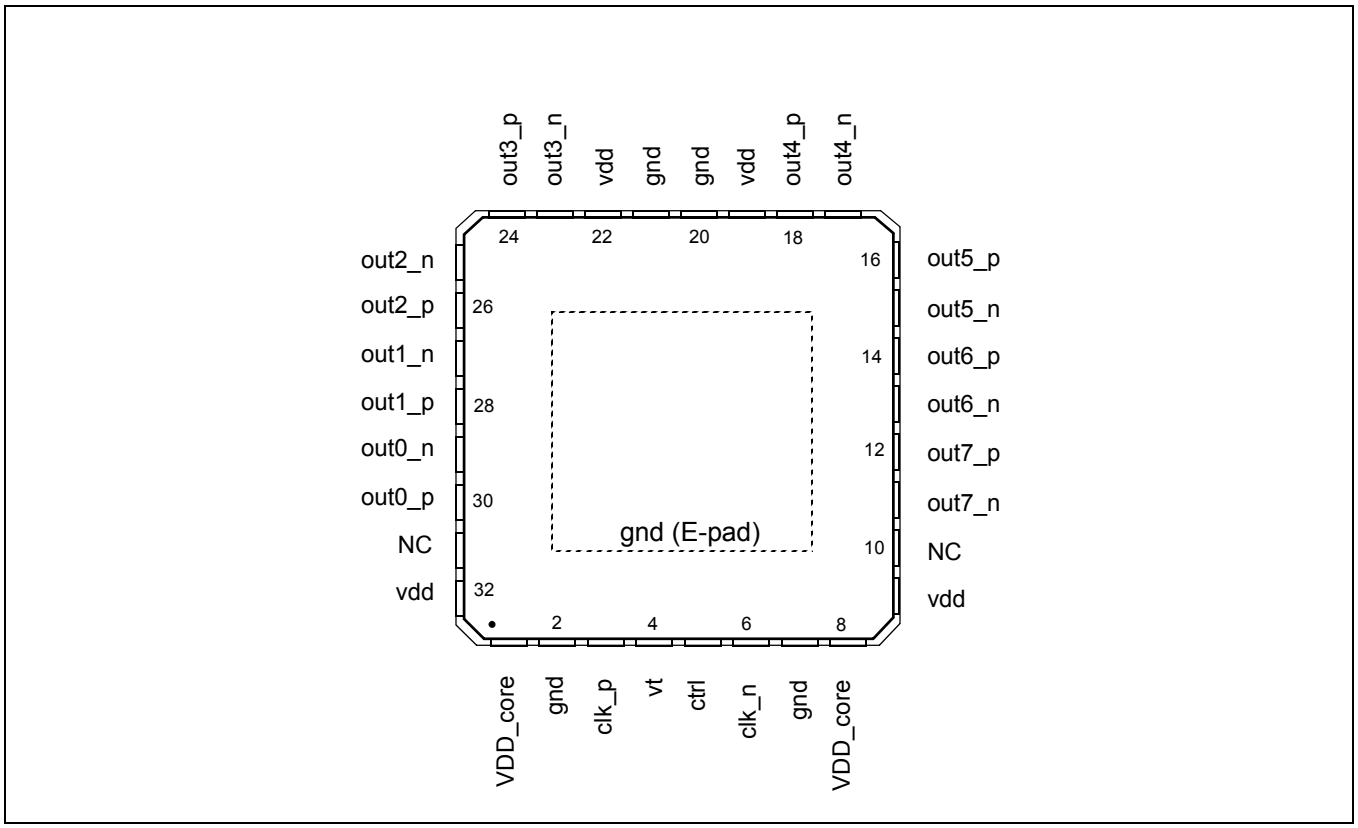



**Figure 2 - Pin Connections**

## 2.0 Pin Description

| Pin # | Name | Description |
|---|---|---|
| 3, 6 | clk_p, clk_n, | **Differential Input (Analog Input).** Differential (or single ended) input signals. For single-ended inputs see See “Clock Inputs” on page 7 |
| 30, 29, 28, 27, 26, 25, 24, 23, 18, 17, 16, 15, 14, 13, 12, 11 | out0_p, out0_n out1_p, out1_n out2_p, out2_n out3_p, out3_n out4_p, out4_n out5_p, out5_n out6_p, out6_n out7_p, out7_n | **Differential Output (Analog Output).** Differential outputs. |
| 9, 19, 22, 32 | vdd | **Positive Supply Voltage.** 2.5 $V_{DC}$ or 3.3 $V_{DC}$ nominal. |
| 1, 8 | vdd_core | **Positive Supply Voltage.** 2.5 $V_{DC}$ or 3.3 $V_{DC}$ nominal. |
| 2, 7, 20, 21 | gnd | **Ground.** 0 V. |
| 4 | vt | **On-Chip Input Termination Node (Analog).** Center tap between internal 50 Ohm termination resistors. The use of this pin is detailed in section “Clock Inputs” on page 7, for various input signal types. |
| 5 | ctrl | **Digital Control for On-Chip Input Termination (Input).** Selects differential input mode; 0: DC coupled LVPECL or LVDS modes 1: AC coupled differential modes This pin is internally pulled down to GND. The use of this pin is detailed in section “Clock Inputs” on page 7, for various input signal types. |
| 10, 31 | NC | **No Connection.** Leave unconnected. |
| Exposed Pad | | **Device GND**. |

## 3.0 Functional Description

he ZL40219 is an LVDS clock fanout buffer with eight output clock drivers capable of operating at frequencies up to 750MHz.

The ZL40219 provides an internal input termination network for DC and AC coupled inputs; optional input biasing for AC coupled inputs is also provided. The ZL40219 can accept DC coupled LVPECL or LVDS and AC coupled LVPECL and LVDS input signals, AC coupled CML or HCSL input signals, and single ended signals. A pin compatible device with external termination is also available.

The ZL40219 is designed to fan out low-jitter reference clocks for wired or optical communications applications while adding minimal jitter to the clock signal. An internal linear power supply regulator and bulk capacitors minimize additive jitter due to power supply noise. The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

The device block diagram is shown in Figure 1; its operation is described in the following sections.

### 3.1 Clock Inputs

The device has a differential input equipped with two on-chip 50 Ohm termination resistors arranged in series with a center tap. The input can accept many differential and single-ended signals with AC or DC coupling as appropriate. A control pin is available to enable internal biasing for AC coupled inputs. A block diagram of the input stage is in Figure 3.

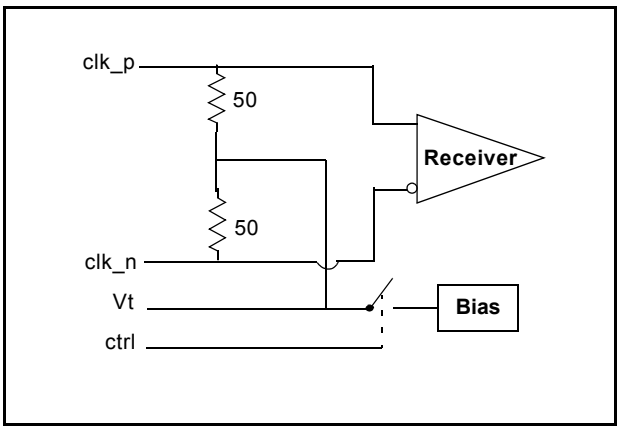



**Figure 3 - Simplified Diagram of Input Stage**

This following figures give the components values and configuration for the various circuits compatible with the input stage and the use of the *Vt* and *ctrl* pins in each case.

In the following diagrams where the *ctrl* pin is logically one and the *Vt* pin is not connected, the *Vt* pin can be instead connected to VDD with a capacitor. A capacitor can also help in Figure 4 between *Vt* and VDD. This capacitor will minimize the noise at the point between the two internal termination resistors and improve the overall performance of the device.

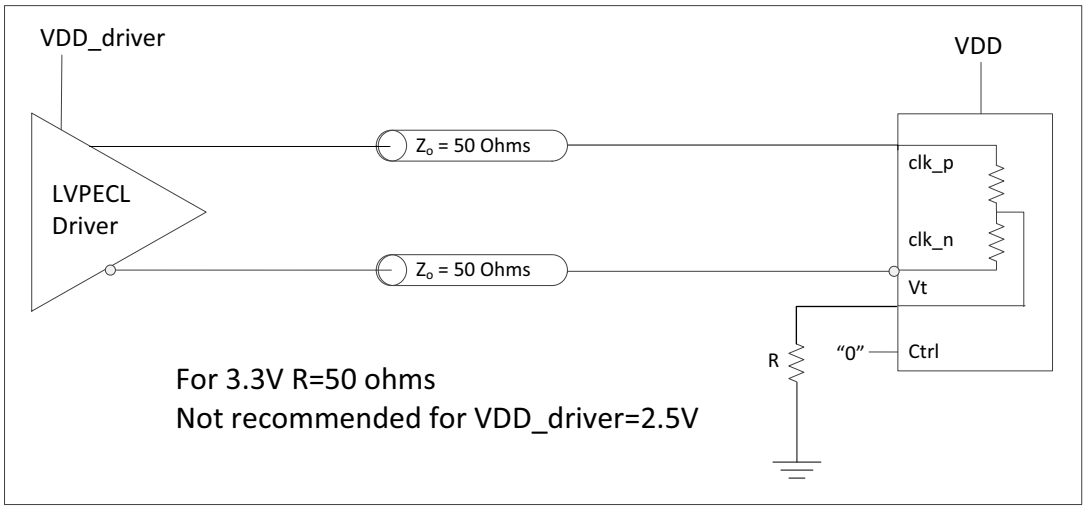



**Figure 4 - Clock Input - LVPECL - DC Coupled**

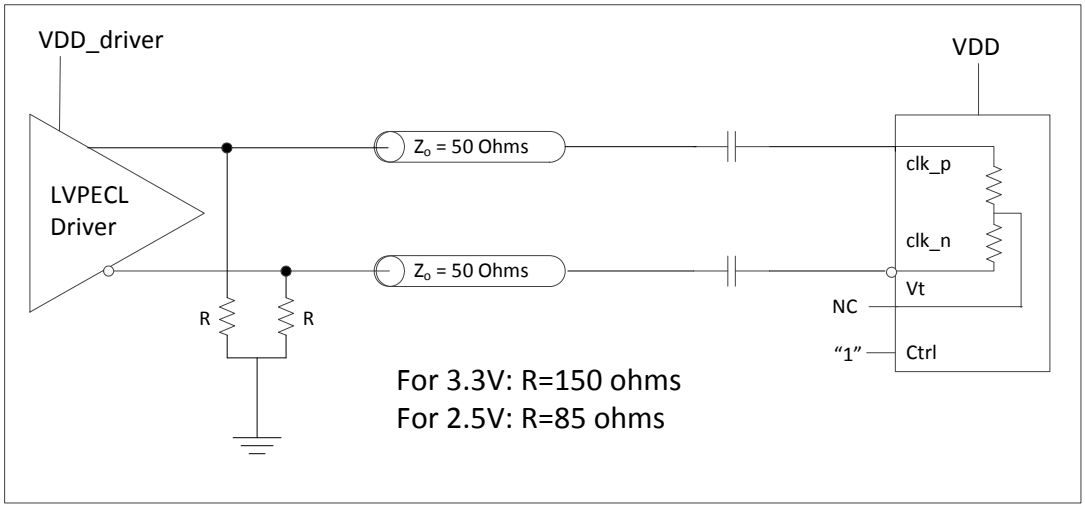



**Figure 5 - Clock Input - LVPECL - AC Coupled**

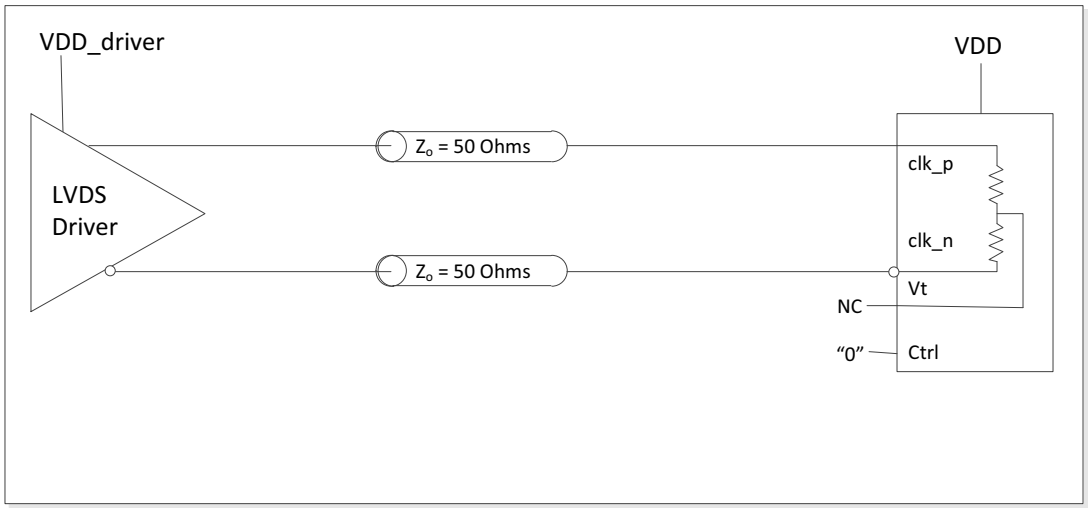



**Figure 6 - Clock Input - LVDS - DC Coupled**

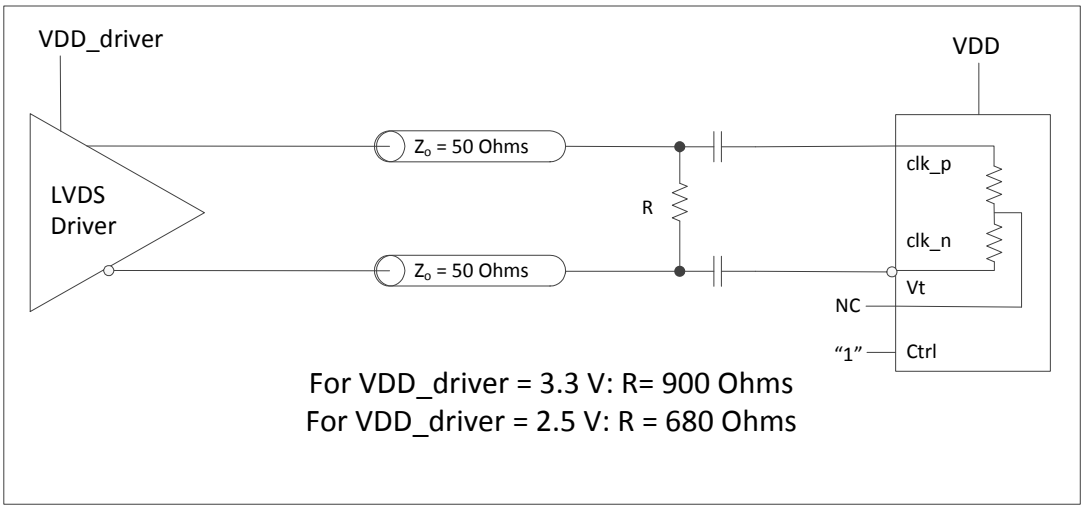



**Figure 7 - Clock Input - LVDS - AC Coupled**

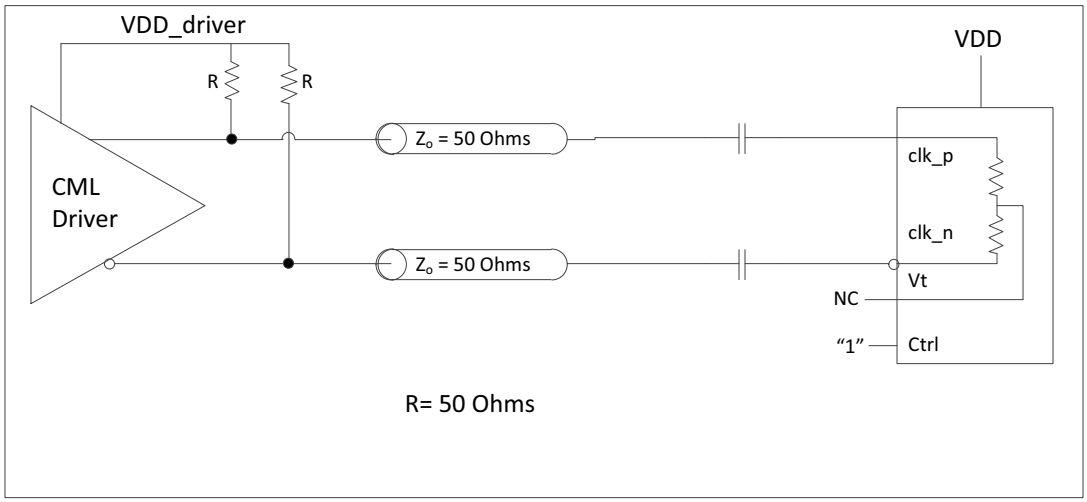



**Figure 8 - Clock Input - CML- AC Coupled**

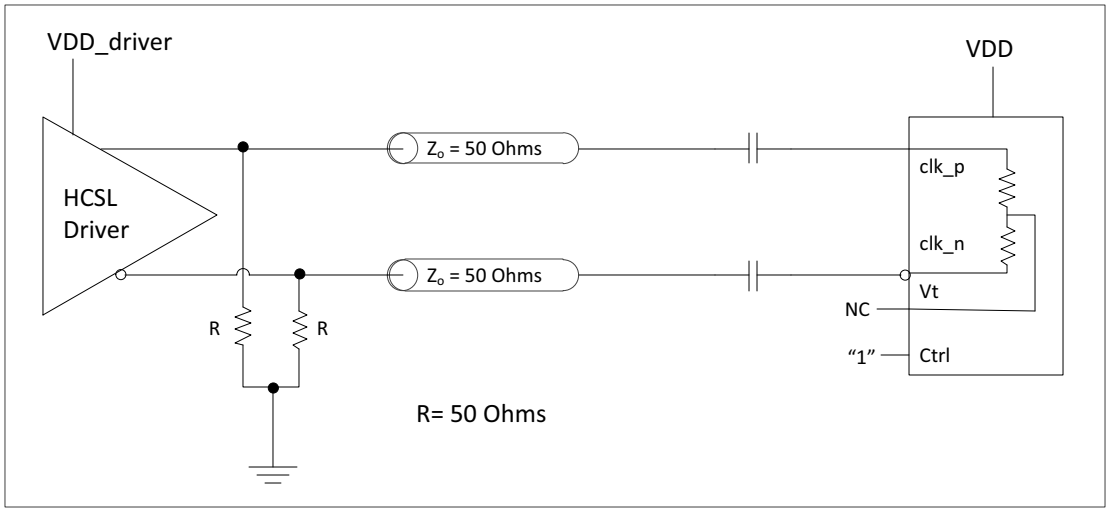



**Figure 9 - Clock Input - HCSL- AC Coupled**

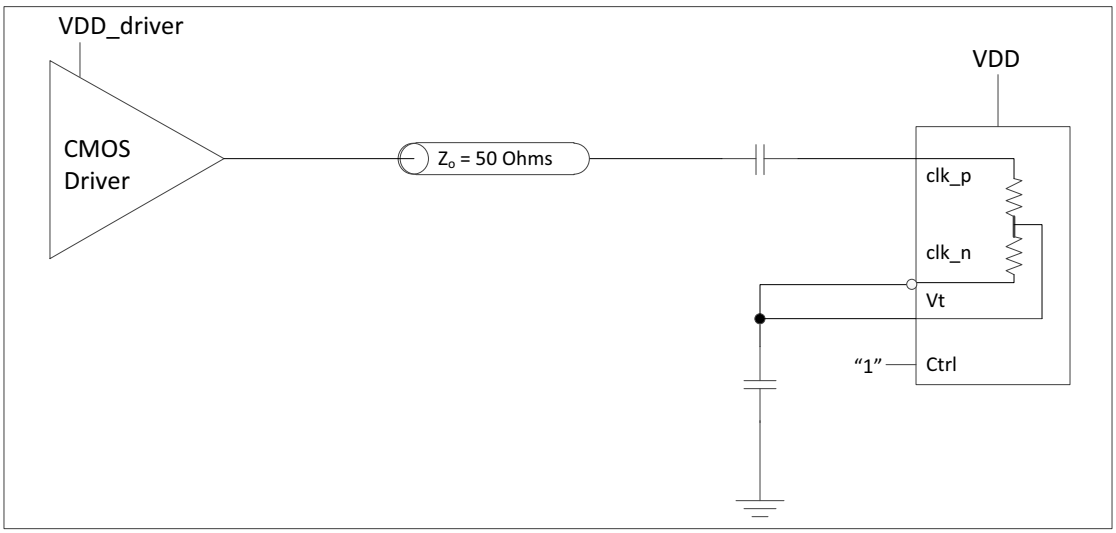



**Figure 10 - Clock Input - AC-coupled Single-Ended**

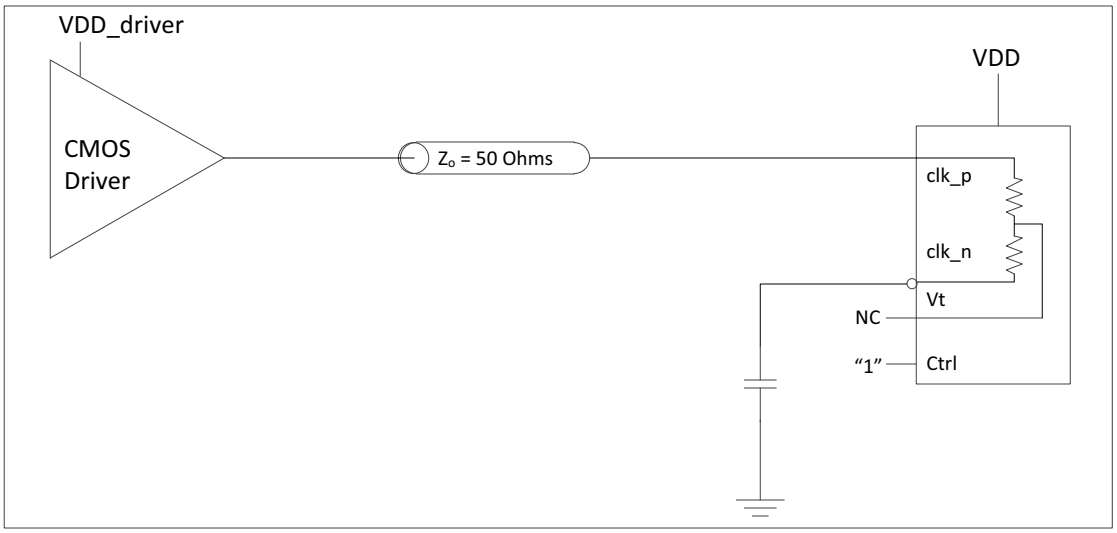



**Figure 11 - Clock Input - DC-coupled 3.3V CMOS**

### 3.2 Clock Outputs

LVDS has lower signal swing than LVPECL which results in a low power consumption. A simplified diagram for the LVDS output stage is shown in Figure 12.

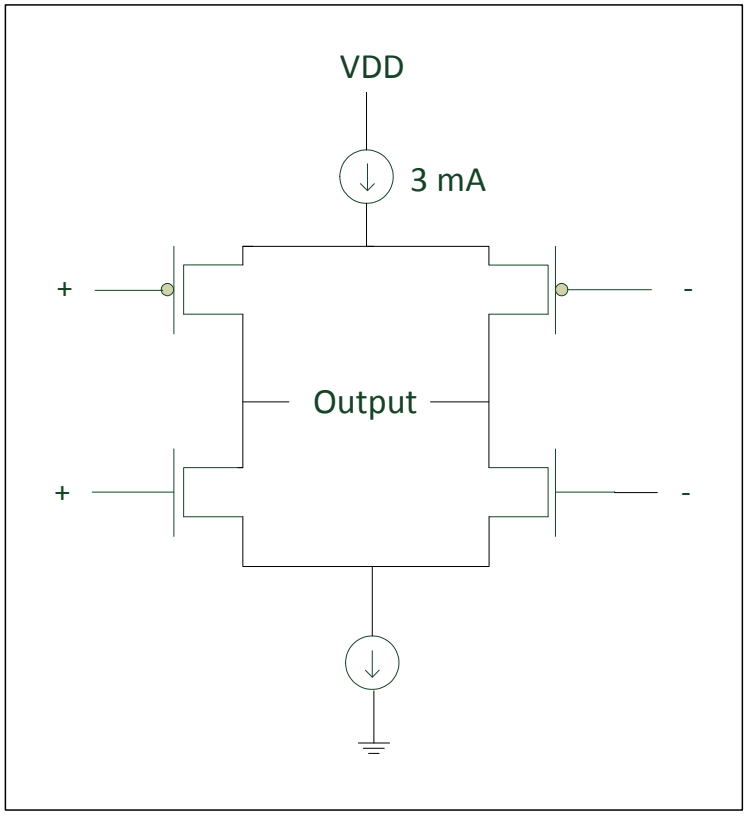



**Figure 12 - Simplified LVDS Output Driver**

The methods to terminate the ZL40219 drivers are shown in the following figures.

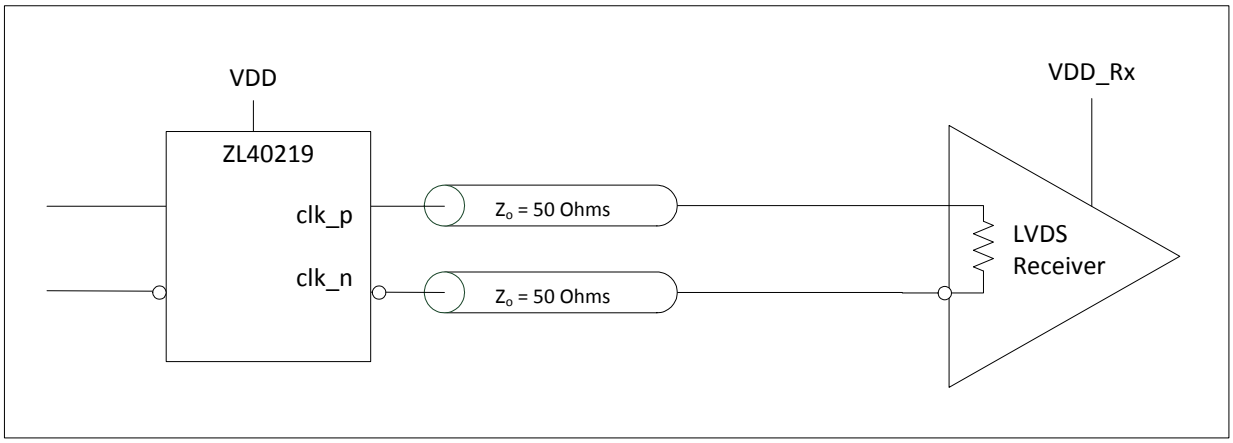



**Figure 13 - LVDS DC Coupled Termination (Internal Receiver Termination)**

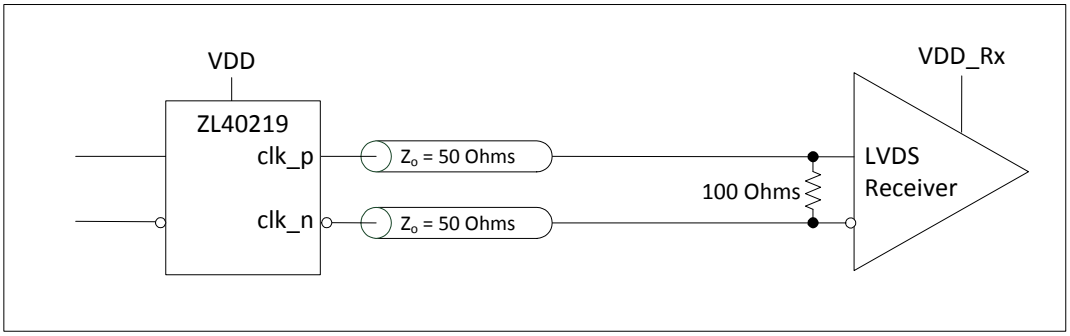



**Figure 14 - LVDS DC Coupled Termination (External Receiver Termination)**

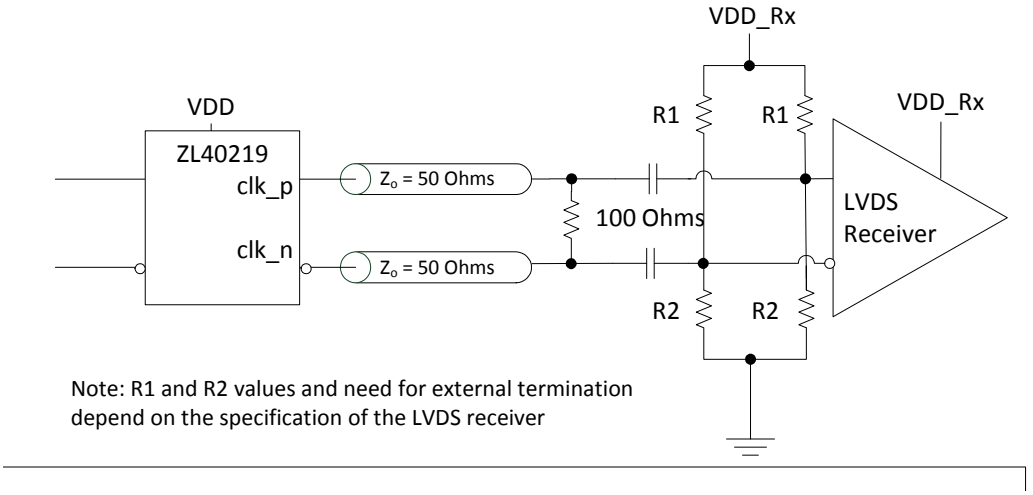



**Figure 15 - LVDS AC Coupled Termination**

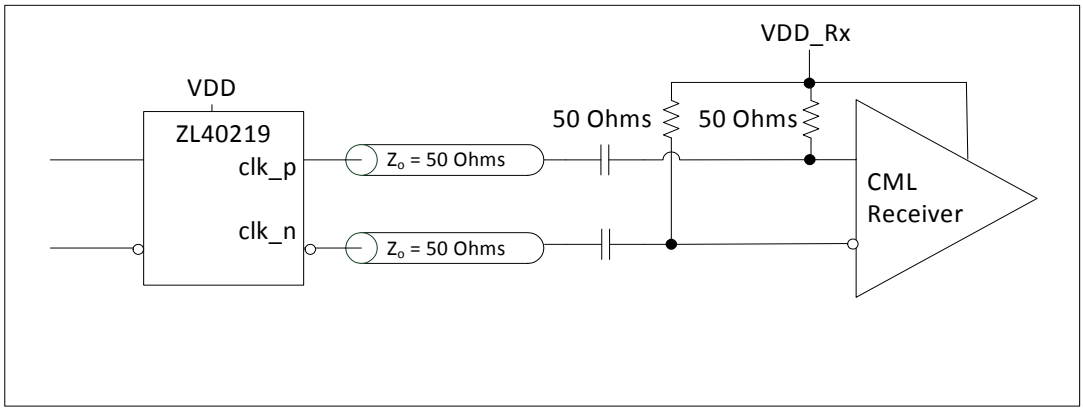



**Figure 16 - LVDS AC Output Termination for CML Inputs**

### 3.3 Device Additive Jitter

The ZL40219 clock fanout buffer is not intended to filter clock jitter. The jitter performance of this type of device is characterized by its additive jitter. Additive jitter is the jitter the device would add to a hypothetical jitter-free clock as it passes through the device. The additive jitter of the ZL40219 is random and as such it is not correlated to the jitter of the input clock signal.

The square of the resultant random RMS jitter at the output of the ZL40219 is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources, but they are not shown in Figure 17.

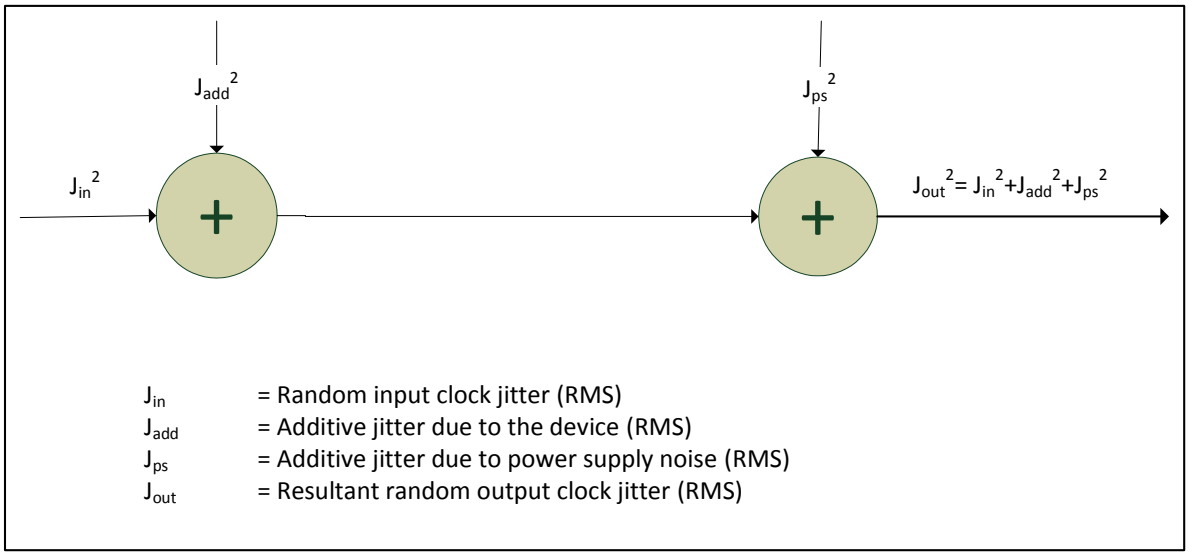



**Figure 17 - Additive Jitter**

## 3.4 Power Supply

This device operates employing either a 2.5V supply or 3.3V supply.

### 3.4.1 Sensitivity to power supply noise

Power supply noise from sources such as switching power supplies and high-power digital components such as FPGAs can induce additive jitter on clock buffer outputs. The ZL40219 is equipped with an on-chip linear power regulator and on-chip bulk capacitors to minimize additive jitter due to power supply noise. The on-chip regulation, recommended power supply filtering, and good PCB layout all work together to minimize the additive jitter from power supply noise.

### 3.4.2 Power supply filtering

Jitter levels may increase when noise is present on the power pins. For optimal jitter performance, the device should be isolated from the power planes connected to its power supply pins as shown in Figure •.

- 10 µF capacitors should be size 0603 or size 0805 X5R or X7R ceramic, 6.3 V minimum rating
- 0.1 µF capacitors should be size 0402 X5R ceramic, 6.3 V minimum rating
- Capacitors should be placed next to the connected device power pins
- A 0.15 ohm resistor is recommended

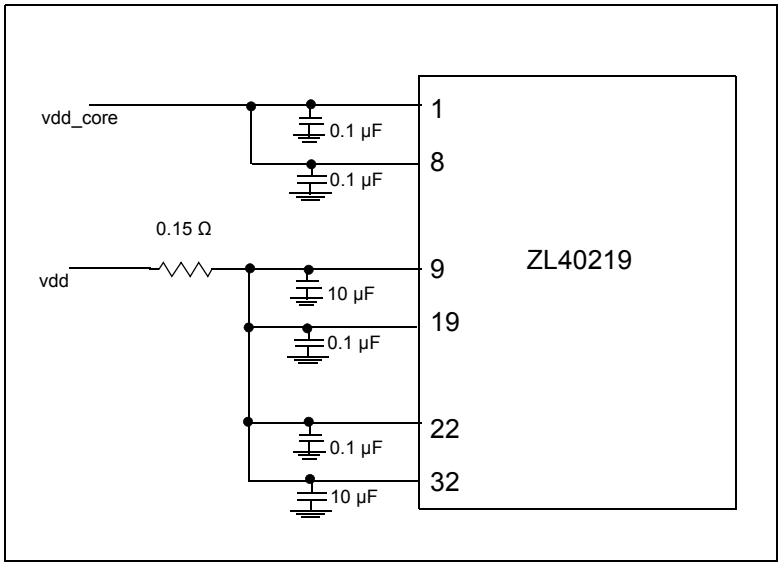



**Figure 18 - Decoupling Connections for Power Pins**

### 3.4.3 PCB layout considerations

The power nets in Figure 18 can be implemented either as a plane island or routed power topology without effect overall jitter performance of the device.

## 4.0 AC and DC Electrical Characteristics

**Absolute Maximum Ratings***

| | Parameter | Sym. | Min. | Max. | Units |
|---|---|---|---|---|---|
| 1 | Supply voltage | $V_{DD\_R}$ | -0.5 | 4.6 | V |
| 2 | Voltage on any digital pin | $V_{PIN}$ | -0.5 | $V_{DD}$ | V |
| 3 | Soldering temperature | T | | 260 | °C |
| 4 | Storage temperature | $T_{ST}$ | -55 | 125 | °C |
| 5 | Junction temperature | $T_j$ | | 125 | °C |
| 6 | Voltage on input pin | $V_{input}$ | | $V_{DD}$ | V |
| 7 | Input capacitance each pin | $C_p$ | | 500 | fF |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

**Recommended Operating Conditions***

| | Characteristics | Sym. | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| 1 | Supply voltage 2.5 V mode | $V_{DD25}$ | 2.375 | 2.5 | 2.625 | V |
| 2 | Supply voltage 3.3 V mode | $V_{DD33}$ | 3.135 | 3.3 | 3.465 | V |
| 3 | Operating temperature | $T_A$ | -40 | 25 | 85 | °C |

* Voltages are with respect to ground (GND) unless otherwise stated

**DC Electrical Characteristics - Current Consumption**

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Supply current LVDS drivers - loaded (all outputs are active) | $I_{dd\_load}$ | | 112 | | mA | |

**DC Electrical Characteristics - Inputs and Outputs - for 2.5/3.3 V Supply**

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | CMOS control logic high-level input | $V_{CIH}$ | 0.7*$V_{DD}$ | | | V | |
| 2 | CMOS control logic low-level input | $V_{CIL}$ | | | 0.3*$V_{DD}$ | V | |
| 3 | CMOS control logic Input leakage current | $I_{IL}$ | | 1 | | µA | $V_I$ = $V_{DD}$ or 0 V |
| 4 | Differential input common mode voltage | $V_{ICM}$ | 1.1 | | 1.6 | V | for 2.5 V |
| 5 | Differential input common mode voltage | $V_{ICM}$ | 1.1 | | 2.0 | V | for 3.3 V |
| 6 | Differential input voltage difference | $V_{ID}$ | 0.25 | | 1 | V | |
| 7 | Differential input resistance | $V_{IR}$ | 80 | 100 | 120 | ohm | |
| 8 | LVDS output differential voltage* | $V_{OD}$ | 0.25 | 0.30 | 0.40 | V | |
| 9 | LVDS Common Mode voltage | $V_{CM}$ | 1.1 | 1.25 | 1.375 | V | |

* The VOD parameter was measured between 125 and 750 MHz

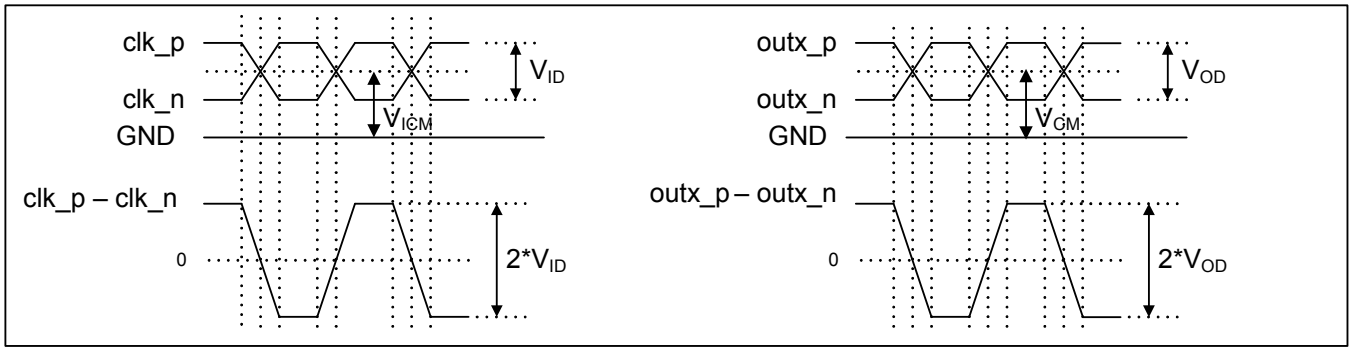



**Figure 19 - Differential Output Voltage Parameter**

**AC Electrical Characteristics* - Inputs and Outputs (see Figure 20) - for 2.5/3.3 V Supply.**

| | Characteristics | Sym. | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|---|
| 1 | Maximum Operating Frequency | $1/t_p$ | | | 750 | MHz | |
| 2 | Input to output clock propagation delay | $t_{pd}$ | 0 | 1 | 2 | ns | |
| 3 | Output to output skew | $t_{out2out}$ | | 80 | 150 | ps | |
| 4 | Part to part output skew | $t_{part2part}$ | | 120 | 300 | ps | |
| 5 | Output clock Duty Cycle degradation | $t_{PWH}/ t_{PWL}$ | -5 | 0 | 5 | Percent | |
| 6 | LVDS Output slew rate | $r_{SL}$ | 0.55 | | | V/ns | |

* Supply voltage and operating temperature are as per Recommended Operating Conditions

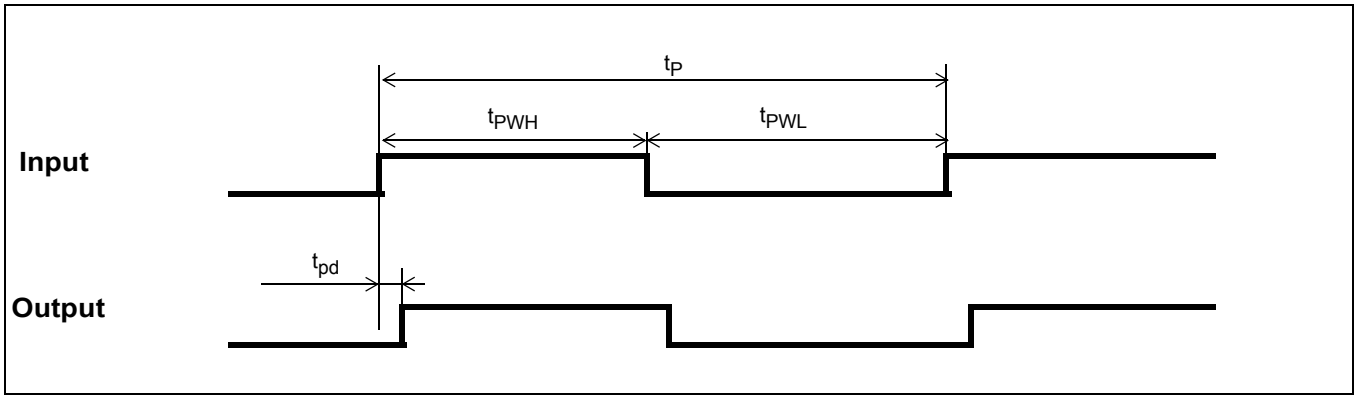



**Figure 20 - Input To Output Timing**

## 5.0 Performance Characterization

### Additive Jitter at 2.5 V*

| | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|---|---|---|---|
| 1 | 125 | 12 kHz - 20 MHz | 184 | |
| 2 | 212.5 | 12 kHz - 20 MHz | 174 | |
| 3 | 311.04 | 12 kHz - 20 MHz | 157 | |
| 4 | 425 | 12 kHz - 20 MHz | 152 | |
| 5 | 500 | 12 kHz - 20 MHz | 139 | |
| 6 | 622.08 | 12 kHz - 20 MHz | 138 | |
| 7 | 750 | 12 kHz - 20 MHz | 135 | |

*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

### Additive Jitter at 3.3 V*

| | Output Frequency (MHz) | Jitter Measurement Filter | Typical RMS (fs) | Notes |
|---|---|---|---|---|
| 1 | 125 | 12 kHz - 20 MHz | 187 | |
| 2 | 212.5 | 12 kHz - 20 MHz | 176 | |
| 3 | 311.04 | 12 kHz - 20 MHz | 156 | |
| 4 | 425 | 12 kHz - 20 MHz | 153 | |
| 5 | 500 | 12 kHz - 20 MHz | 140 | |
| 6 | 622.08 | 12 kHz - 20 MHz | 139 | |
| 7 | 750 | 12 kHz - 20 MHz | 137 | |

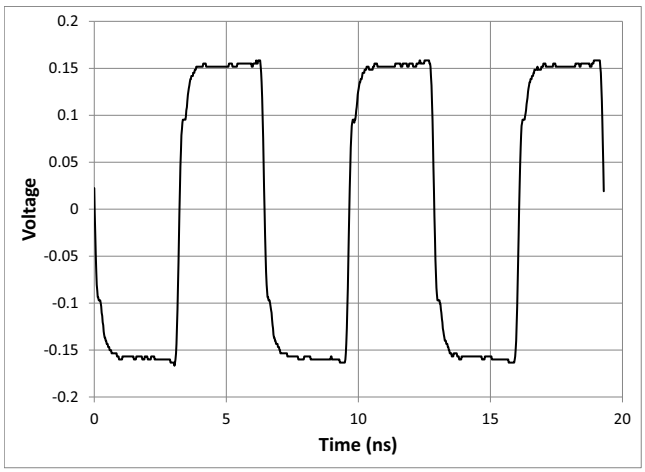
*The values in this table were taken with an approximate slew rate of 0.8 V/ns.

### Additive Jitter from a Power Supply Tone*

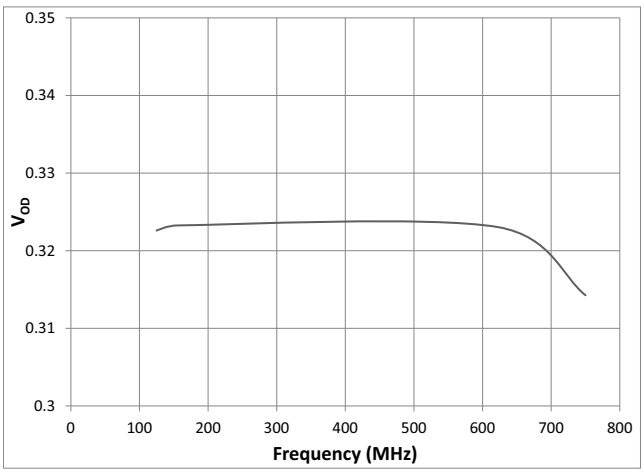
| Carrier frequency | Parameter | Typical | Units | Notes |
|---|---|---|---|---|
| 125MHz | 25 mV at 100 kHz | 33 | fs RMS | |
| 750MHz | 25 mV at 100 kHz | 33 | fs RMS | |

* The values in this table are the additive periodic jitter caused by an interfering tone typically caused by a switching power supply. For this test, measurements were taken over the full temperature and voltage range for $V_{DD}$ = 3.3 V. The magnitude of the interfering tone is measured at the DUT.

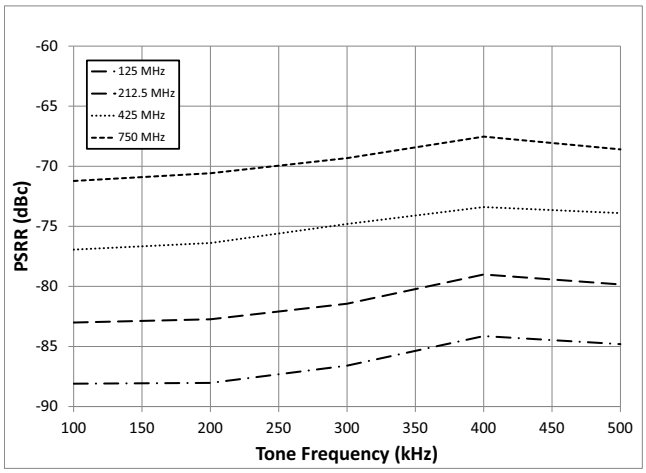
## 6.0 Typical Behavior



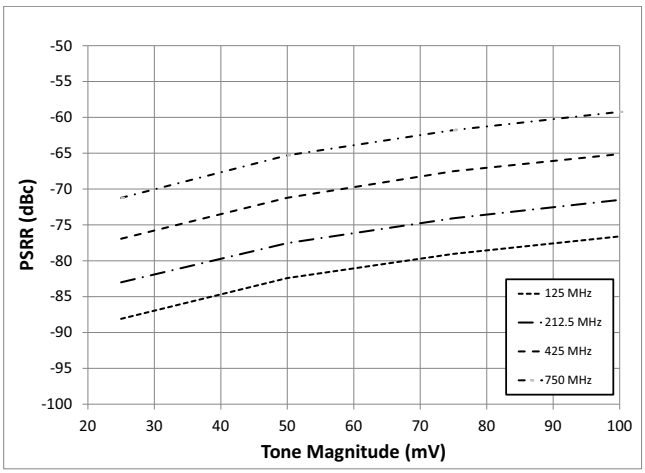

Typical Waveform at 155.52 MHz



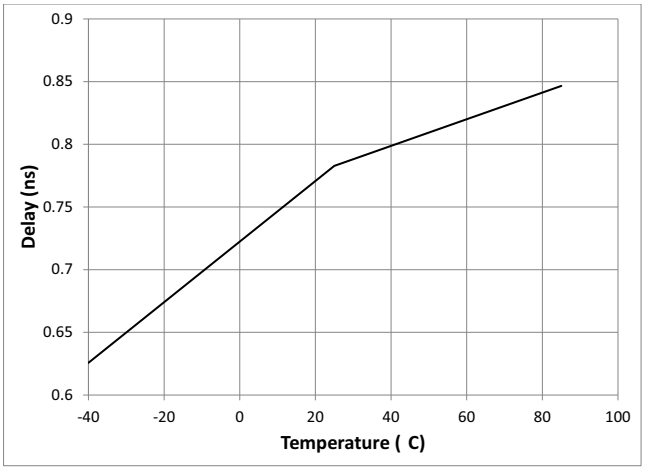

$V_{OD}$ vs Frequency




Power Supply Tone Frequency versus PSRR




Power Supply Tone Magnitude versus PSRR




Propagation Delay versus Temperature

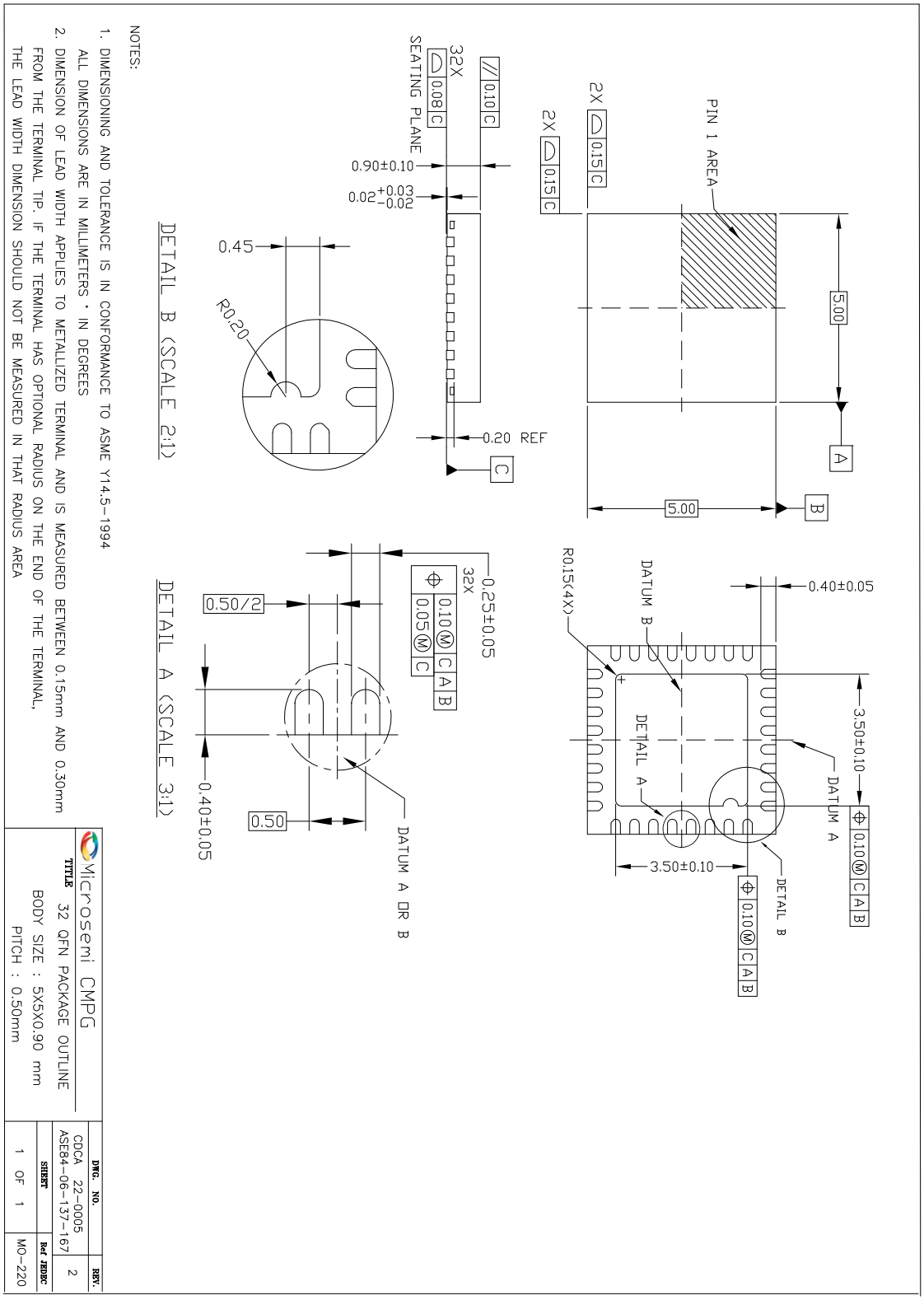
Note: This is for a single device. For more details, see the characterization section.

## 7.0 Package Characteristics

### Thermal Data

| Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|
| Junction to Ambient Thermal Resistance | $\Theta_{JA}$ | Still Air<br>1 m/s<br>2 m/s | 37.4<br>33.1<br>31.5 | $^{o}$C/W |
| Junction to Case Thermal Resistance | $\Theta_{JC}$ | | 24.4 | $^{o}$C/W |
| Junction to Board Thermal Resistance | $\Theta_{JB}$ | | 19.5 | $^{o}$C/W |
| Maximum Junction Temperature* | $T_{jmax}$ | | 125 | $^{o}$C |
| Maximum Ambient Temperature | $T_{A}$ | | 85 | $^{o}$C |

## 8.0 Mechanical Drawing



For more information about all Microsemi products
visit our website at
www.microsemi.com

TECHNICAL DOCUMENTATION – NOT FOR RESALE

Microsemi Corporate Headquarters One
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world’s standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at www.microsemi.com.