TS8388B
ADC 8-bit 1 Gsps

Datasheet

1. Features

- 8-bit Resolution
- ADC Gain Adjust
- 1.5 GHz Full Power Input Bandwidth (–3 dB)
- 1 Gsps (min.) Sampling Rate
- SINAD = 44.3 dB (7.2 Effective Bits), SFDR = 58 dBc, at F_S = 1 Gsps, F_{IN} = 20 MHz
- SINAD = 42.9 dB (7.0 Effective Bits), SFDR = 52 dBc, at F_S = 1 Gsps, F_{IN} = 500 MHz
- SINAD = 40.3 dB (6.8 Effective Bits), SFDR = 50 dBc, at F_S = 1 Gsps, F_{IN} = 1000 MHz (–3 dBFS)
- 2-tone IMD: –52 dBc (489 MHz, 490 MHz) at 1 Gsps
- DNL = 0.3 lsb, INL = 0.7 lsb
- Low Bit Error Rate (10^{-13}) at 1 Gsps
- Very Low Input Capacitance: 3 pF
- 500 mVpp Differential or Single-ended Analog Inputs
- Differential or Single-ended 50Ω ECL Compatible Clock Inputs
- ECL or LVDS/HSTL Output Compatibility
- Data Ready Output with Asynchronous Reset
- Gray or Binary Selectable Output Data; NRZ Output Mode
- Power Consumption: 3.4W at T_J = 70°C Typical
- Radiation Tolerance Oriented Design (150 Krad (Si) Measured)
- Two Package Versions
- Evaluation Board: TSEV8388B
- Demultiplexer TS81102G0: Companion Device Available

2. Applications

- Digital Sampling Oscilloscopes
- Satellite Receiver
- Electronic Countermeasures/Electronic Warfare
- Direct RF Down-conversion

3. Description

The TS8388B is a monolithic 8-bit analog-to-digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 1 Gsps.

The TS8388B uses an innovative architecture, including an on-chip Sample and Hold (S/H), and is fabricated with an advanced high-speed bipolar process.

The on-chip S/H has a 1.5 GHz full power input bandwidth, providing excellent dynamic performance in undersampling applications (high IF digitizing).

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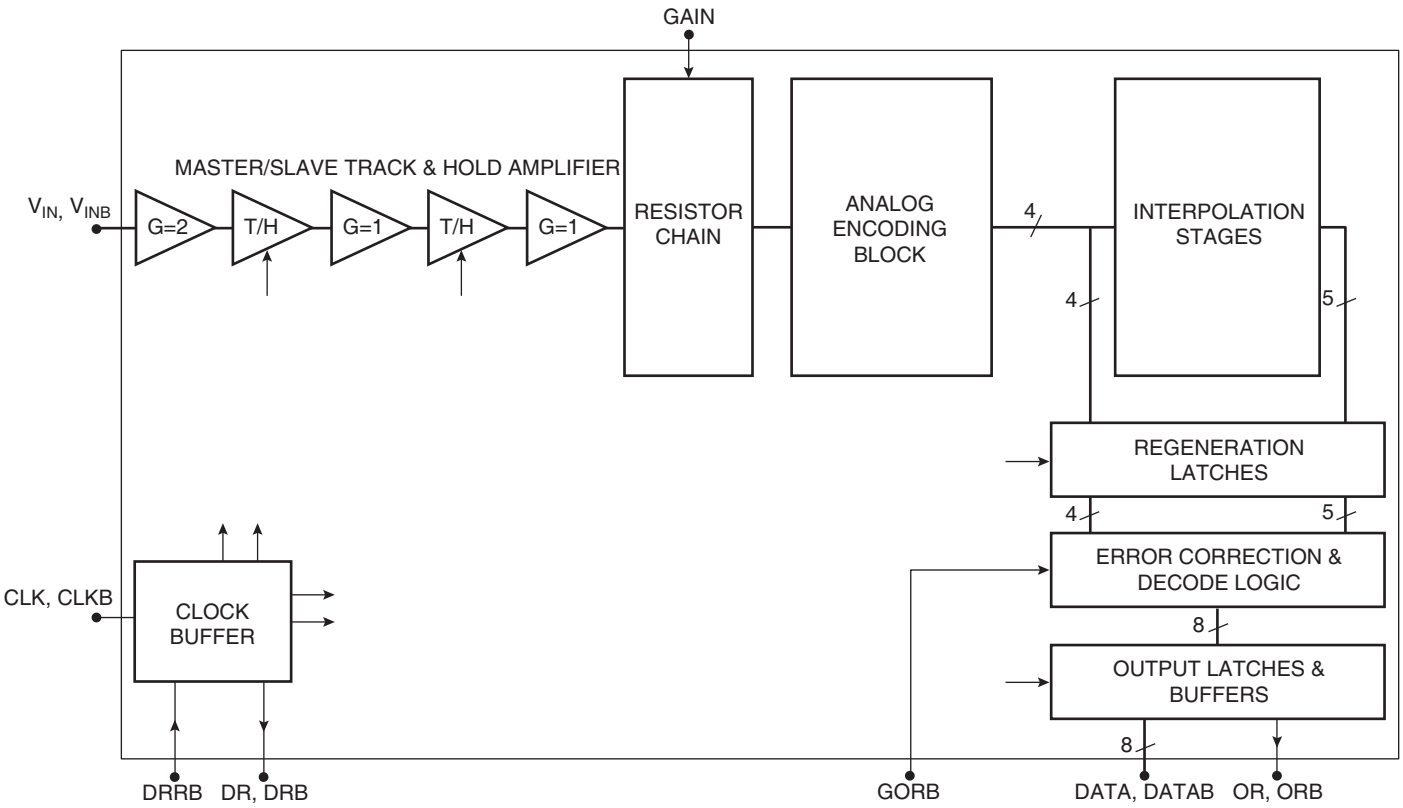
4. Functional Description

4.1 Block Diagram

The following figure shows the simplified block diagram.

Figure 4-1. Simplified Block Diagram



4.2 Functional Description

The TS8388B is an 8-bit 1 Gsps ADC based on an advanced high-speed bipolar technology featuring a cutoff frequency of 25 GHz.

The TS8388B includes a front-end master/slave Track and Hold stage (S/H), followed by an analog encoding stage and interpolation circuitry.

Successive banks of latches regenerate the analog residues into logical data before entering an error correction circuitry and a resynchronization stage followed by 75Ω differential output buffers.

The TS8388B works in fully differential mode from analog inputs up to digital outputs.
The TS8388B features a full-power input bandwidth of 1.5 GHz.
A control pin GORB is provided to select either Gray or Binary data output format.
A gain control pin is provided in order to adjust the ADC gain.
A Data Ready output asynchronous reset (DRRB) is available on TS8388B.

The TS8388B uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, which allow enhanced radiation tolerance (no performance drift measured at 150 kRad total dose).

5. Specifications

5.1 Absolute Maximum Ratings

Table 5-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	DV_{EE}		GND to –5.7	V
Digital positive supply voltage	V_{PLUSD}		GND –0.3 to 2.8	V
Negative supply voltage	V_{EE}		GND to –6	V
Maximum difference between negative supply voltage	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		–1 to +1	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		–2 to +2	V
Digital input voltage	V_D	GORB	–0.3 to V_{CC} +0.3	V
Digital input voltage	V_D	DRRB	V_{EE} –0.3 to +0.9	V
Digital output voltage	V_O		V_{PLUSD} –3 to V_{PLUSD} –0.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		–3 to +1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		–2 to +2	V
Maximum junction temperature	T_J		+135	°C
Storage temperature	T_{stg}		–65 to +150	°C
Lead temperature (soldering 10s)	T_{leads}		+300	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability. The use of a thermal heat sink is mandatory. See “The board set comes fully assembled and tested, with the TS8388B installed.” on page 43.

5.2 Recommended Operating Conditions

Table 5-2. Recommended Operating Conditions

Parameter	Symbol	Comments	Recommended Value			Unit
			Min	Typ	Max	
Positive supply voltage	V_{CC}		4.5	+5	5.25	V
Positive digital supply voltage	V_{PLUSD}	ECL output compatibility	–	GND	–	V
Positive digital supply voltage	V_{PLUSD}	LVDS output compatibility	+1.4	+2.4	+2.6	V
Negative supply voltage	V_{EE}, DV_{EE}		–5.25	–5	–4.75	V
Differential analog input voltage (Full Scale)	V_{IN}, V_{INB} V_{IN} - V_{INB}	50Ω differential or single-ended	±113 450	±125 500	±137 550	mV mVpp
Clock input power level	P_{CLK}, P_{CLKB}	50Ω single-ended clock input	3	4	10	dBm
Operating temperature range	T_J	Commercial grade: “C” Industrial grade: “V” Military grade: “M”	0 < Tc; T_J < 90 –40 < Tc; T_J < 110 –55 < Tc; T_J < +125			°C

5.3 Electrical Operating Characteristics

- V_{EE} = DV_{EE} = –5V; V_{CC} = +5V; V_{IN} - V_{INB} = 500 mVpp Full Scale differential input
- Digital outputs 75 or 50Ω differentially terminated
- T_J (typical) = 70°C. Full Temperature Range: up to –55°C < Tc; T_J - < +125°C, depending on device grade

Table 5-3. Electrical Specifications

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
Power Requirements (CBGA68 package)							
Positive supply voltage							
Analog	V_{CC}	1	4.5	5	5.5	V	
Digital (ECL)	V_{PLUSD}	4	–	0	–	V	
Digital (LVDS)	V_{PLUSD}	4	1.4	2.4	2.6	V	
Positive supply current							
Analog	I_{CC}	1	–	420	445	mA	
Digital	I_{PLUSD}	1	–	130	145	mA	
Negative supply voltage	V_{EE}	1	–5.5	–5	–4.5	V	
Negative supply current							
Analog	AI_{EE}	1	–	185	200	mA	
Digital	DI_{EE}	1	–	160	180	mA	
Nominal power dissipation	PD	1	–	3.9	4.1	W	
Power supply rejection ratio	PSRR	4	–	0.5	2	mV/V	
Power Requirements							
Power Requirements (CQFP68 packaged device)							
Positive supply voltage							
Analog	V_{CC}	1, 2, 6	4.7	5	5.3	V	
Digital (ECL)	V_{PLUSD}	4	–	0	–	V	
Digital (LVDS)	V_{PLUSD}	4	1.4	2.4	2.6	V	
Positive supply current							
	I_{CC}	1, 2	–	385	445	mA	
Analog		6	–	395	445	mA	
	I_{PLUSD}	1, 2	–	115	145	mA	
Digital		6	–	120	145	mA	
Negative supply voltage	V_{EE}	1, 2, 6	–5.3	–5	–4.7	V	
Negative supply current							
	AI_{EE}	1, 2	–	165	200	mA	
Analog		6	–	170	200	mA	
	DI_{EE}	1, 2	–	135	180	mA	
Digital		6	–	145	180	mA	

Table 5-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
Nominal power dissipation	PD	1, 2 6	– –	3.4 3.6	4.1 4.3	W W	
Power supply rejection ratio	PSRR	4	–	0.5	2	mV/V	
Resolution	–	–	–	8	–	bits	(2)
Analog Inputs							
Full Scale Input Voltage range (differential mode) (0V common mode voltage)	V_{IN} V_{INB}	4 –	–125 –125	– –	125 125	mV mV	
Full Scale Input Voltage range (single-ended input option) (See Application Notes)	V_{IN} V_{INB}	4 –	–250 –	– 0	250 –	mV mV	
Analog input capacitance	C_{IN}	4	–	3	3.5	pF	
Input bias current	I_{IN}	4	–	10	20	µA	
Input Resistance	R_{IN}	4	0.5	1	–	MΩ	
Full Power input Bandwidth (–3dB) CBGA68 package CQFP68 package	FPBW – –	– 4 4	– – –	– 1.8 1.5	– – –	– GHz GHz	–
Small signal input Bandwidth (10% full scale)	SSBW	4	1.5	1.7	–	GHz	
Clock Inputs							
Logic compatibility for clock inputs (See Application Notes)	–	–	ECL or specified clock input power level in dBm			–	(10)
ECL Clock inputs voltages (V_{CLK} or V_{CLKB}):	–	4	–	–	–	–	
Logic “0” voltage	V_{IL}	–	–	–	–1.5	V	
Logic “1” voltage	V_{IH}	–	–1.1	–	–	V	
Logic “0” current	I_{IL}	–	–	5	50	µA	
Logic “1” current	I_{IH}	–	–	5	50	µA	
Clock input power level into 50Ω termination	–	–	dBm into 50Ω			–	
Clock input power level	–	4	–2	4	10	dBm	
Clock input capacitance	C_{CLK}	4	–	3	3.5	pF	
Digital Outputs Single-ended or differential input mode, 50% clock duty cycle (CLK, CLKB), Binary output data format, T_J (typical) = 70°C.							(1)(6)
Logic compatibility for digital outputs (Depending on the value of V_{PLUSD}) (See Application Notes)	–	–	ECL or LVDS			–	
Differential output voltage swings (assuming V_{PLUSD} = 0V):	–	4	–	–	–	–	
75Ω open transmission lines (ECL levels)	–	–	1.5	1.620	–	V	
75Ω differentially terminated	–	–	0.70	0.825	–	V	

Table 5-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
50Ω differentially terminated	–	–	0.54	0.660	–	V	
Output levels (assuming V_{PLUSD} = 0V) 75Ω open transmission lines:	–	4	–	–	–	–	(6)
Logic “0” voltage	V_{OL}	–	–	–1.62	–1.54	V	
Logic “1” voltage	V_{OH}	–	–0.88	–0.8	–	V	
Output levels (assuming V_{PLUSD} = 0V) 75Ω differentially terminated:	–	4	–	–	–	–	(6)
Logic “0” voltage	V_{OL}	–	–	–1.41	–1.34	V	
Logic “1” voltage	V_{OH}	–	–1.07	–1	–	V	
Output levels (assuming V_{PLUSD} = 0V) 50Ω differentially terminated:	–	–	–	–	–	–	(6)
Logic “0” voltage	V_{OL}	1, 2 6	– –	–1.40 –1.40	–1.32 –1.25	V V	
Logic “1” voltage	V_{OH}	1, 2 6	–1.16 –1.25	–1.10 –1.10	– –	V V	
Differential Output Swing	DOS	4	270	300	–	mV	
Output level drift with temperature	–	4	–	–	1.6	mV/°C	
DC Accuracy (CBGA68 package) Single-ended or differential input mode, 50% clock duty cycle (CLK, CLKB), Binary output data format T_J (typical) = 70°C							
Differential nonlinearity	DNL-	1	–0.6	–0.4	–	lsb	(2)(3)
Differential nonlinearity	DNL+	1	–	0.4	0.6	lsb	
Integral nonlinearity	INL-	1	–1.2	–0.7	–	lsb	(2)(3)
Integral nonlinearity	INL+	1	–	0.7	1.2	lsb	
No missing codes	–	Guaranteed over specified temperature range					(3)
Gain	–	1, 2	90	98	110	%	
Input offset voltage	–	1, 2	–26	–5	26	mV	
Gain error drift Offset error drift	– –	4 4	100 40	125 50	150 60	ppm/°C ppm/°C	
DC Accuracy (CQFP68 package) Single-ended or differential input mode, 50% clock duty cycle (CLK, CLKB), Binary output data format T_J (typical) = 70°C.							
Differential nonlinearity	DNL-	1, 2 6	–0.5 –0.6	–0.25 –0.35	– –	lsb lsb	(2)(3)
Differential nonlinearity	DNL+	1, 2 6	– –	0.3 0.4	0.6 0.7	lsb lsb	

Table 5-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
Integral nonlinearity	INL-	1, 2 6	–1.0 –1.2	0.7 0.9	– –	lsb lsb	(2)(3)
Integral nonlinearity	INL+	1, 2 6	– –	0.7 0.9	1.0 1.2	lsb lsb	
No missing code	–	Guaranteed over specified temperature range					(3)
Gain error	–	1, 2 6	–10 –11	–2 –2	10 11	% F_S % F_S	
Input offset voltage	–	1, 2 6	–26 –30	–5 –5	26 30	mV mV	
Gain error drift Offset error drift	– –	4 4	100 40	125 50	150 60	ppm/°C ppm/°C	
Transient Performance							
Bit Error Rate F_S = 1 Gsps F_{IN} = 62.5 MHz	BER	4	–	–	1E-12	Error/ sample	(2)(4)
ADC settling time V_{IN} -V_{INB} = 400 mVpp	TS	4	–	0.5	1	ns	(2)
Overvoltage recovery time	TOR	4	–	0.5	1	ns	(2)
AC Performance Single-ended or differential input and clock mode, 50% clock duty cycle (CLK, CLKB), Binary output data format, T_J = 70°C, unless otherwise specified.							
Signal to Noise and Distortion ratio	SINAD	–	–	–	–	–	(2)
F_S = 1 Gsps, F_{IN} = 20 MHz		4	42	44	–	dB	
F_S = 1 Gsps, F_{IN} = 500 MHz		4	41	43	–	dB	
F_S = 1 Gsps, F_{IN} = 1000 MHz (-1 dBFs)		4	38	40	–	dB	
F_S = 50 Msps, F_{IN} = 25 MHz		1, 2, 6	40	44	–	dB	
Effective Number of Bits	ENOB	–	–	–	–	–	
F_S = 1 Gsps, F_{IN} = 20 MHz		4	7.0	7.2	–	Bits	
F_S = 1 Gsps, F_{IN} = 500 MHz		4	6.6	6.8	–	Bits	
F_S = 1 Gsps, F_{IN} = 1000 MHz (–1 dBFs)		4	6.2	6.4	–	Bits	
F_S = 50 Msps, F_{IN} = 25 MHz		1, 2, 6	7.0	7.2	–	Bits	
Signal to Noise Ratio	SNR	–	–	–	–	–	(2)
F_S = 1 Gsps, F_{IN} = 20 MHz		4	42	45	–	dB	
F_S = 1 Gsps, F_{IN} = 500 MHz		4	41	44	–	dB	
F_S = 1 Gsps, F_{IN} = 1000 MHz (–1 dBFs)		4	41	44	–	dB	
F_S = 50 Msps, F_{IN} = 25 MHz		1, 2, 6	44	45	–	dB	

Table 5-3. Electrical Specifications (Continued)

Parameter	Symbol	Test Level	Value			Unit	Note
			Min	Typ	Max		
Total Harmonic Distortion	THD	–	–	–	–	–	(2)
F_S = 1 Gsps, F_{IN} = 20 MHz		4	50	54	–	dB	
F_S = 1 Gsps, F_{IN} = 500 MHz		4	46	50	–	dB	
F_S = 1 Gsps, F_{IN} = 1000 MHz (–1 dBFs)		4	42	46	–	dB	
F_S = 50 Msps, F_{IN} = 25 MHz		1, 2, 6	46	45	–	dB	
Spurious Free Dynamic Range	SFDR	–	–	–	–	–	(2)
F_S = 1 Gsps, F_{IN} = 20 MHz		4	52	57	–	dBc	
F_S = 1 Gsps, F_{IN} = 500 MHz		4	47	52	–	dBc	
F_S = 1 Gsps, F_{IN} = 1000 MHz (–1 dBFs)		4	42	47	–	dBc	
F_S = 1 Gsps, F_{IN} = 1000 MHz (–3 dBFs)		4	45	50	–	dBc	
F_S = 50 Msps, F_{IN} = 25 MHz		1, 2, 6	40	54	–	dBc	
Two-tone Intermodulation Distortion	IMD	4	–	–	–	–	(2)
F_{IN1} = 489 MHz at F_S = 1 Gsps F_{IN2} = 490 MHz at F_S = 1 Gsps		–	–47	–52	–	dBc	
Switching Performance and Characteristics – *See Figure 5-1 and Figure 5-2 on page 10*							
Maximum clock frequency	F_S	–	1	–	1.4	Gsps	(14)
Minimum clock frequency	F_S	4	10	–	50	Msps	(15)
Minimum Clock pulse width (high)	TC1	4	0.280	0.500	50	ns	
Minimum Clock pulse width (low)	TC2	4	0.350	0.500	50	ns	
Aperture delay	T_A	4	100	+250	400	ps	(2)
Aperture uncertainty	Jitter	4	–	0.4	0.6	ps (rms)	(2)(5)
Data output delay	TDO	4	1150	1360	1660	ps	(2)(10)(11)(12)
Output rise/fall time for DATA (20% to 80%)	TR/TF	4	250	350	550	ps	(11)
Output rise/fall time for DATA READY (20% to 80%)	TR/TF	4	250	350	550	ps	(11)
Data ready output delay	TDR	4	1110	1320	1620	ps	(2)(10)(11)(12)
Data ready reset delay	TRDR	4	–	720	1000	ps	
Data to data ready – Clock low pulse width (See "Timing Diagrams" on page 10.)	TOD-TDR	4	0	40	80	ps	(9)(13)(14)
Data to data ready output delay (50% duty cycle) at 1 Gsps (See "Timing Diagrams" on page 10.)	TD1	4	420	460	500	ps	(2)(15)
Data pipeline delay	TPD	4		4		clock cycles	

Notes: 1. Differential output buffers are internally loaded by 75Ω resistors. Buffer bias current = 11 mA.

2. See “Definition of Terms” on page 49.
3. Histogram testing based on sampling of a 10 MHz sinewave at 50 Msps.
4. Output error amplitude < ± 4 lsb around correct code (including gain and offset error).
5. Maximum jitter value obtained for single-ended clock input on the JTS8388B die (chip on board): 200 fs. (500 fs expected on TS8388BG)
6. Digital output back termination options depicted in Application Notes.
7. With a typical value of TD = 465 ps, at 1 Gsps, the timing safety margin for the data storing using the ECLinPS 10E452 output registers from Freescale® is of ± 315 ps, equally shared before and after the rising edge of the Data Ready signals (DR, DRB).
8. The clock inputs may be indifferently entered in differential or single-ended, using ECL levels or 4 dBm typical power level into the 50Ω termination resistor of the inphase clock input. (4 dBm into 50Ω clock input correspond to 10 dBm power level for the clock generator.)
9. At 1 Gsps, 50/50 clock duty cycle, TC2 = 500 ps (TC1). TDR - TOD = –100 ps (typ) does not depend on the sampling rate.
10. Specified loading conditions for digital outputs:
    - 50Ω or 75Ω controlled impedance traces properly 50/75Ω terminated, or unterminated 75Ω controlled impedance traces.
    - Controlled impedance traces far end loaded by 1 standard ECLinPS register from Freescale. (that is: 10E452) (Typical input parasitic capacitance of 1.5 pF including package and ESD protections.)
11. Termination load parasitic capacitance derating values:
    - 50Ω or 75Ω controlled impedance traces properly 50/75Ω terminated: 60 ps/pF or 75 ps per additional ECLinPS load.
    - Unterminated (source terminated) 75Ω controlled impedance lines: 100 ps/pF or 150 ps per additional ECLinPS termination load.
12. Apply proper 50/75Ω impedance traces propagation time derating values: 6 ps/mm (155 ps/inch) for TSEV8388B Evaluation Board.
13. Values for TOD and TDR track each other over temperature, (1% variation for TOD-TDR per 100°C temperature variation). Therefore TOD-TDR variation over temperature is negligible. Moreover, the internal (on-chip) and package skews between each Data TODs and TDR effect can be considered as negligible. Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values (see Advanced Application Notes about “TOD-TDR Variation Over Temperature” on page 28).
14. Min value guarantees performance. Max value guarantees functionality.
15. Min value guarantees functionality. Max value guarantees performance.

5.4 Timing Diagrams

Figure 5-1. TS8388B Timing Diagram (1 Gsps Clock Rate), Data Ready Reset, Clock Held at *Low* Level

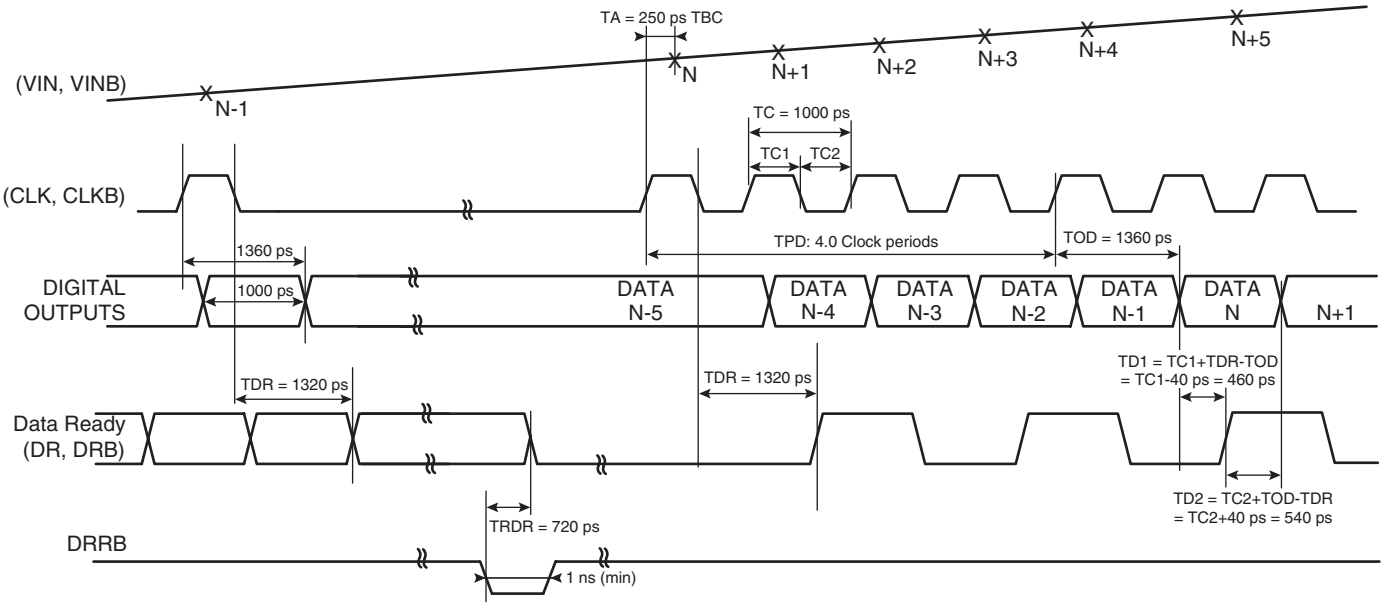
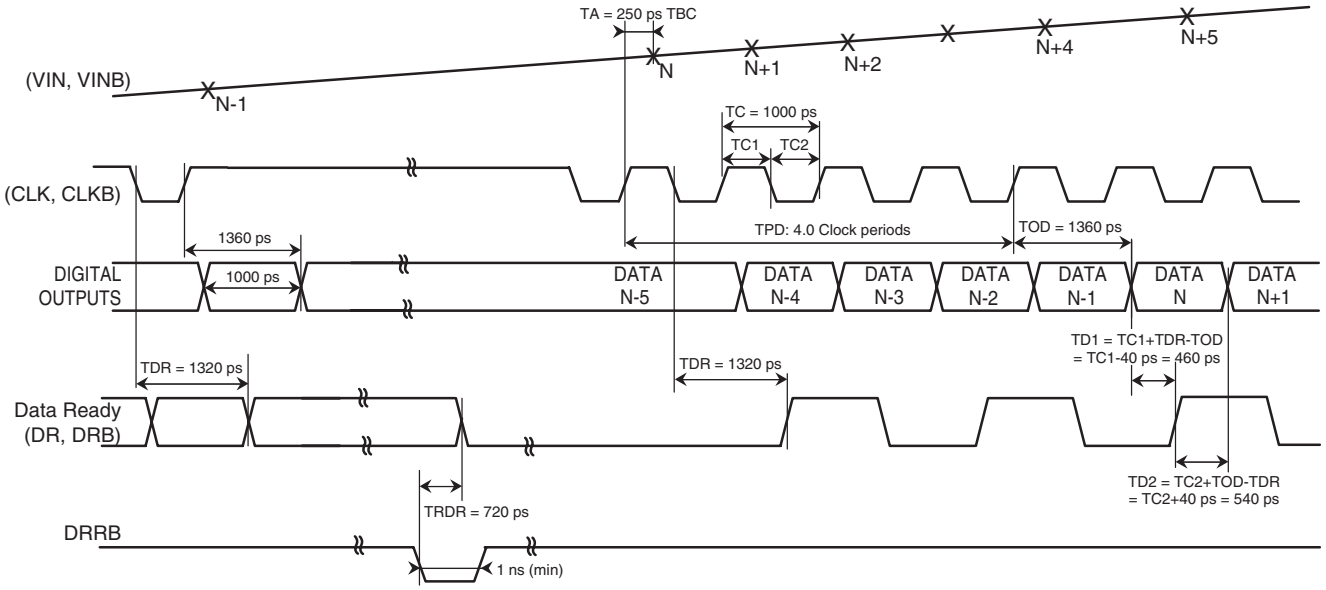


Figure 5-2. TS8388B Timing Diagram (1 Gsps Clock Rate), Data Ready Reset, Clock Held at *High* Level



5.5 Explanation of Test Levels

Table 5-4. Explanation of Test Levels

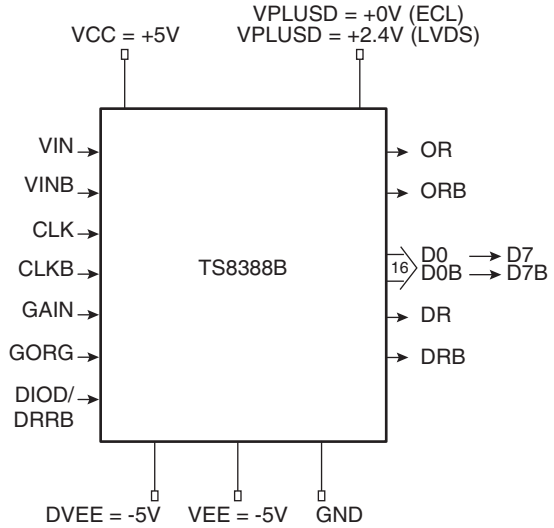
No.	Characteristics
1	100% production tested at +25°C(1) (for “C” Temperature range(2)).
2	100% production tested at +25°C(1), and sample tested at specified temperatures (for “V” and “M” Temperature range(2)).
3	Sample tested only at specified temperatures.
4	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
5	Parameter is a typical value only.
6	100% production tested over specified temperature range (for “B/Q” Temperature range(2)).

Notes: 1. Unless otherwise specified, all tests are pulsed tests: therefore $T_J = Tc = T_{amb}$, where T_J, Tc and T_A are junction, case and ambient temperature respectively.
2. Refer to “Ordering Information” on page 52.
3. Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

5.6 Functions Description

Table 5-5. Functions Description

Name	Function
V_{CC}	Positive power supply
V_{EE}	Analog negative power supply
V_{PLUSD}	Digital positive power supply
GND	Ground
V_{IN}, V_{INB}	Differential analog inputs
CLK, CLKB	Differential clock inputs
<D0:D7> <D0B:D7B>	Differential output data port
DR, DRB	Differential data ready outputs
OR, ORB	Out-of-range outputs
GAIN	ADC gain adjust
GORB	Gray or Binary digital output select
DIOD/DRRB	Die junction temperature measurement/ asynchronous data ready reset



5.7 Digital Output Coding

NRZ (Non Return to Zero) mode, ideal coding: does not include gain, offset, and linearity voltage errors.

Table 5-6. Digital Output Coding

Differential Analog Input	Voltage Level	Digital Output		Out-of Range
		Binary GORB = VCC or Floating	Gray GORB = GND	
> +251 mV	> Positive full scale + 1/2 lsb	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1
+251 mV +249 mV	Positive full scale + 1/2 lsb Positive full scale – 1/2 lsb	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1	0 0
+126 mV +124 mV	Positive 1/2 scale + 1/2 lsb Positive 1/2 scale – 1/2 lsb	1 1 0 0 0 0 0 0 1 0 1 1 1 1 1 1	1 0 1 0 0 0 0 0 1 1 1 0 0 0 0 0	0 0
+1 mV –1 mV	Bipolar zero + 1/2 lsb Bipolar zero – 1/2 lsb	1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1	1 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0	0 0
–124 mV –126 mV	Negative 1/2 scale + 1/2 lsb Negative 1/2 scale – 1/2 lsb	0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 1 1 0 0 0 0 0 0 0 1 0 0 0 0 0	0 0
–249 mV –251 mV	Negative full scale + 1/2 lsb Negative full scale – 1/2 lsb	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0
< –251 mV	< Negative full scale – 1/2 lsb	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1

6. Package Description

6.1 Pin Description

Table 6-1. TS8388BGL Pin Description (CBGA68 Package)

Symbol	Pin number	Function
GND	A2, A5, B1, B5, B10, C2, D2, E1, E2, E11, F1, F2, G11, K2, K3, K4, K5, K10, L2, L5	Ground pins. To be connected to external ground plane.
V_{CC}	A4, A6, B2, B4, B6, H1, H2, L6, L7	+5V positive supply.
V_{EE}	A3, B3, G1, G2, J1, J2	5V analog negative supply.
DV_{EE}	F10, F11	–5V digital negative supply.
V_{IN}	L3	In phase (+) analog input signal of the Sample and Hold differential preamplifier.
V_{INB}	L4	Inverted phase (-) of ECL clock input signal (CLK).
CLK	C1	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	D1	Inverted phase (-) of ECL clock input signal (CLK).
B0, B1, B2, B3, B4, B5, B6, B7	A8, A9, A10, D10, H11, J11, K9, K8	In phase (+) digital outputs. B0 is the LSB. B7 is the MSB.

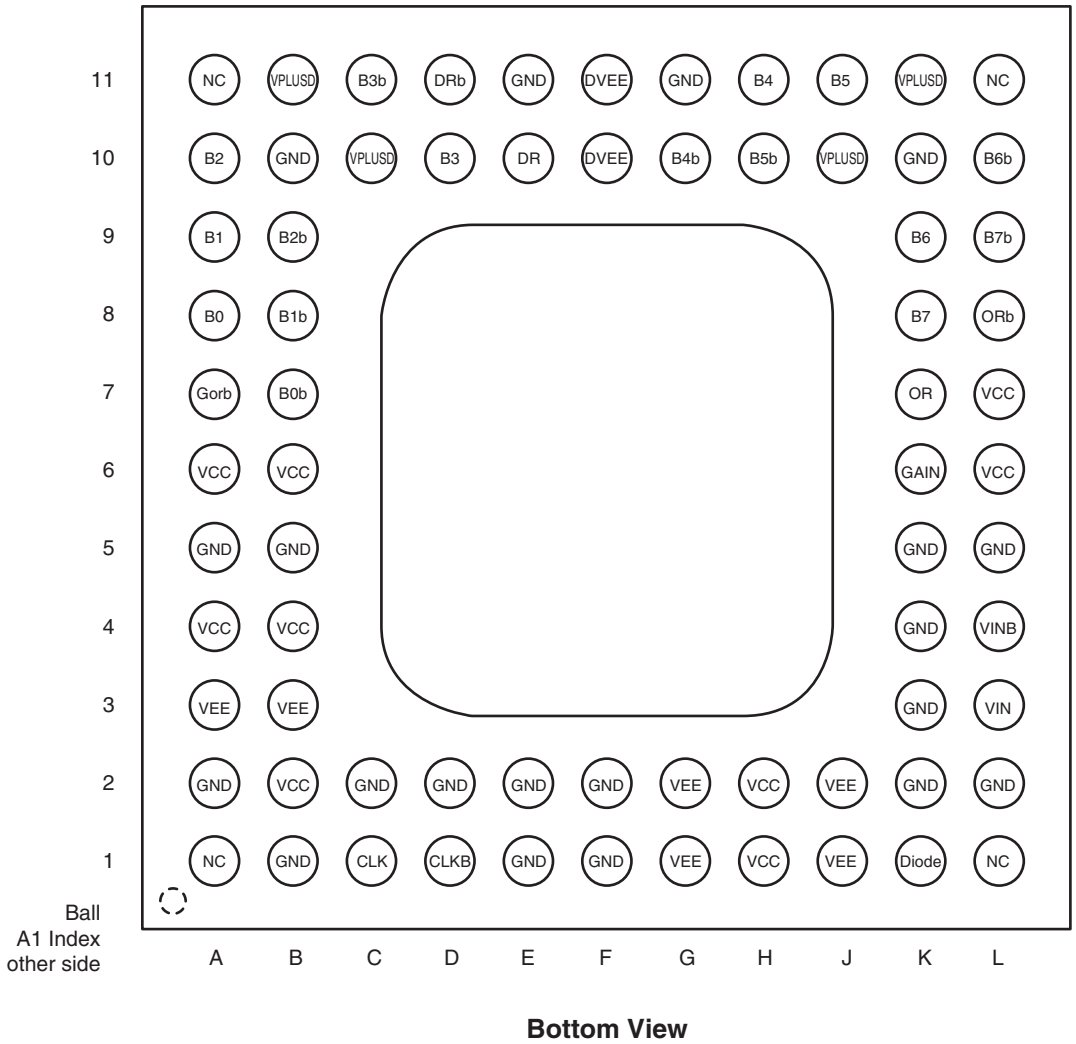
Table 6-1. TS8388BGL Pin Description (CBGA68 Package)

Symbol	Pin number	Function
B0B, B1B, B2B, B3B, B4B, B5B, B6B, B7B	B7, B8, B9, C11, G10, H10, L10, L9	Inverted phase (-) digital outputs. B0B is the inverted LSB. B7B is the inverted MSB.
OR	K7	In phase (+) out-of-range bit. Out of Range is high on the leading edge of code 0 and code 256.
ORB	L8	Inverted phase (+) out-of-range bit (OR).
DR	E10	In phase (+) output of Data Ready Signal.
DRB	D11	Inverted phase (-) output of Data Ready Signal (DR).
GORB	A7	Gray or Binary select output format control pin. - Binary output format if GORB is floating or V_{CC}. - Gray output format if GORB is connected at ground (0V).
GAIN	K6	ADC gain adjust pin. The gain pin is by default grounded, the ADC gain transfer function is nominally close to one.
DIOD/DRRB	K1	Die function temperature measurement pin and asynchronous data ready reset active low, single-ended ECL input.
V_{PLUSD}	B11, C10, J10, K11	+2.4V for LVDS output levels otherwise to GND(2).
NC	A1, A11, L1, L11	Not connected.

Note: 1. The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

6.2 TS8388BGL Pinout

Figure 6-1. TS8388BGL Pinout of CBGA 68 Package



Bottom View

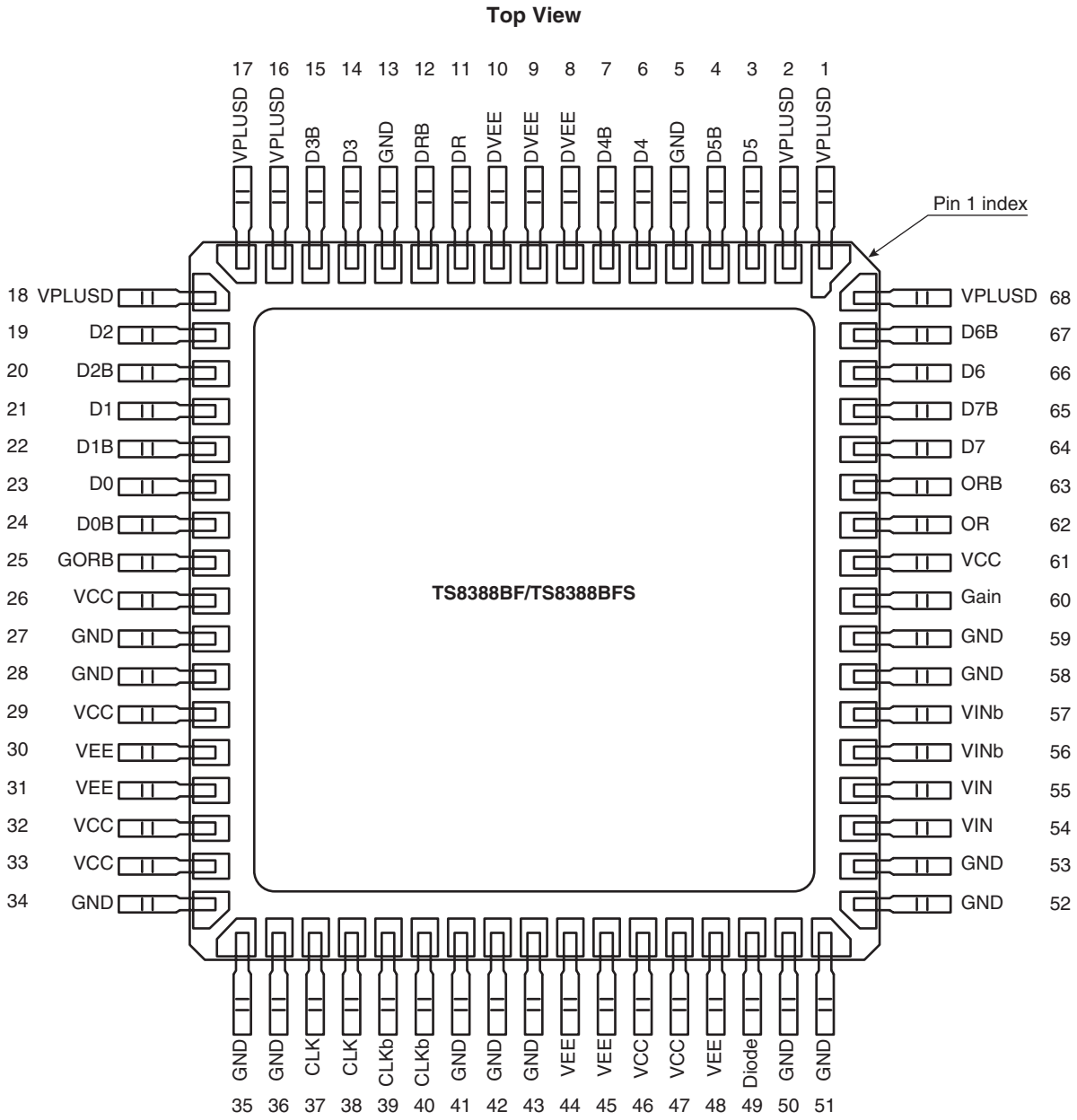
Table 6-2. TS8388BF/TS8388BFS Pin Description (CQFP68 Package)

Symbol	Pin number	Function
GND	5, 13, 27, 28, 34, 35, 36, 41, 42, 43, 50, 51, 52, 53, 58, 59	Ground pins. To be connected to external ground plane.
V_{PLUSD}	1, 2, 16, 17, 18, 68	Digital positive supply (0V for ECL compatibility, 2.4V for LVDS compatibility).(2)
V_{CC}	26, 29, 32, 33, 46, 47, 61	+5V positive supply.
V_{EE}	30, 31, 44, 45, 48	–5V analog negative supply.
DV_{EE}	8, 9, 10	–5V digital negative supply.
V_{IN}	54(1), 55	In phase (+) analog input signal of the Sample and Hold differential preamplifier.
V_{INB}	56, 57(1)	Inverted phase (-) of analog input signal (V_{IN}).
CLK	37(1), 38	In phase (+) ECL clock input signal. The analog input is sampled and held on the rising edge of the CLK signal.
CLKB	39, 40(1)	Inverted phase (-) of ECL clock input signal (CLK).
D0, D1, D2, D3, D4, D5, D6, D7	23, 21, 19, 14, 6, 3, 66, 64	In phase (+) digital outputs. B0 is the LSB. B7 is the MSB.
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B	24, 22, 20, 15, 7, 4, 67, 65	Inverted phase (-) digital outputs. B0B is the inverted LSB. B7B is the inverted MSB.
OR	62	In phase (+) out-of-range bit. Out of Range is high on the leading edge of code 0 and code 256.
ORB	63	Inverted phase (+) out-of-range bit (OR).
DR	11	In phase (+) output of Data Ready Signal.
DRB	12	Inverted phase (-) output of Data Ready Signal (DR).
GORB	25	Gray or Binary select output format control pin. - Binary output format if GORB is floating or V_{CC}. - Gray output format if GORB is connected at ground (0V).
GAIN	60	ADC gain adjust pin.
DIOD/DRRB	49	This pin has a double function (can be left open or grounded if not used): - DIOD: die junction temperature monitoring pin. - DRRB: asynchronous data ready reset function.

Notes:
1. Following pin numbers 37 (CLK), 40 (CLKB), 54 (V_{IN}) and 57 (V_{INB}) have to be connected to GND through a 50Ω resistor as close as possible to the package (50Ω termination preferred option).
2. The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the same proportion in order to spare power dissipation.

6.3 TS8388BF/TS8388BFS Pinout

Figure 6-2. TS8388BF/TS8388BFS Pinout of CQFP68 Package

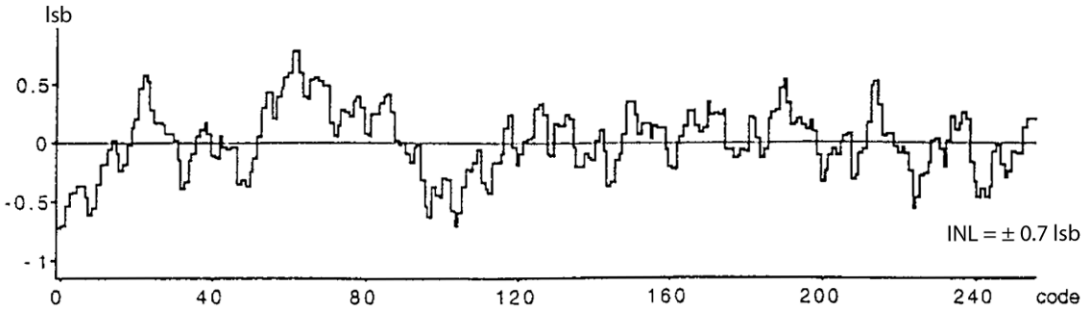


7. Typical Characterization Results

7.1 Static Linearity

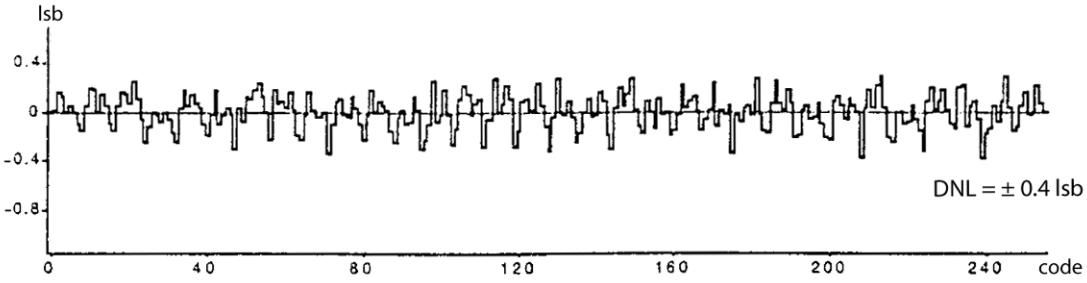
F_S = 50 Msps/F_{IN} = 10 MHz

Figure 7-1. Integral Non-Linearity



Note: Clock Frequency = 50 Msps; Signal Frequency = 10 MHz.
Positive peak: 0.78 lsb; Negative peak: –0.73 lsb.

Figure 7-2. Differential Non-Linearity



Note: Clock Frequency = 50 Msps; Signal Frequency = 10 MHz.
Positive peak: 0.3 lsb; Negative peak: –0.39 lsb.

7.2 Effective Number of Bits vs. Power Supplies Variation

Figure 7-3. Effective Number of Bits = f (V_{EEA}); F_S = 500 Msps; F_{IN} = 100 MHz

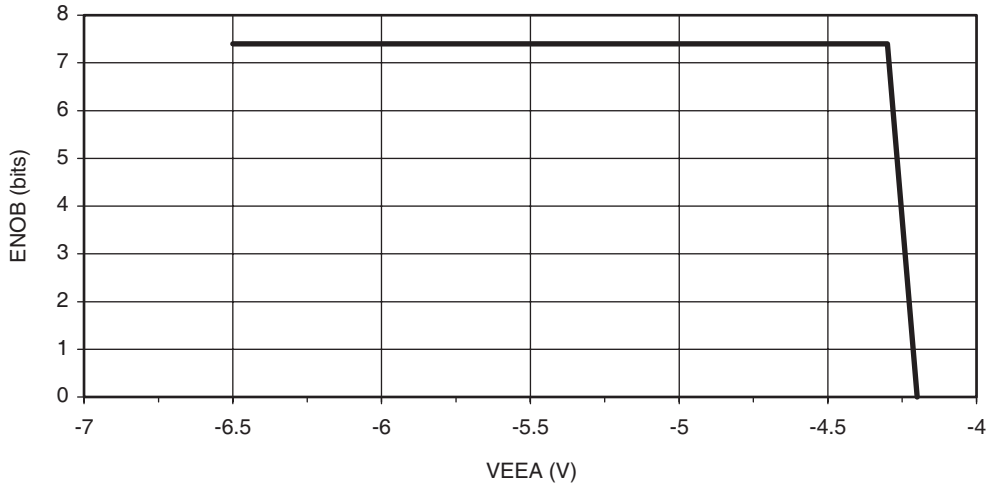


Figure 7-4. Effective Number of Bits = f (V_{CC}); F_S = 500 Msps; F_{IN} = 100 MHz

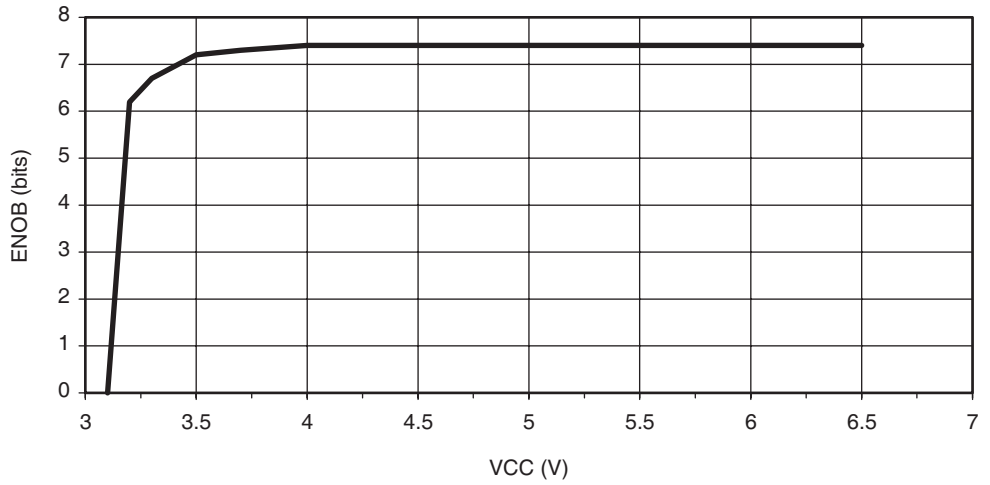
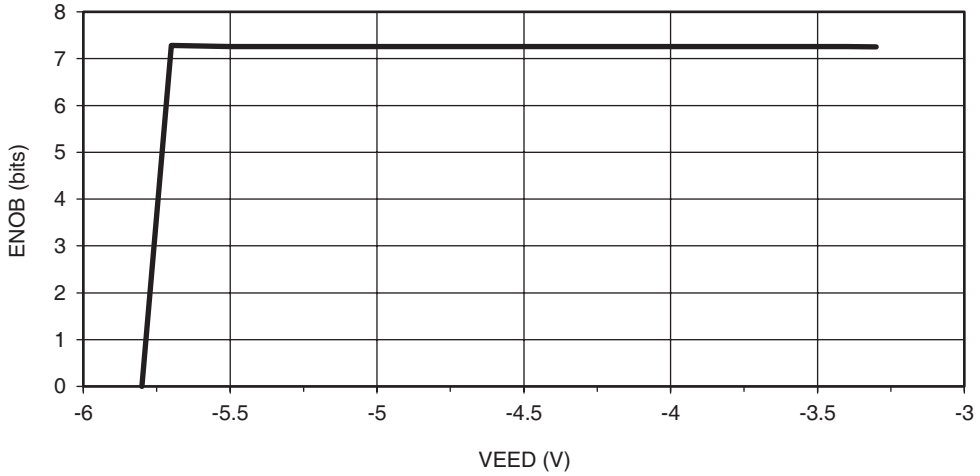
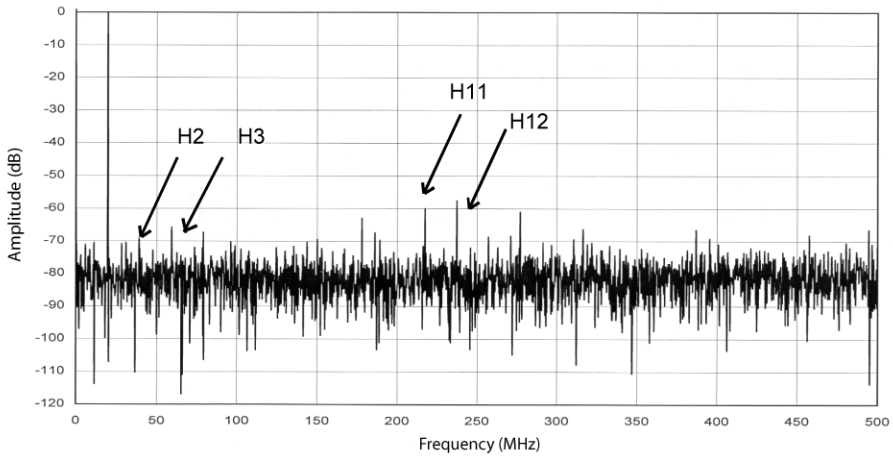


Figure 7-5. Effective Number of Bits = f (V_{EED}); F_S = 500 Msps; F_{IN} = 100 MHz



7.3 Typical FFT Results

Figure 7-6. F_S = 1 Gsps; F_{IN} = 20 MHz



Single Ended or differential

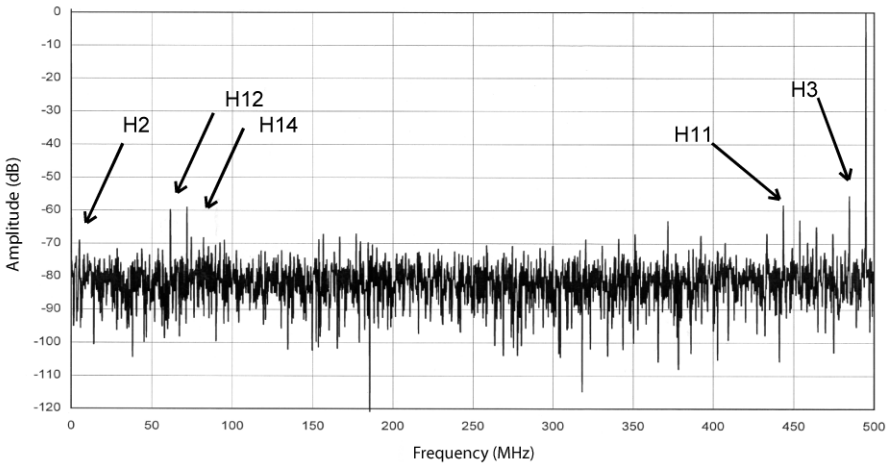
Fs =1 GSPS
Fin = 20 MHz

Eff. Bits =7.2
SINAD = 44.3 dB
SNR = 44.7dB
THD = -54dBc
SFDR = -57 dBc

Binary output coding

clock duty cycle = 50 %

Figure 7-7. F_S = 1 Gsps; F_{IN} = 495 MHz



Single Ended or differential

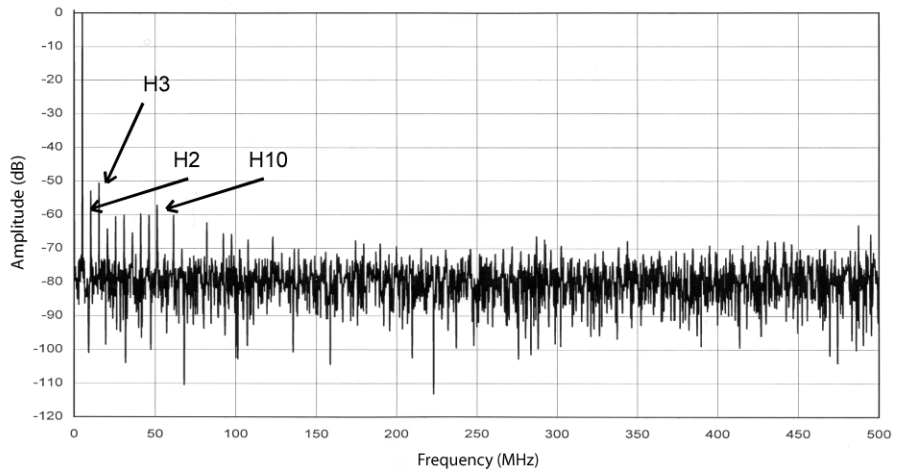
Fs =1 GSPS
Fin=495MHz

Eff. Bits =6.8
SINAD =43 dB
SNR = 44.1 dB
THD = -50 dBc
SFDR= -52 dBc

Binary output coding

clock duty cycle = 50 %

Figure 7-8. F_S = 1 Gsps; F_{IN} = 995 MHz (–3 dB Full Scale Input)



Single Ended or differential

Fs =1 GSPS
Fin=995 MHz

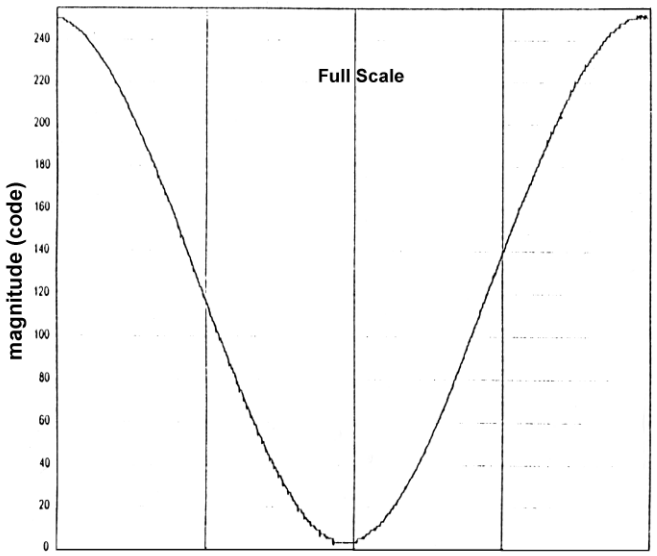
Eff. Bits =6.6
SINAD =40.8 dB
SNR = 44 dB
THD = -48 dBc
SFDR= -50 dBc

Binary output coding

clock duty cycle = 50 %

7.4 Spurious Free Dynamic Range vs. Input Amplitude

Figure 7-9. Sampling Frequency: F_S = 1 Gsps; Input Frequency F_{IN} = 995 MHz; Full Scale; ENOB = 6.4; SINAD = 40 dB; SNR = 44 dB; THD = –46 dBc; SFDR = –47 dBc; Gray or Binary Output Coding



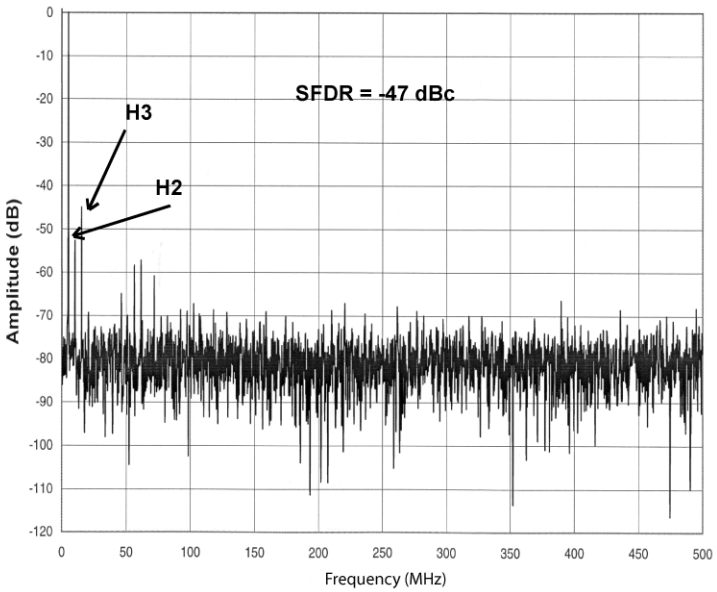
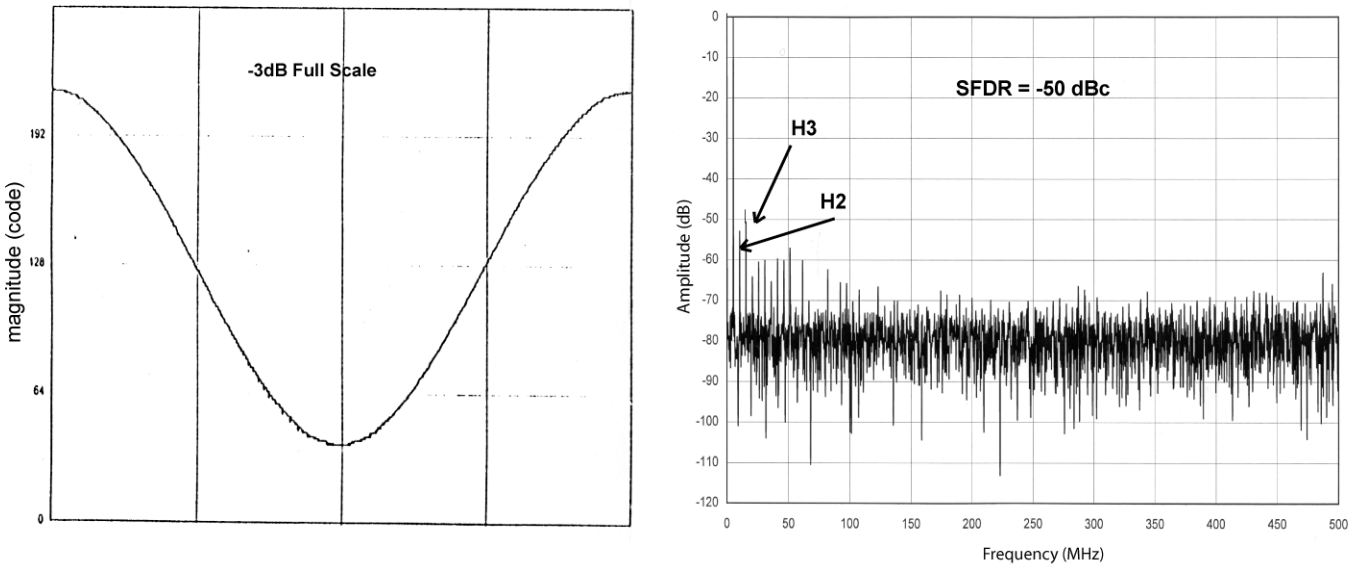


Figure 7-10. Sampling Frequency: F_S = 1 Gsps; Input Frequency F_{IN} = 995 MHz; –3 dB Full Scale; ENOB = 6.6; SINAD = 40.8 dB; SNR = 44 dB; THD = –48 dBc; SFDR = –50 dBc; Gray or Binary Output Coding



7.5 Dynamic Performance vs. Analog Input Frequency

F_S = 1 Gsps, F_{IN} = 0 up to 1600 MHz, Full Scale input (F_S), F_S –3 dB

Clock duty cycle 50/50, Binary/Gray output coding, fully differential or single-ended analog and clock inputs.

Figure 7-11. ENOB (dB)

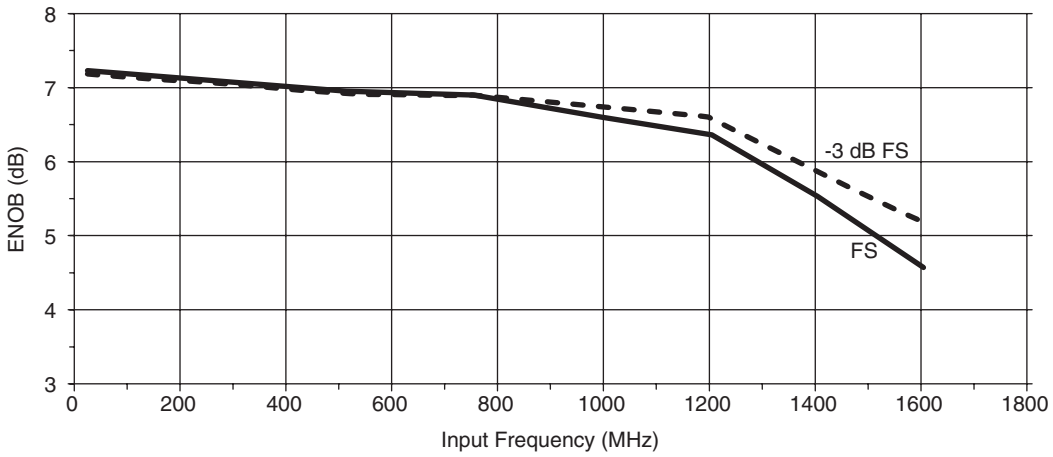


Figure 7-12. SNR (dB)

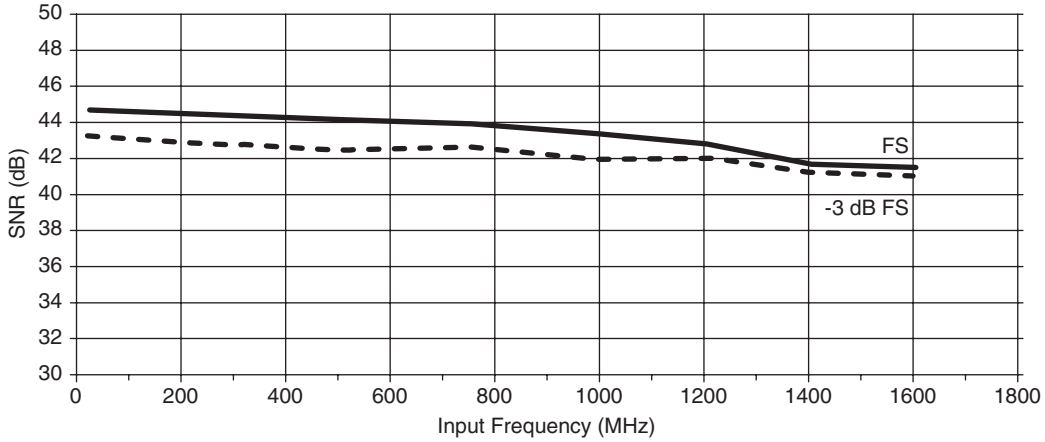
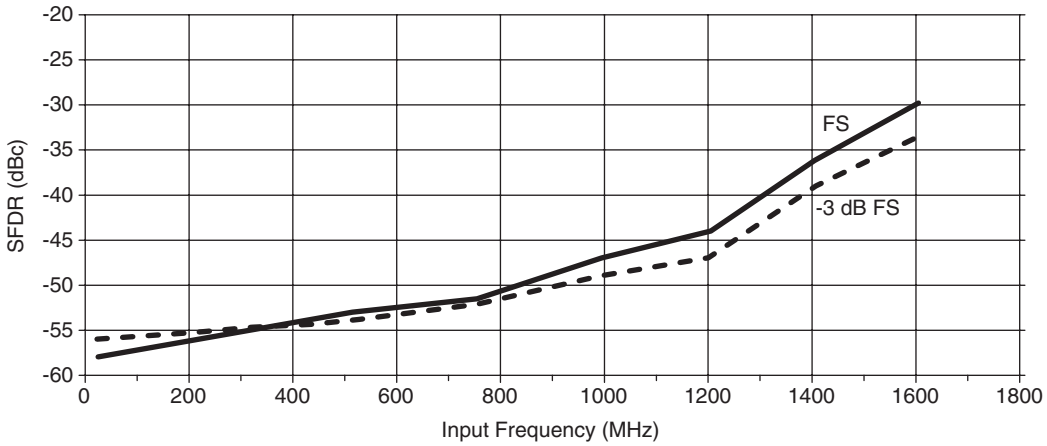


Figure 7-13. SFDR (dBc)

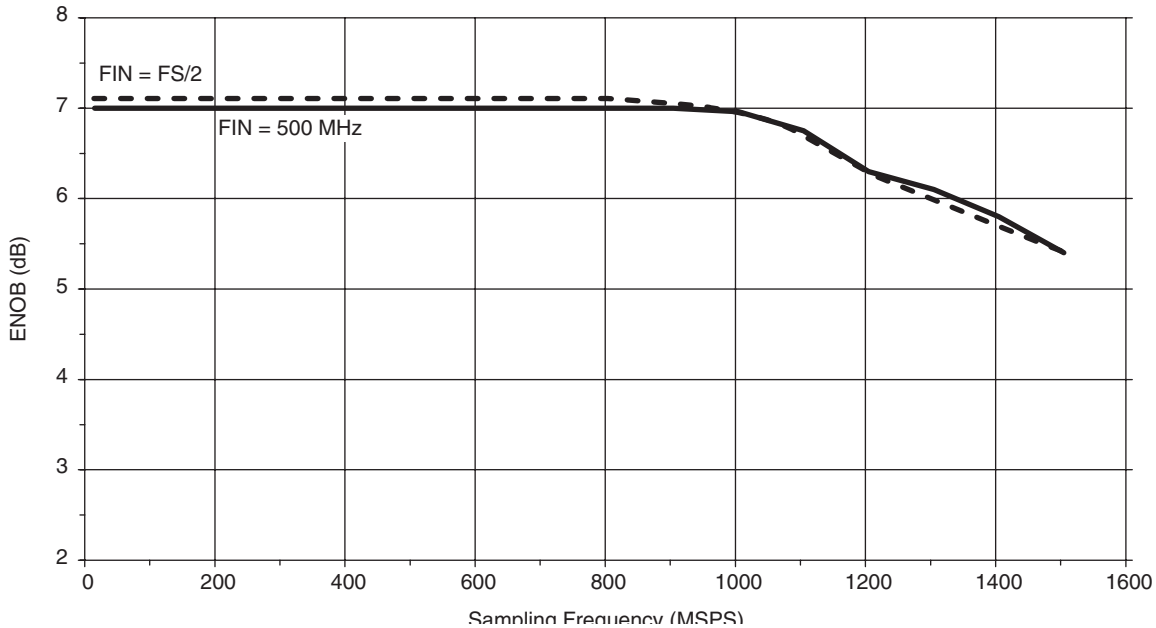


7.6 Effective Number of Bits (ENOB) vs. Sampling Frequency

Analog Input Frequency: F_{IN} = 495 MHz and Nyquist conditions ($F_{IN} = F_S/2$)

Clock duty cycle 50/50, Binary output coding

Figure 7-14. ENOB (dB)

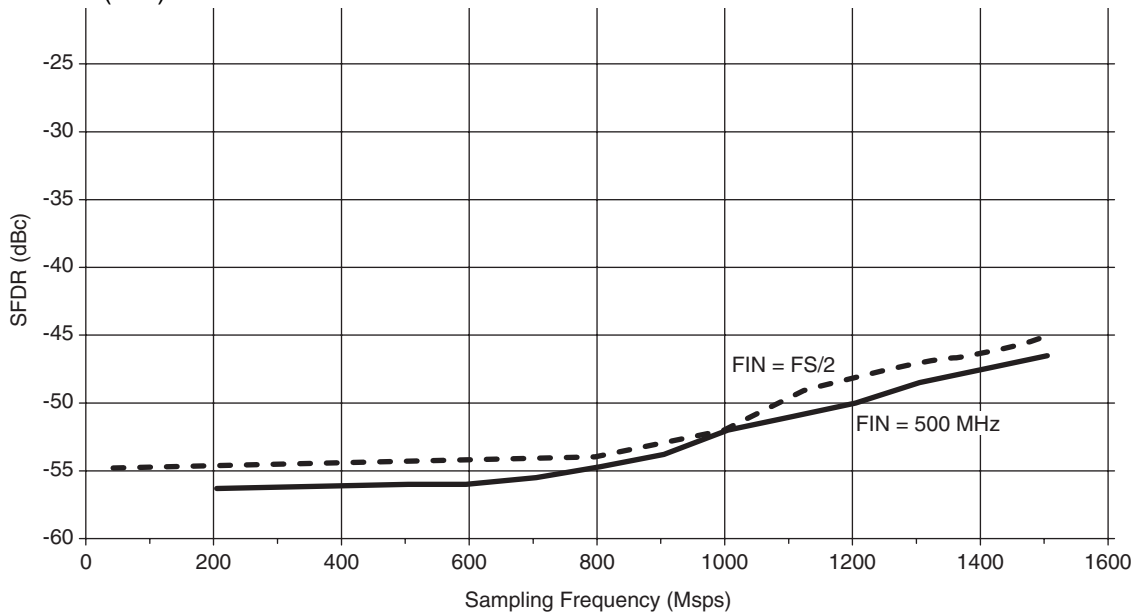


7.7 SFDR vs. Sampling Frequency

Analog Input Frequency: F_{IN} = 495 MHz and Nyquist conditions ($F_{IN} = F_S/2$)

Clock duty cycle 50/50, Binary output coding

Figure 7-15. SFDR (dBc)



7.8 TS8388B ADC Performances vs. Junction Temperature

Figure 7-16. Effective Number of Bits vs. Junction Temperature
F_S = 1 Gsps; F_{IN} = 500 MHz; Duty Cycle = 50%

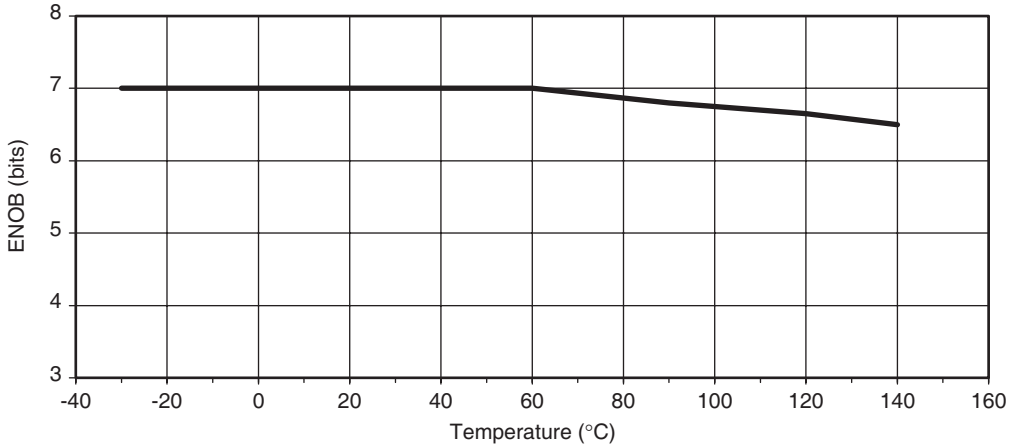


Figure 7-17. Signal to Noise Ratio vs. Junction Temperature
F_S = 1 Gsps; F_{IN} = 507 MHz; Differential Clock; Single-ended Analog Input (V_{IN} = –1 dBFs)

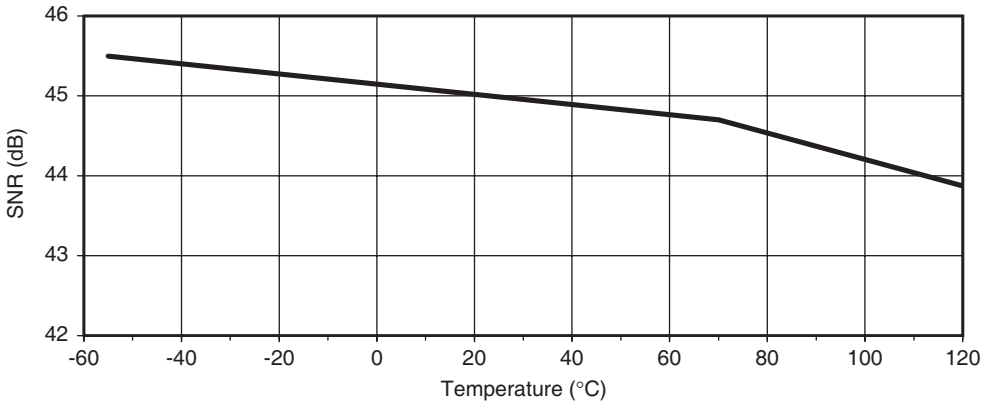


Figure 7-18. Total Harmonic Distortion vs. Junction Temperature
F_S = 1 Gsps; F_{IN} = 507 MHz; Differential Clock; Single-ended Analog Input (V_{IN} = –1 dBFs)

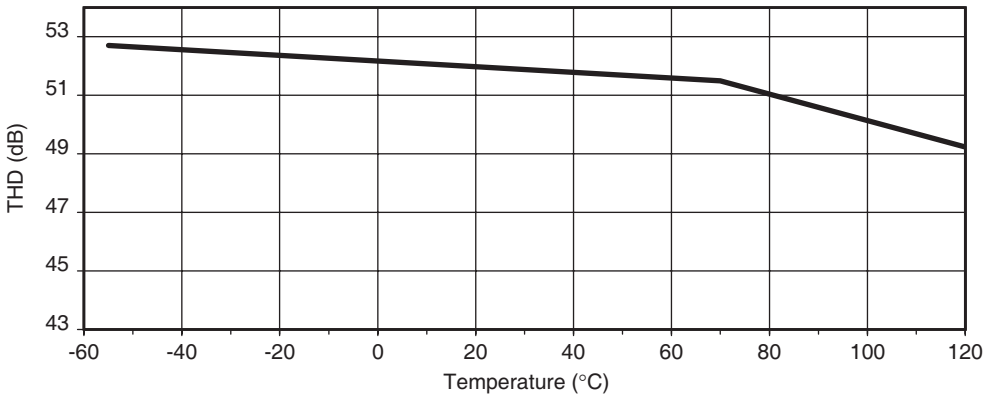
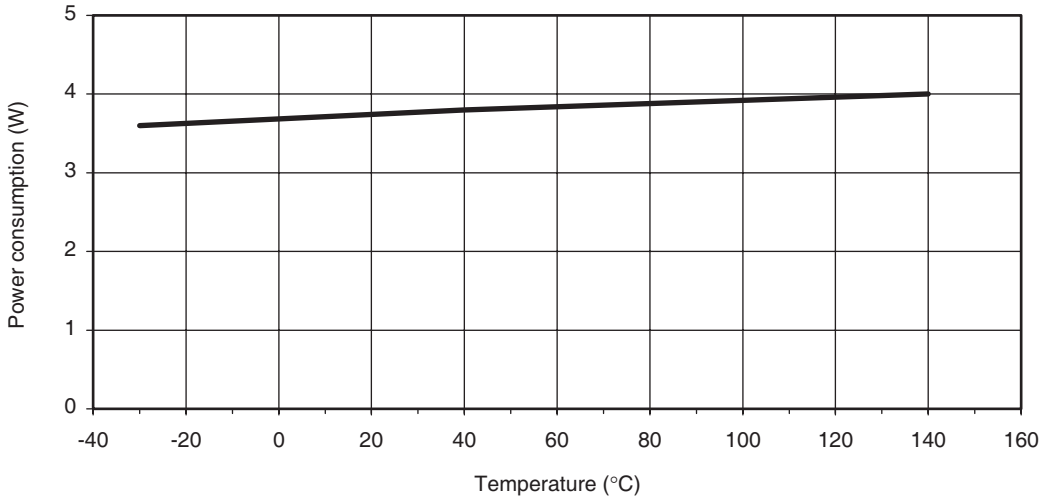


Figure 7-19. Power Consumption vs. Junction Temperature, F_S = 1 Gsps; F_{IN} = 500 MHz; Duty Cycle = 50%



7.9 Typical Full Power Input Bandwidth

Figure 7-20. 1.8 GHz at –3 dB (–2 dBm Full Power Input) – CBGA68 Package

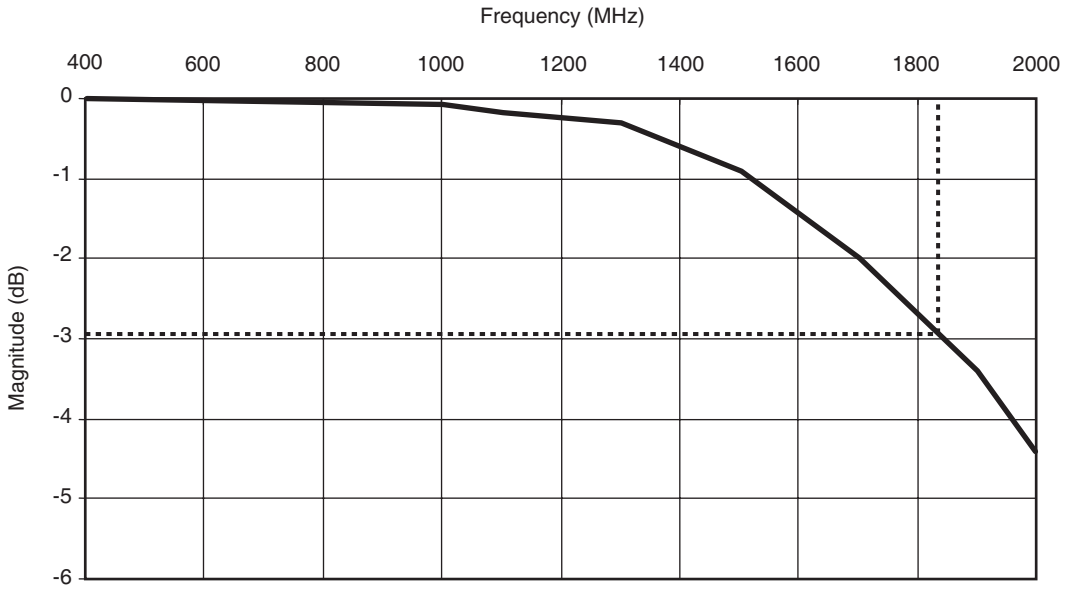
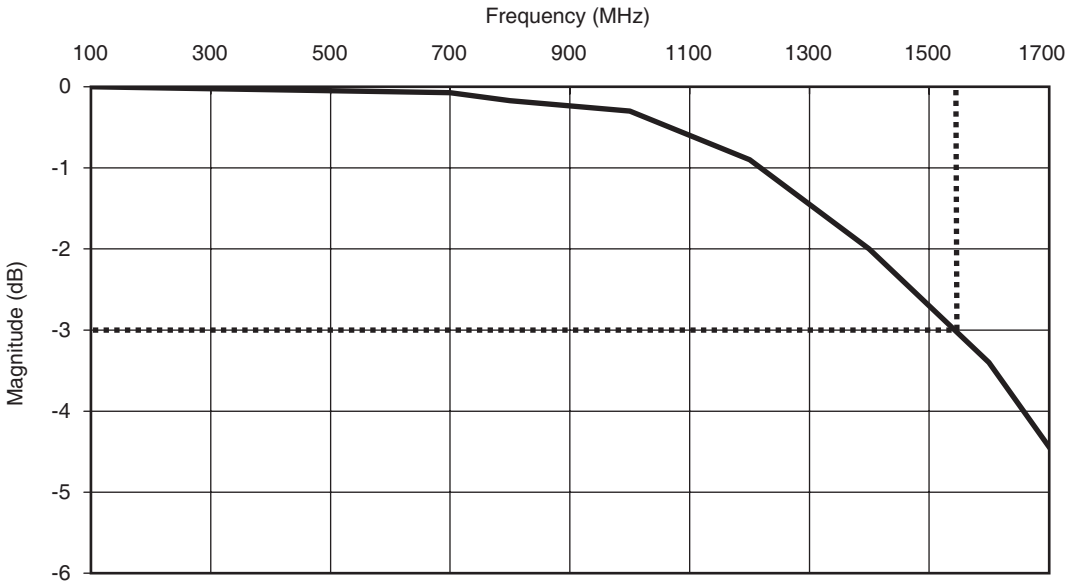


Figure 7-21. 1.5 GHz at –3 dB (–2 dBm Full Power Input) – CQFP68 Package



7.10 ADC Step Response

Test pulse input characteristics: 20% to 80% input full scale and rise time ~ 200 ps.

Note: This step response was obtained with the TSEV8388B chip on-board (device in die form).

Figure 7-22. Test Pulse Digitized with 20 GHz DSO

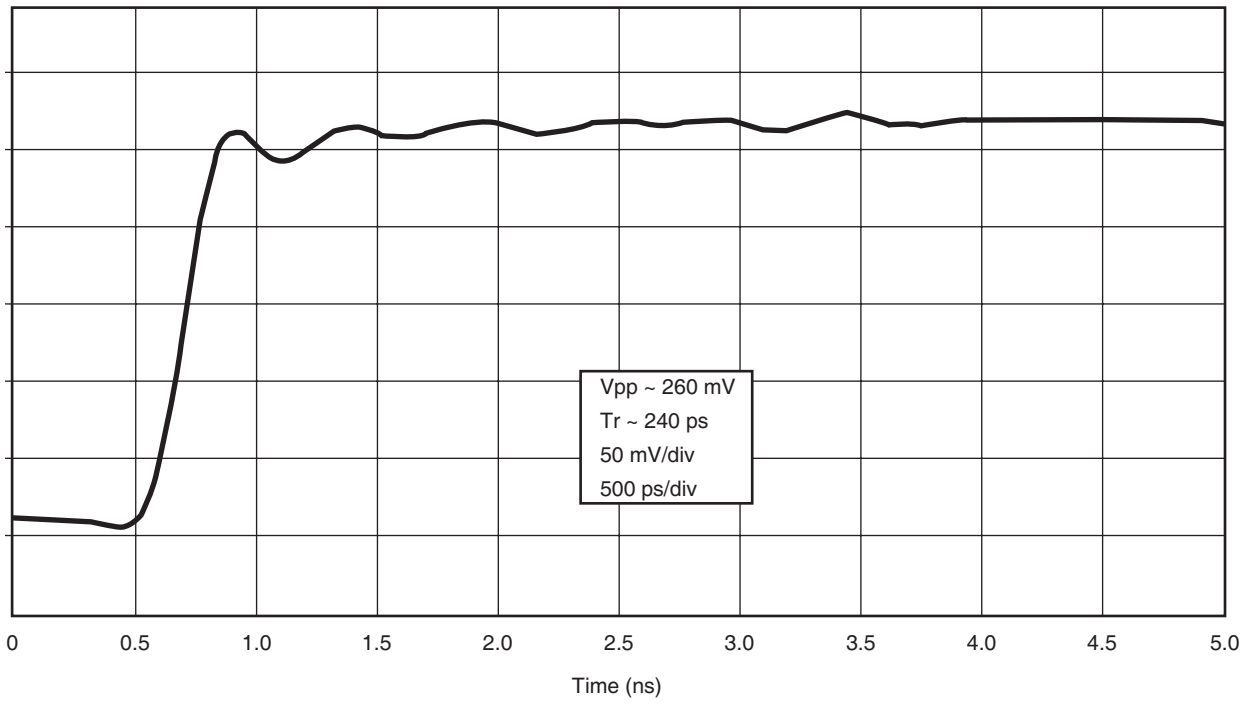
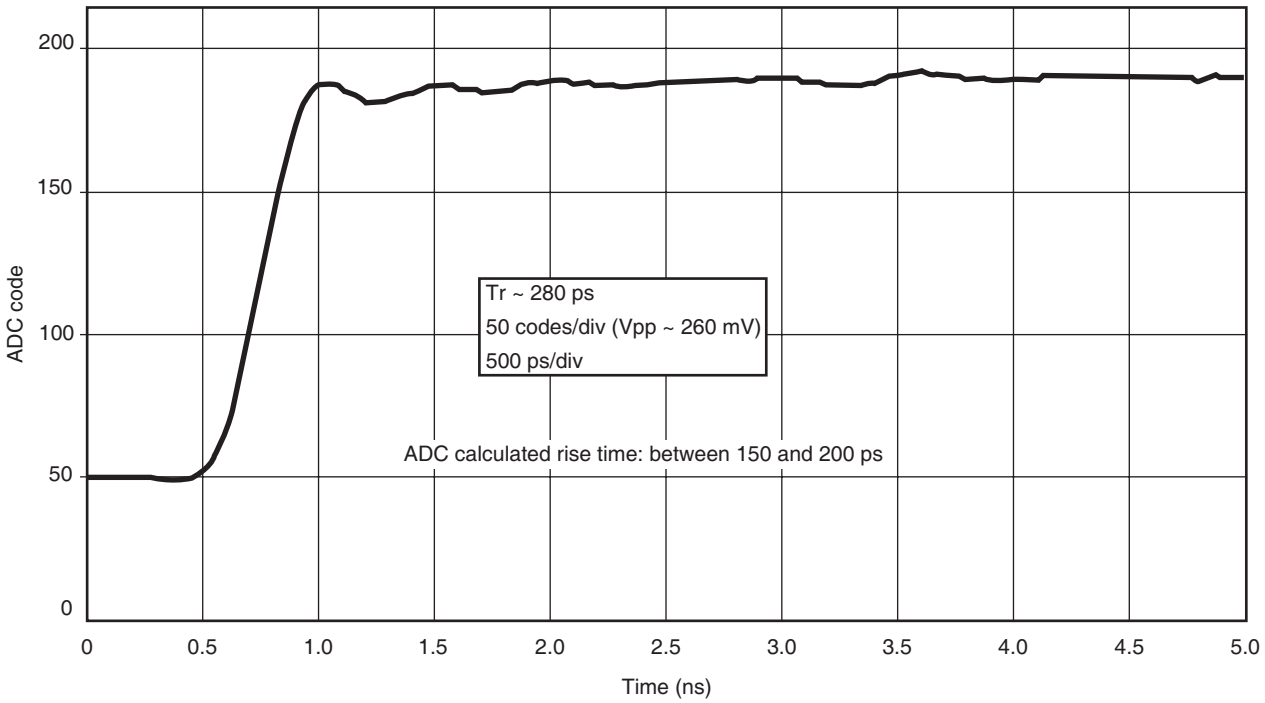


Figure 7-23. Same Test Pulse Digitized with TS8388B ADC



Note: Ripples are due to the test setup (they are present on both measurements).

8. TS8388B Main Features

8.1 Timing Information

8.1.1 Timing Value for TS8388B

Timing values as defined in Table 5-3 on page 4 are advanced data, issued from electric simulations and first characterizations results fitted with measurements.

Timing values are given at package inputs/outputs, taking into account package internal controlled impedance traces propagation delays, gullwing pin model, and specified termination loads.
Propagation delays in 50/75Ω impedance traces are not taken into account for TOD and TDR.
Apply proper derating values corresponding to termination topology.

The min/max timing values are valid over the full temperature range in the following conditions:

- Specified Termination Load (Differential output Data and Data Ready):
  50Ω resistor in parallel with 1 standard ECLinPS register from Freescale (that is: 10E452)
  Typical ECLinPS inputs shows a typical input capacitance of 1.5 pF (including package and ESD protections).
  If addressing an output DMUX, take care if some Digital outputs do not have the same termination load and apply corresponding derating value given below.
- Output Termination Load derating values for TOD and TDR:
  ~ 35 ps/pF or 50 ps per additional ECLinPS load.
- Propagation time delay derating values have also to be applied for TOD and TDR:
  ~ 6 ps/mm (155 ps/inch) for TSEV8388B Evaluation Board.
  Apply proper time delay derating value if a different dielectric layer is used.

8.1.2 Propagation Time Considerations

TOD and TDR Timing values are given from pin to pin and *do not* include the additional propagation times between device pins and input/output termination loads. For the TSEV8388B Evaluation Board, the propagation time delay is 6 ps/mm (155 ps/inch) corresponding to 3.4 (at 10 GHz) dielectric constant of the RO4003 used for the board.

If a different dielectric layer is used (for instance Teflon), please use appropriate propagation time values.

TD does *not* depend on propagation times because it is a differential data (TD is the time difference between data ready output delay and digital data output delay).

TD is also the most straightforward data to measure, again because it is differential: TD can be measured directly onto termination loads, with matched oscilloscopes probes.

8.1.3 TOD-TDR Variation Over Temperature

Values for TOD and TDR track each other over temperature (1% variation for TOD-TDR per 100°C temperature variation).

Therefore TOD-TDR variation over temperature is negligible. Moreover, the internal (on-chip) and package skews between each Data TODs and TDR effect can be considered as negligible.

Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values.

In other terms:

– If TOD is at 1150 ps, TDR will not be at 1620 ps (maximum time delay for TDR).

– If TOD is at 1660 ps, TDR will not be at 1110 ps (minimum time delay for TDR). However, external TOD-TDR values may be dictated by total digital data skews between every TODs (each digital data) and TDR: MCM Board, bonding wires and output lines lengths differences, and output termination impedance mismatches.

The external (on board) skew effect has NOT been taken into account for the specification of the minimum and maximum values for TOD-TDR.

8.1.4 Principle of Operation

The Analog input is sampled on the rising edge of external clock input (CLK, CLKB) after TA (aperture delay) of typically 250 ps. The digitized data is available after 4 clock periods latency (pipeline delay (TPD)), on clock rising edge, after 1360 ps typical propagation delay TOD.

The Data Ready differential output signal frequency (DR, DRB) is half the external clock frequency, that is it switches at the same rate as the digital outputs.

The Data Ready output signal (DR, DRB) switches on external clock falling edge after a propagation delay TDR of typically 1320 ps.

A Master Asynchronous Reset input command DRRB (ECL compatible single-ended input) is available for initializing the differential Data Ready output signal (DR, DRB). This feature is mandatory in certain applications using interleaved ADCs or using a single ADC with demultiplexed outputs. Actually, without Data Ready signal initialization, it is impossible to store the output digital data in a defined order.

8.2 Principle of Data Ready Signal Control by DRRB Input Command

8.2.1 Data Ready Output Signal Reset

The Data Ready signal is reset on falling edge of DRRB input command, on ECL logical low level (–1.8V). DRRB may also be tied to V_{EE} = -5V for Data Ready output signal Master Reset. So long DRRB remains at logical low level, (or tied to V_{EE} = -5V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.

The Data Ready output signal (DR, DRB) is reset to logical zero after TRDR = 920 ps typical.

TRDR is measured between the -1.3V point of the falling edge of DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data Ready Reset command may be a pulse of 1 ns minimum time width.

8.2.2 Data Ready Output Signal Restart

The Data Ready output signal restarts on DRRB command rising edge, ECL logical high levels (-0.8V). DRRB may also be Grounded, or is allowed to float, for normal free running Data Ready output signal.

The Data Ready signal restart sequence depends on the logical level of the external encoding clock, at DRRB rising edge instant:

- The DRRB rising edge occurs when external encoding clock input (CLK, CLKB) is LOW: The Data Ready output first rising edge occurs after half a clock period on the clock falling edge, after a delay time TDR = 1320 ps already defined here above.
- The DRRB rising edge occurs when external encoding clock input (CLK, CLKB) is HIGH: The Data Ready output first rising edge occurs after one clock period on the clock falling edge, and a delay TDR = 1320 ps.

Consequently, as the analog input is sampled on clock rising edge, the first digitized data corresponding to the first acquisition (N) after Data Ready signal restart (rising edge) is always strobed by the third rising edge of the data ready signal.

The time delay (TD1) is specified between the last point of a change in the differential output data (zero crossing point) to the rising or falling edge of the differential Data Ready signal (DR, DRB) (zero crossing point).

For normal initialization of Data Ready output signal, the external encoding clock signal frequency and level must be controlled. It is reminded that the minimum encoding clock sampling rate for the ADC is 10 Msps and consequently the clock cannot be stopped.

One single pin is used for both DRRB input command and die junction temperature monitoring. Pin denomination will be DRRB/DIOD. On the former version denomination was DIOD. Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

8.3 Analog Inputs (V_{IN}) (V_{INB})

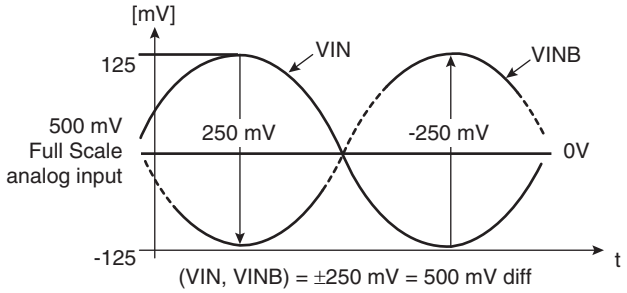
The analog input Full Scale range is 0.5V peak to peak (Vpp), or –2 dBm into the 50Ω termination resistor.

In differential mode input configuration, that means 0.25V on each input, or ±125 mV around 0V. The input common mode is *ground*.

The typical input capacitance is 3 pF for TS8388B in CQFP and CBGA packages.
The input capacitance is mainly due to the package.

8.3.1 Differential Inputs Voltage Span

Figure 8-1. Differential Inputs Voltage Span



8.3.2 Differential vs. Single-ended Analog Input Operation

The TS8388B can operate at full speed in either differential or single-ended configuration.

This is explained by the fact the ADC uses a high input impedance differential preamplifier stage, (preceeding the sample and hold stage), which has been designed in order to be entered either in differential mode or single-ended mode.

This is true so long as the out-of-phase analog input pin V_{INB} is 50Ω terminated very closely to one of the neighboring shield ground pins (52, 53, 58, 59) which constitute the local ground reference for the inphase analog input pin (V_{IN}).

Thus the differential analog input preamplifier will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.

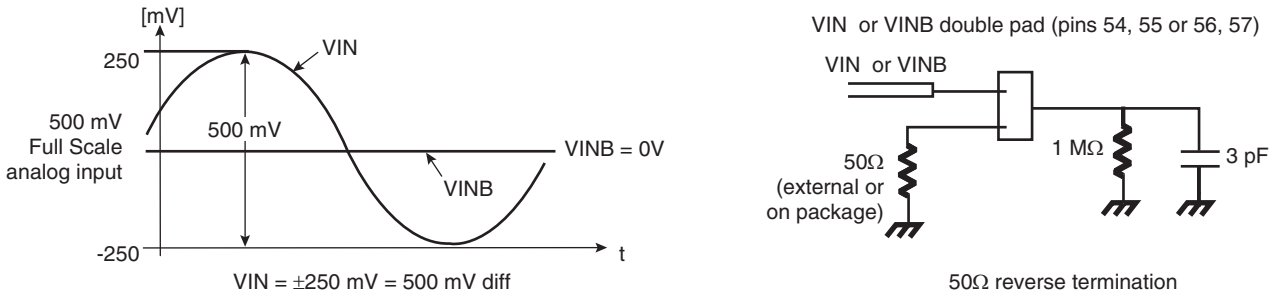
In typical single-ended configuration, enter on the (V_{IN}) input pin, with the inverted phase input pin (V_{INB}) grounded through the 50Ω termination resistor.

In single-ended input configuration, the in-phase input amplitude is 0.5V peak to peak, centered on 0V (or -2 dBm into 50Ω). The inverted phase input is at ground potential through a 50Ω termination resistor.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

8.3.3 Typical Single-ended Analog Input Configuration

Figure 8-2. Typical Single-ended Analog Input Configuration



Note: Since VIN and VINB have a double pad architecture, a 50Ω reverse termination is needed. For the CBGA package, this reverse termination is already on package.

8.4 Clock Inputs (CLK) (CLKB)

The TS8388B can be clocked at full speed without noticeable performance degradation in either differential or single-ended configuration.

This is explained by the fact the ADC uses a differential preamplifier stage for the clock buffer, which has been designed in order to be entered either in differential or single-ended mode.

Recommended sinewave generator characteristics are typically –120 dBc/Hz phase noise floor spectral density, at 1 kHz from carrier, assuming a single tone 4 dBm input for the clock signal.

8.4.1 Single-ended Clock Input (Ground Common Mode)

Although the clock inputs were intended to be driven differentially with nominal –0.8V/–1.8V ECL levels, the TS8388B clock buffer can manage a single-ended sinewave clock signal centered around 0V. This is the most convenient clock input configuration as it does not require the use of a power splitter.

No performance degradation (that is: due to timing jitter) is observed in this particular single-ended configuration up to 1.2 Gsps Nyquist conditions (F_{IN} = 600 MHz).

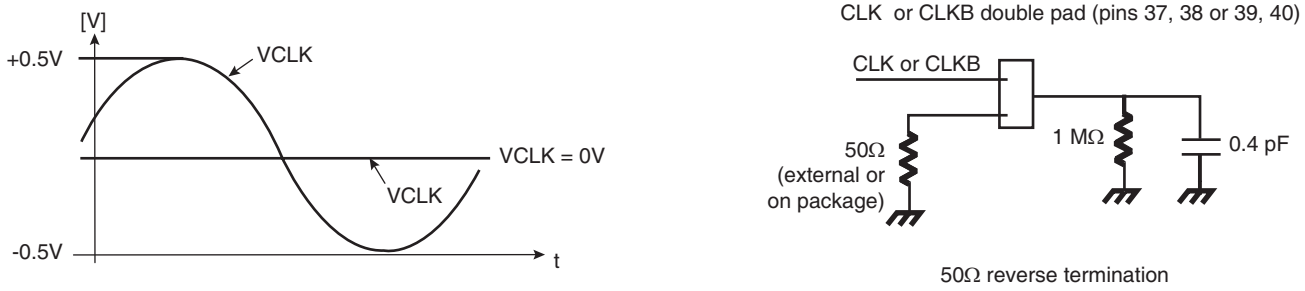
This is true so long as the inverted phase clock input pin is 50Ω terminated very closely to one of the neighboring shield ground pins, which constitutes the local Ground reference for the inphase clock input.

Thus the TS8388B differential clock input buffer will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects. Moreover, a very low phase noise sinewave generator must be used for enhanced jitter performance.

The typical inphase clock input amplitude is 1V peak to peak, centered on 0V (ground) common mode. This corresponds to a typical clock input power level of 4 dBm into the 50Ω termination resistor. Do not exceed 10 dBm to avoid saturation of the preamplifier input transistors.

The inverted phase clock input is grounded through the 50Ω termination resistor.

Figure 8-3. Single-ended Clock Input (Ground common mode):
VCLK Common Mode = 0V; VCLKB = 0V; 4 dBm Typical Clock Input Power Level (into 50Ω termination resistor)



Note: Do not exceed 10 dBm into the 50Ω termination resistor for single clock input power level.

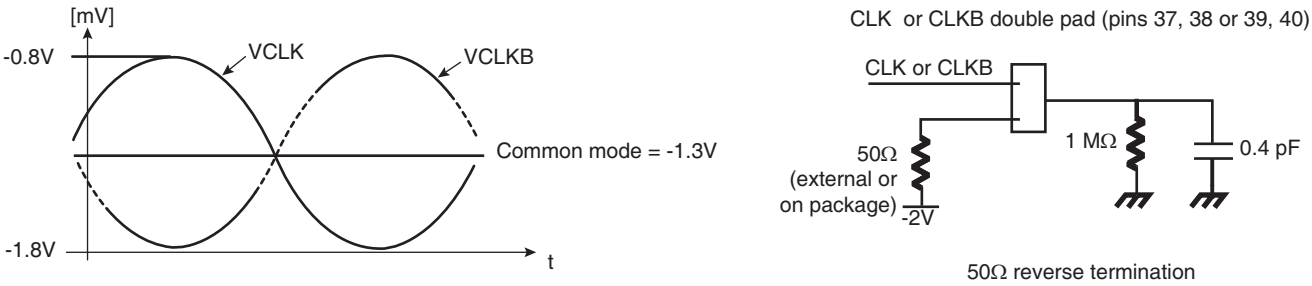
8.4.2 Differential ECL Clock Input

The clock inputs can be driven differentially with nominal –0.8V/–1.8V ECL levels.

In this mode, a low phase noise sinewave generator can be used to drive the clock inputs, followed by a power splitter (hybrid junction) in order to obtain 180 degrees out of phase sinewave signals. Biasing tees can be used for offseting the common mode voltage to ECL levels.

Note: As the biasing tees propagation times are not matching, a tunable delay line is required in order to ensure the signals to be 180 degrees out of phase especially at fast clock rates in the Gsps range.

Figure 8-4. Differential Clock Inputs (ECL Levels)

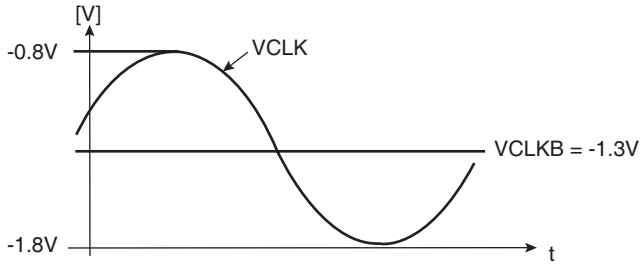


8.4.3 Single-ended ECL Clock Input

In single-ended configuration enter on CLK (resp. CLKB) pin, with the inverted phase clock input pin CLKB (respectively CLK) connected to –1.3V through the 50Ω termination resistor.

The inphase input amplitude is 1V peak to peak, centered on –1.3V common mode.

Figure 8-5. Single-ended Clock Input (ECL):
VCLK Common Mode = –1.3V; VCLKB = –1.3V



8.5 Noise Immunity Information

Circuit noise immunity performance begins at design level.

Efforts have been made on the design in order to make the device as insensitive as possible to chip environment perturbations resulting from the circuit itself or induced by external circuitry (Cascode stages isolation, internal damping resistors, clamps, internal (on-chip) decoupling capacitors).

Furthermore, the fully differential operation from analog input up to the digital outputs provides enhanced noise immunity by common mode noise rejection.

Common mode noise voltage induced on the differential analog and clock inputs will be canceled out by these balanced differential amplifiers.

Moreover, proper active signals shielding has been provided on the chip to reduce the amount of coupled noise on the active inputs.

The analog inputs and clock inputs of the TS8388B device have been surrounded by ground pins, which must be directly connected to the external ground plane.

8.6 Digital Outputs

The TS8388B differential output buffers are internally 75Ω loaded. The 75Ω resistors are connected to the digital ground pins through a –0.8V level shift diode (see Figure 8-6, Figure 8-7, Figure 8-8 on page 36).

The TS8388B output buffers are designed for driving 75Ω (default) or 50Ω properly terminated impedance lines or coaxial cables. An 11 mA bias current flowing alternately into one of the 75Ω resistors when switching ensures a 0.825V voltage drop across the resistor (unterminated outputs).

The V_{PLUSD} positive supply voltage allows the adjustment of the output common mode level from –1.2V (V_{PLUSD} = 0V for ECL output compatibility) to +1.2V (V_{PLUSD} = 2.4V for LVDS output compatibility).

Therefore, the single-ended output voltages vary approximately between –0.8V and –1.625V, (outputs unterminated), around –1.2V common mode voltage.

Three possible line driving and back-termination scenarios are proposed (assuming V_{PLUSD} = 0V):

1. 75Ω impedance transmission lines, 75Ω differentially terminated (Figure 8-6):

   Each output voltage varies between –1V and –1.42V (respectively +1.4V and +1V), leading to ±0.41V = 0.825V in differential, around –1.21V (respectively +1.21V) common mode for V_{PLUSD} = 0V (respectively 2.4V).

2. 50Ω impedance transmission lines, 50Ω differentially termination (Figure 8-7):

   Each output voltage varies between –1.02V and –1.35V (respectively +1.38V and +1.05V), leading to ±0.33V = 660 mV in differential, around –1.18V (respectively +1.21V) common mode for V_{PLUSD} = 0V (respectively 2.4V).

3. 75Ω impedance open transmission lines (Figure 8-8):

   Each output voltage varies between –1.6V and –0.8V (respectively +0.8V and +1.6V), which are true ECL levels, leading to ±0.8V = 1.6V in differential, around –1.2V (respectively +1.2V) common mode for V_{PLUSD} = 0V (respectively 2.4V). Therefore, it is possible to drive directly high input impedance storing registers, without terminating the 75Ω transmission lines. In time domain, that means that the incident wave will reflect at the 75Ω transmission line output and travel back to the generator (that is: the 75Ω data output buffer). As the buffer output impedance is 75Ω, no back reflection will occur.

Note: This is no longer true if a 50Ω transmission line is used, as the latter is not matching the buffer 75Ω output impedance.

Each differential output termination length must be kept identical. It is recommended to decouple the midpoint of the differential termination with a 10 nF capacitor to avoid common mode perturbation in case of slight mismatch in the differential output line lengths.

Too large mismatches (keep < a few mm) in the differential line lengths will lead to switching currents flowing into the decoupling capacitor leading to switching ground noise.

The differential output voltage levels (75Ω or 50Ω termination) are not ECL standard voltage levels, however it is possible to drive standard logic ECL circuitry like the ECLinPS logic line from Freescale®.

At sampling rates exceeding 1 Gsps, it may be difficult to trigger any Acquisition System with digital outputs. It becomes necessary to regenerate digital data and Data Ready by means of external amplifiers, in order to be able to test the TS8388B at its optimum performance conditions.

8.6.1 Differential Output Loading Configurations (Levels for ECL Compatibility)

Figure 8-6. Differential Output: 75Ω Terminated

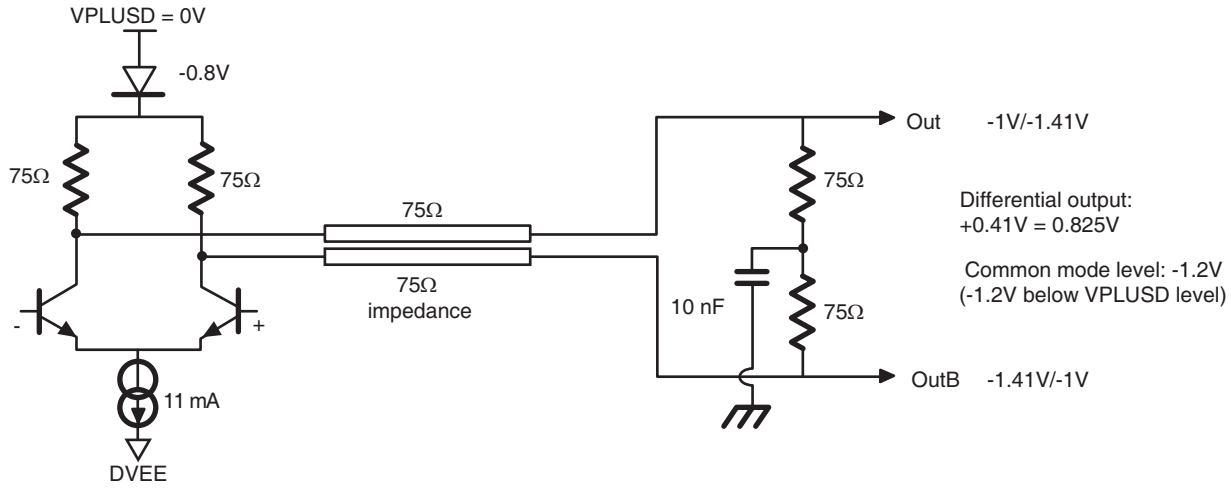


Figure 8-7. Differential Output: 50Ω Terminated

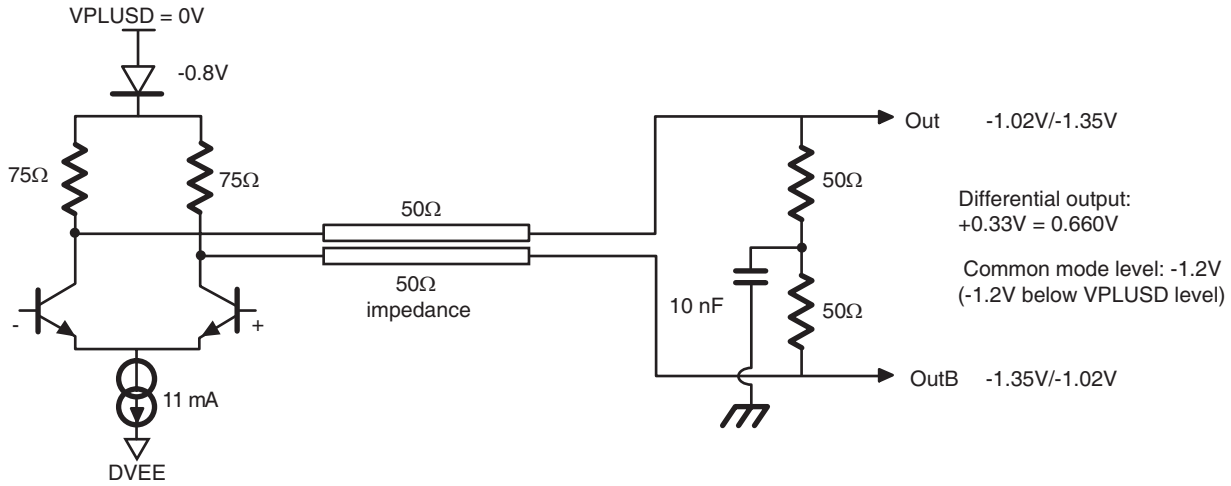
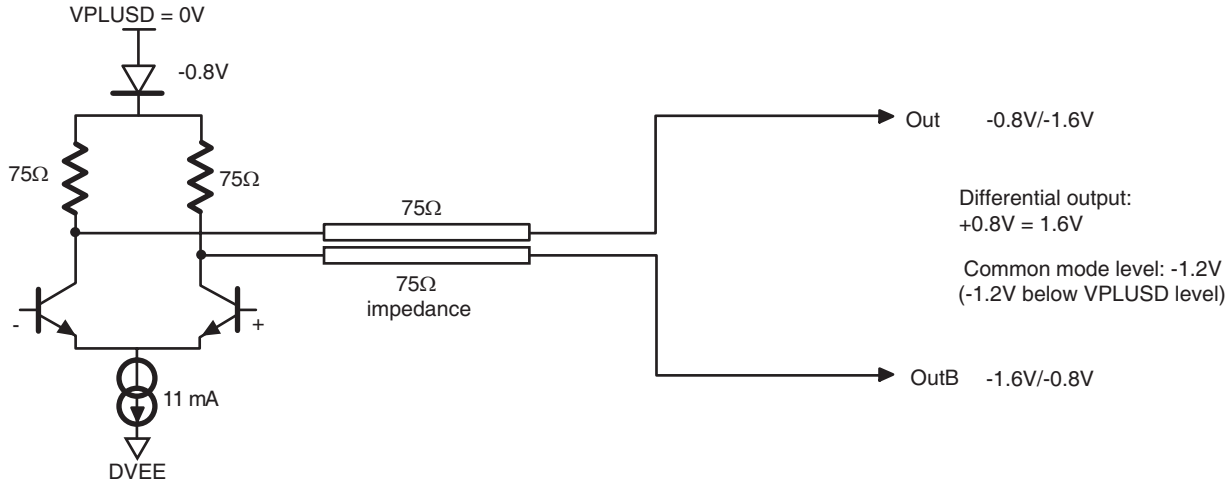


Figure 8-8. Differential Output: Open Loaded



8.6.2 Differential Output Loading Configurations (Levels for LVDS Compatibility)

Figure 8-9. Differential Output: 75Ω Terminated

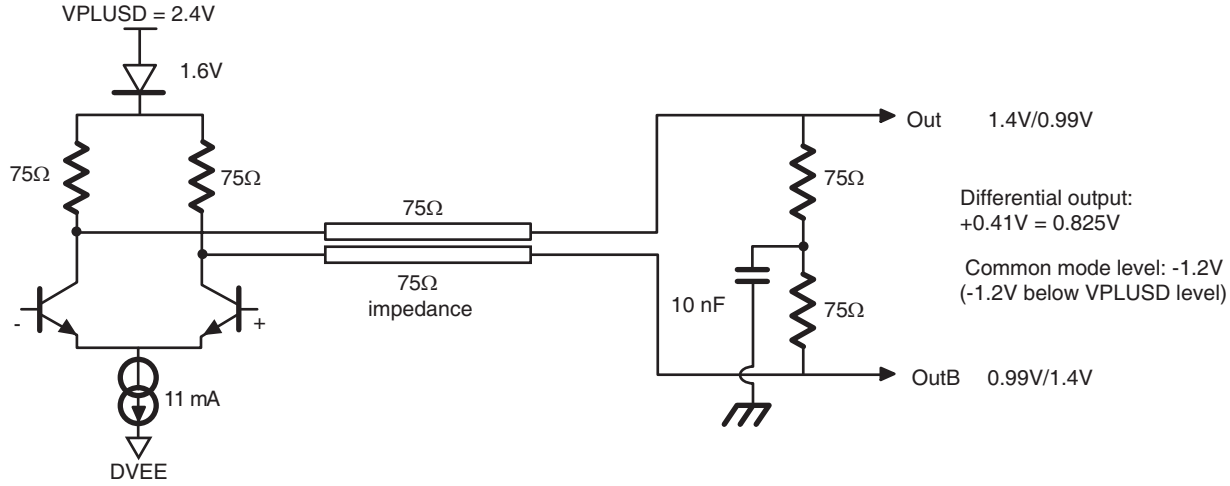


Figure 8-10. Differential Output: 50Ω Terminated

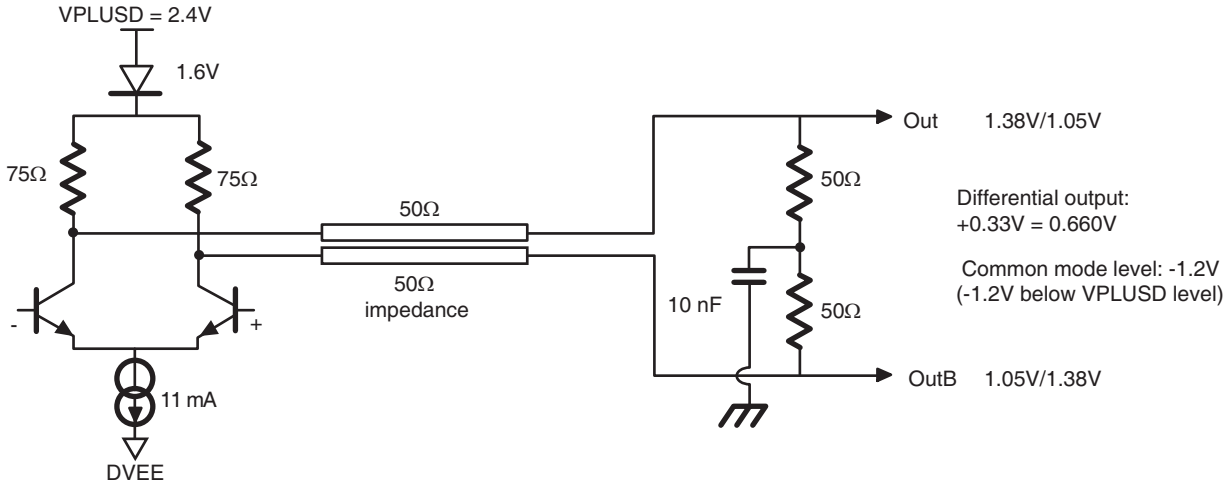
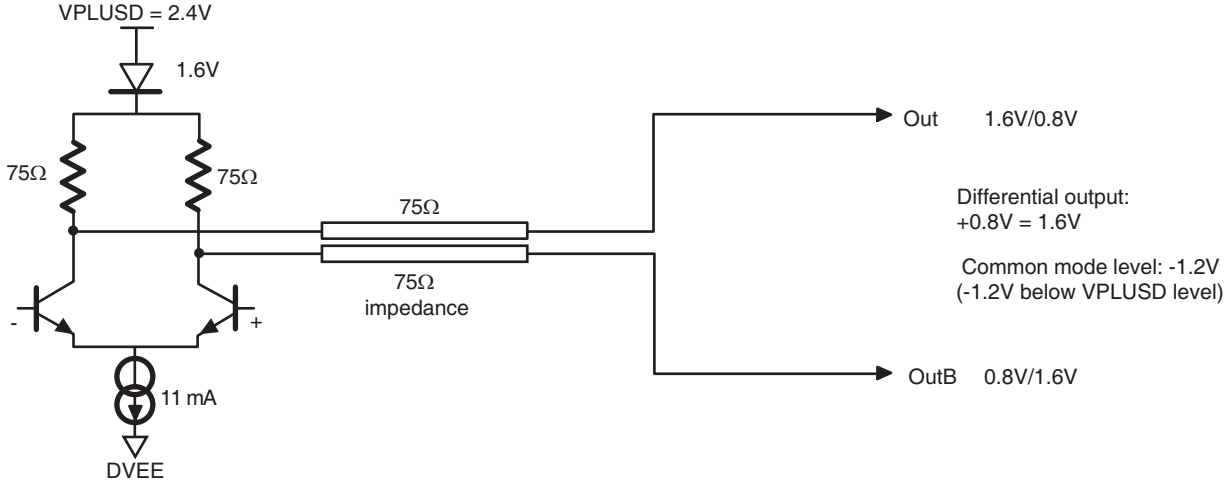


Figure 8-11. Differential Output: Open Loaded



8.7 Out-of-range Bit

An out-of-range (OR, ORB) bit is provided that goes to logical high state when the input exceeds the positive full scale or falls below the negative full scale.

When the analog input exceeds the positive full scale, the digital output data remain at high logical state, with (OR, ORB) at logical one.

When the analog input falls below the negative full scale, the digital outputs remain at logical low state, with (OR, ORB) at logical one again.

8.8 Gray or Binary Output Data Format Select

The TS8388B internal regeneration latches indecision (for inputs very close to latches threshold) may produce errors in the logic encoding circuitry and leading to large amplitude output errors.

This is due to the fact that the latches are regenerating the internal analog residues into logical states with a finite voltage gain value (Av) within a given positive amount of time $\Delta(t)$:

$Av = \exp(\Delta(t)/\tau)$, with τ the positive feedback regeneration time constant.

The TS8388B has been designed for reducing the probability of occurrence of such errors to approximately 10^{-13} (targeted for the TS8388B at 1 Gsps).

A standard technique for reducing the amplitude of such errors down to ± 1 lsb consists of outputting the digital data in Gray code format. Though the TS8388B has been designed for featuring a Bit Error Rate of 10^{-13} with a binary output format, it is possible for the user to select between the Binary or Gray output data format, in order to reduce the amplitude of such errors when occurring, by storing Gray output codes.

Digital data format selection:

- Binary output format if GORB is floating or V_{CC}
- Gray output format if GORB is connected to ground (0V)

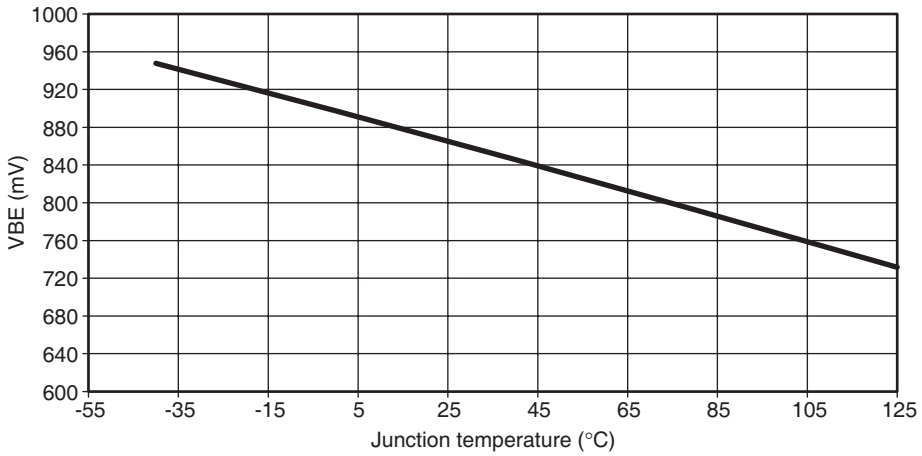
8.9 Diode Pin 49

One single pin is used for both DRRB input command and die junction monitoring. The pin denomination is DRRB/DIOD. Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

(See “Principle of Data Ready Signal Control by DRRB Input Command” on page 29 for Data Ready Reset input command).

The operating die junction temperature must be kept below 145°C, therefore an adequate cooling system has to be set up. The diode mounted transistor measured Vbe value vs. junction temperature is given below.

Figure 8-12. Diode Pin 49

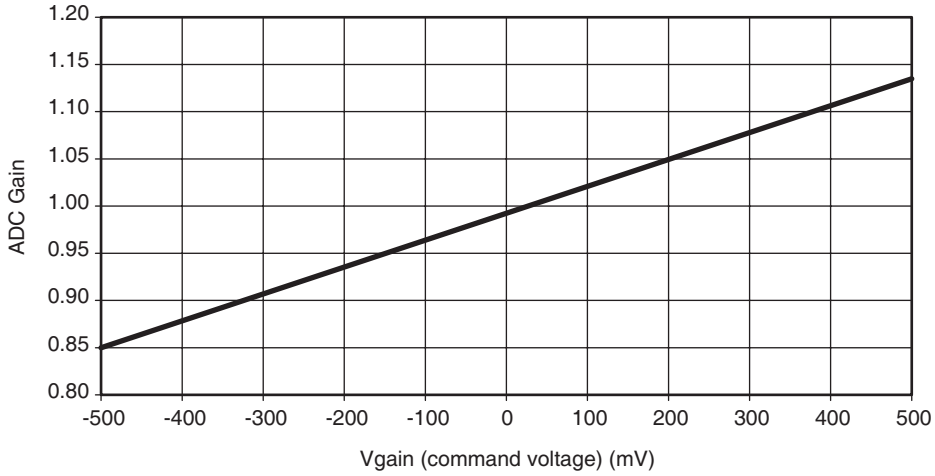


8.10 ADC Gain Control Pin 60

The ADC gain is adjustable by the means of the pin 60 (input impedance is 1 MΩ in parallel with 2 pF).

The gain adjust transfer function is given below.

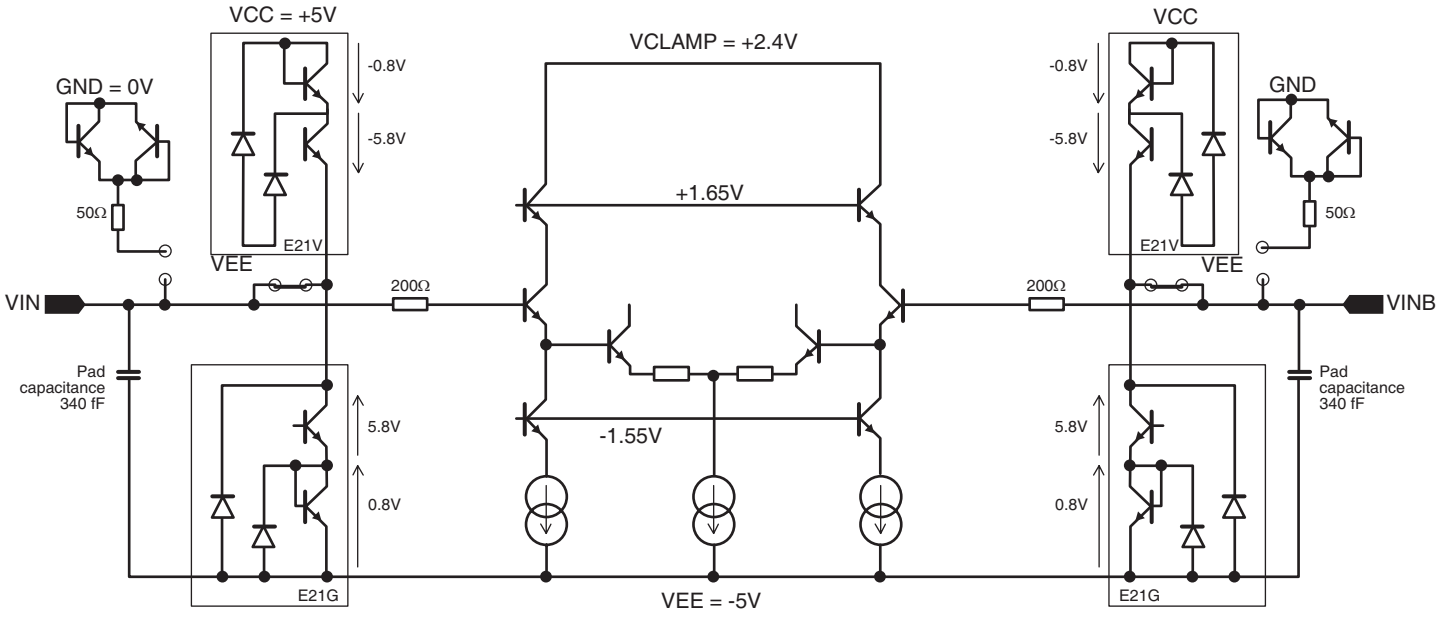
Figure 8-13. ADC Gain Control Pin 60



Note: For more information, please refer to the document “DEMUX and ADCs Application Notes”.

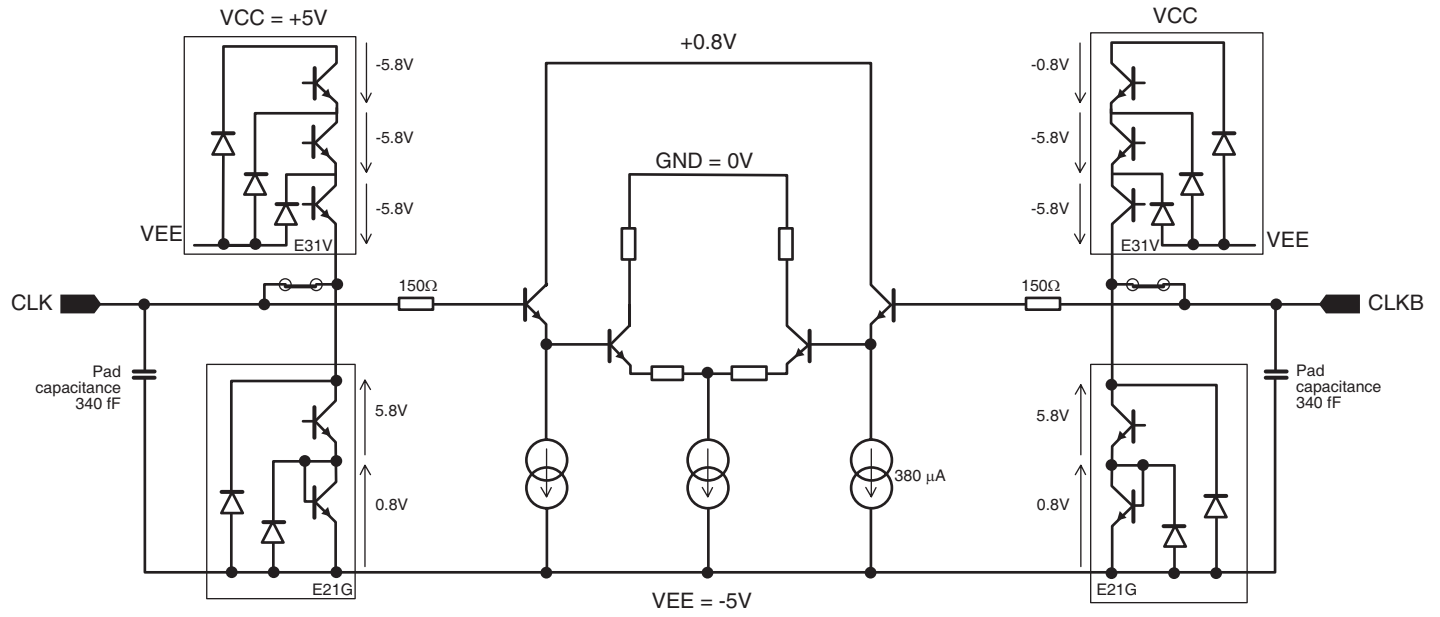
9. Equivalent Input/Output Schematics

Figure 9-1. Equivalent Analog Input Circuit and ESD Protections



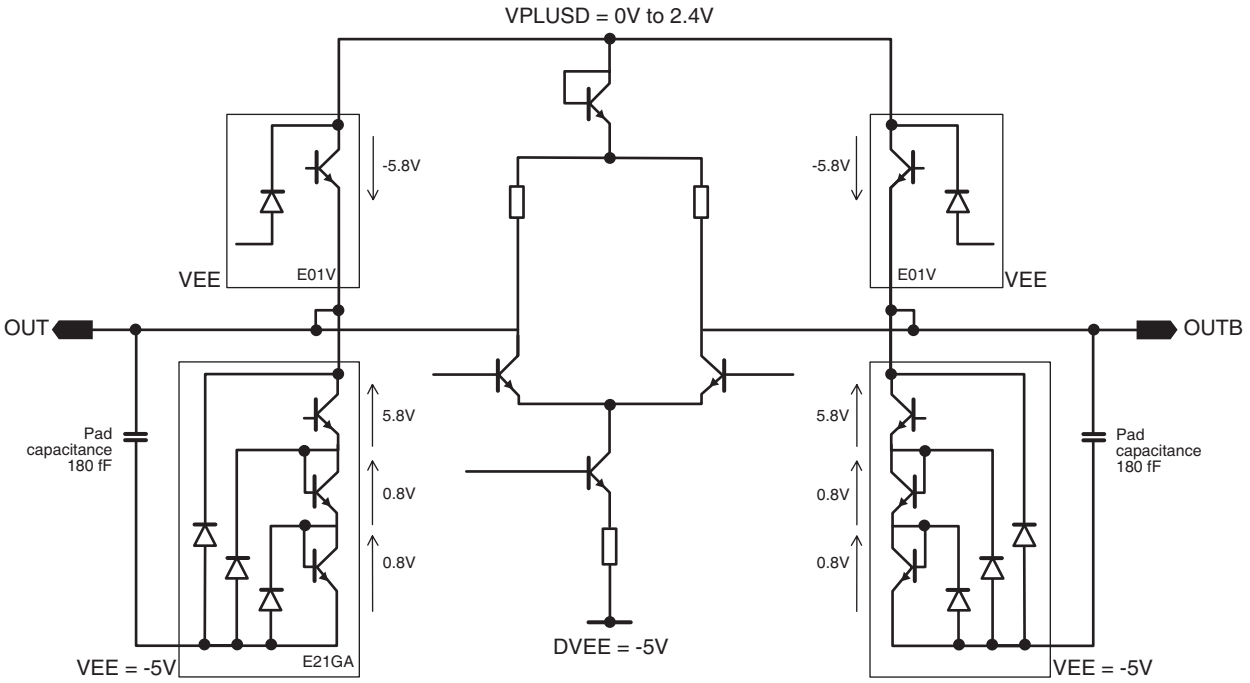
Note: The ESD protection equivalent capacitance is 150 fF.

Figure 9-2. Equivalent Analog Clock Input Circuit and ESD Protections



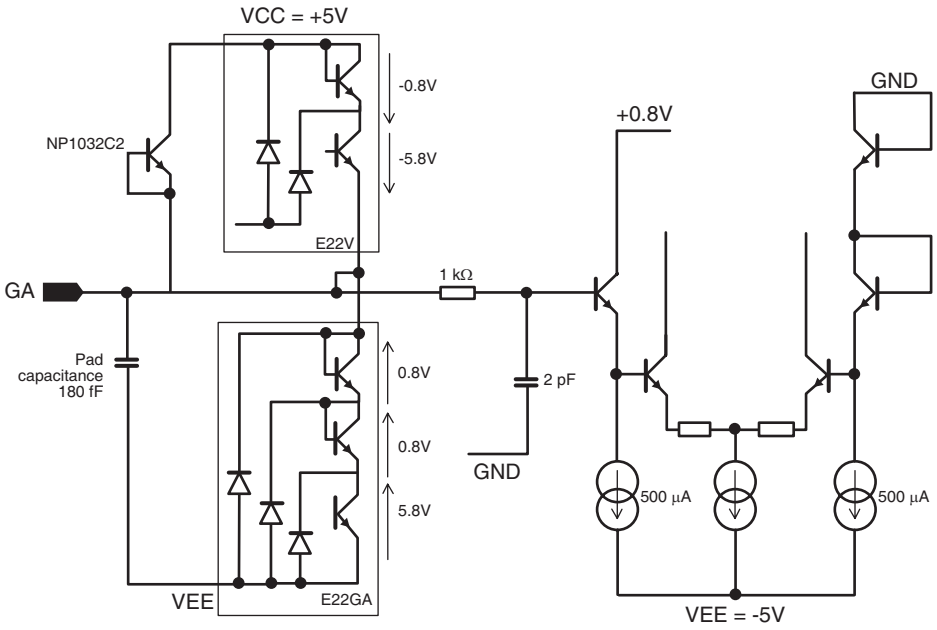
Note: The ESD protection equivalent capacitance is 150 fF.

Figure 9-3. Equivalent Data Output Buffer Circuit and ESD Protections



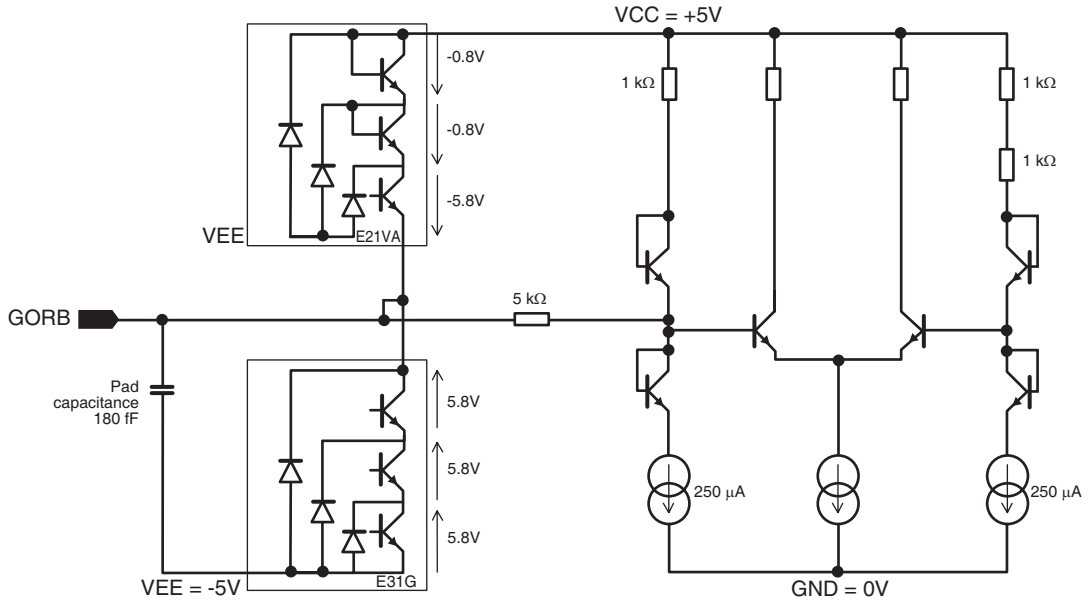
Note: The ESD protection equivalent capacitance is 150 fF.

Figure 9-4. ADC Gain Adjust Equivalent Analog Input Circuit and ESD Protections



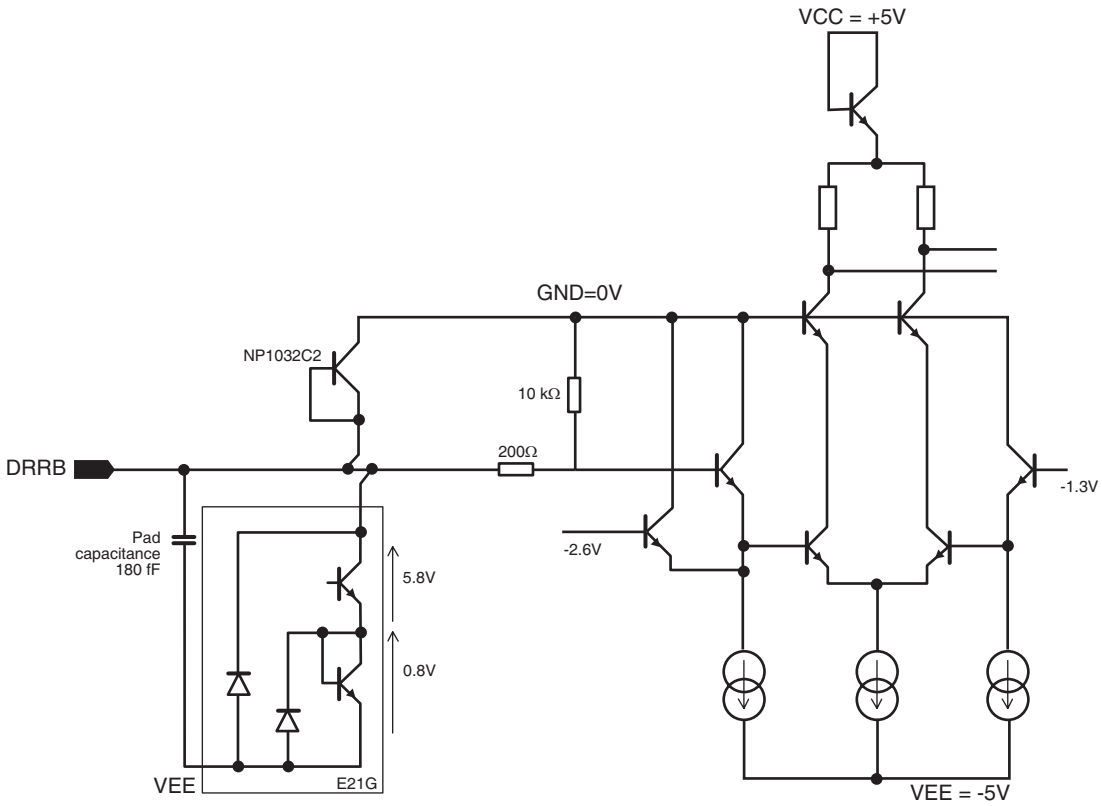
Note: The ESD protection equivalent capacitance is 150 fF.

Figure 9-5. GORB Equivalent Input Schematic and ESD Protections
GORB: Gray or Binary Select Input, Floating or Tied to V_{CC} -> Binary



Note: The ESD protection equivalent capacitance is 150 fF.

Figure 9-6. DRRB Equivalent Input Schematic and ESD Protections
(Actual protection range: 6.6V above V_{EE}, in fact stress above GND are clipped by the CB diode used for T_J monitoring)



Note: The ESD protection equivalent capacitance is 150 fF.

10. TSEV8388B: Device Evaluation Board

For complete specification, see separate TSEV8388B document.

10.1 General Description

The TSEV8388B Evaluation Board (EB) is a board which has been designed in order to facilitate the evaluation and the characterization of the TS8388B device up to its 1.5 GHz full power bandwidth at up to 1 Gsps in the military temperature range.

The high speed of the TS8388B requires careful attention to circuit design and layout to achieve optimal performance.

This four metal layer board with internal ground plane has the adequate functions in order to allow a quick and simple evaluation of the TS8388B ADC performances over the temperature range.

The TSEV8388B Evaluation Board is very straightforward as it only implements the TS8388B ADC, SMA connectors for input/output accesses and a 2.54 mm pitch connector compatible with high speed acquisition system probes.

The board also implements a de-embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the input microstrip lines, and a die junction temperature measurement setting.

The board is constituted by a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

The board dimensions are 130 mm x 130 mm.

The board set comes fully assembled and tested, with the TS8388B installed.

10.2 CBGA68 Thermal and Moisture Characteristics

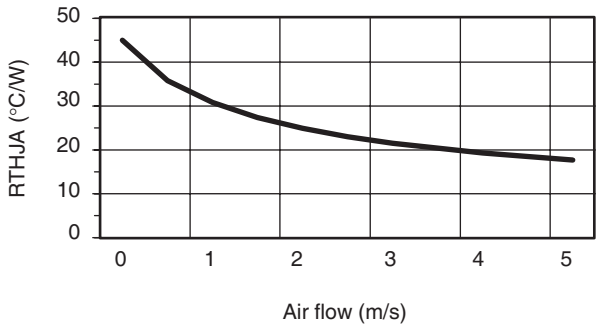
10.2.1 Thermal Resistance from Junction to Ambient: RTHJA

The following table lists the converter thermal performance parameters of the device itself, with no external heatsink added.

Table 10-1. Thermal Resistance

Air flow (m/s)	Estimated JA thermal resistance (°C/W)
0	45
0.5	35.8
1	30.8
1.5	27.4
2	24.9
2.5	23
3	21.5
4	19.3
5	17.7

Figure 10-1. Thermal Resistance from Junction to Ambient: RTHJA



10.2.2 Thermal Resistance from Junction to Case: RTHJC

Typical value for Rthjc is given to 6.7°C/W (8°C/W max).

This value does not include thermal contact resistance between package and external component (heat-sink or PCBoard).

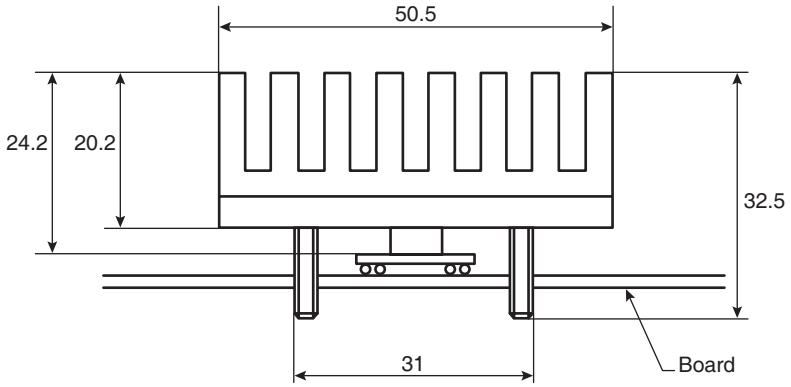
As an example, 2.0°C/W can be taken for 50 µm of thermal grease.

10.2.3 CBGA68 Board Assembly with External Heatsink

It is recommended to use an external heatsink or PCBoard special design.

Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.

Figure 10-2. CBGA68 Board Assembly



10.2.4 Moisture Characteristics

This device is sensitive to the moisture (MSL3 according to JEDEC standard):

Shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

After this bag is opened, devices that will be subjected to infrared reflow, vapor-phase reflow, or equivalent processing (peak package body temperature 220°C) must be:

- Mounted within 198 hours at factory conditions of ≤30°C/60% RH, or
- Stored at ≤20% RH

Devices require baking, before mounting, if Humidity Indicator Card is >20% when read at 23°C ±5°C.

If baking is required, devices may be baked for:

- 192 hours at 40°C +5°C/–0°C and <5% RH for low-temperature device containers, or
- 24 hours at 125°C ±5°C for high temperature device containers

10.3 Nominal CQFP68 Thermal Characteristics

Although the power dissipation is low for this performance, the use of a heat sink is mandatory.

The user will find some advice on this topics below.

10.3.1 Thermal Resistance from Junction to Ambient: RTHJA

The following table lists the converter thermal performance parameters, with or without heatsink.

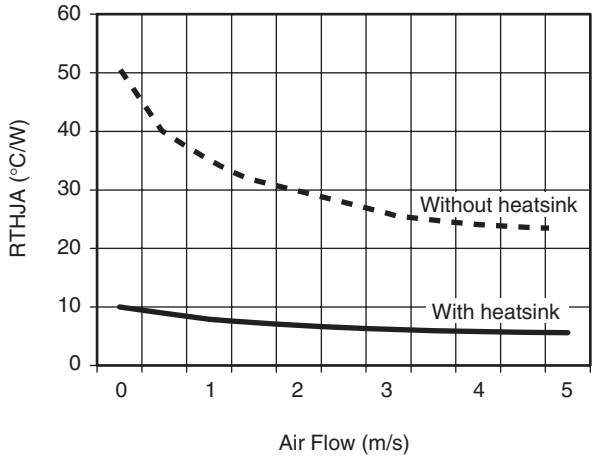
For the following measurements, a 50 x 50 x 16 mm heatsink has been used (see Figure 10-4 on page 47).

Table 10-2. Thermal Resistance

Air Flow (m/s)	Estimated JA Thermal Resistance (°C/W) CQFP68 on Board	
	Estimated – without Heatsink	Targeted – with Heatsink(1)
0	50	10
0.5	40	8.9
1	35	7.9
1.5	32	7.3
2	30	6.8
2.5	28	6.5
3	26	6.2
4	24	5.8
5	23.5	5.6

Note: 1. Heatsink is glued to backside of package or screwed and pressed with thermal grease.

Figure 10-3. Thermal Resistance from Junction to Ambient: RTHJA

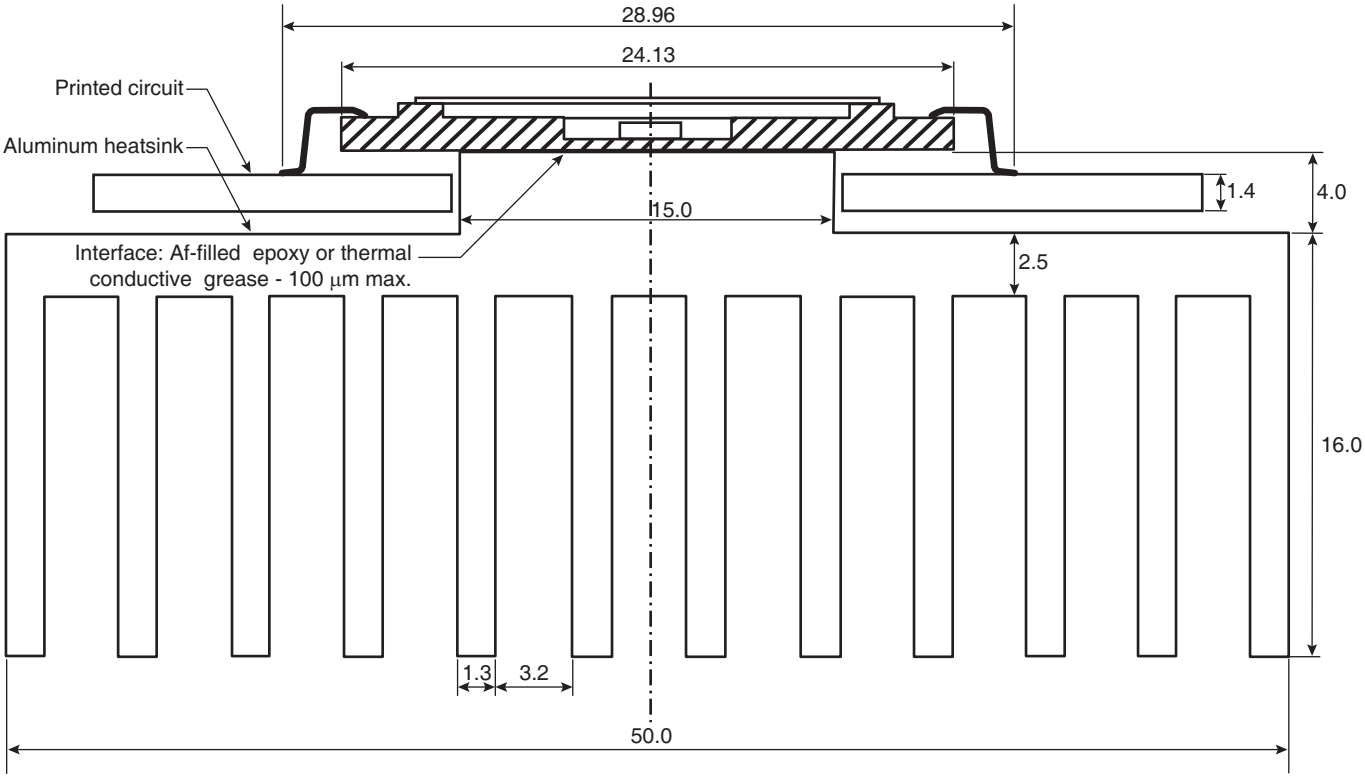


10.3.2 Thermal Resistance from Junction to Case: RTHJC

Typical value for Rthjc is given to 4.75°C/W.

10.3.3 CQFP68 Board Assembly

Figure 10-4. CQFP68 Board Assembly with a 50 x 50 x 16 mm External Heatsink



10.4 Enhanced CQFP68 Thermal Characteristics

10.4.1 Enhanced CQFP68

The CQFP68 has been modified, in order to improve the thermal characteristics:

- A CuW heatspreader has been added at the bottom of the package.
- The die has been electrically isolated with the ALN substrate.

10.4.2 Thermal Resistance from Junction to Case: RTHJC

Typical value for Rthjc is given to 1.56°C/W.

This value does not include thermal contact resistance between package and external component (heat-sink or PCBoard).

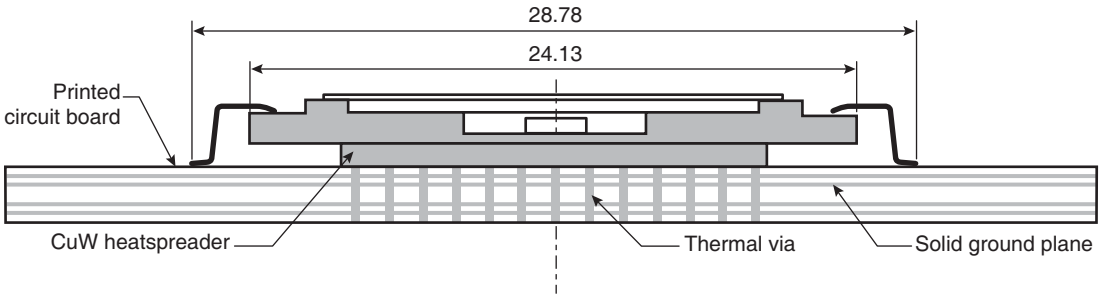
As an example, 2.0°C/W can be taken for 50 µm of thermal grease.

10.4.3 Heatsink

It is recommended to use an external heatsink, or PCBoard special design.

The stand off has been calculated to permit the simultaneous soldering of the leads and of the heatspreader with the solder paste.

Figure 10-5. Enhanced CQFP68 Suggested Assembly



Cooling system efficiency can be monitored using the Temperature Sensing Diode, integrated in the device.

10.5 Definitions

10.5.1 Definition of Terms

10.5.1.1 (BER) Bit Error Rate

Probability to exceed a specified error threshold for a sample. An error code is a code that differs by more than ± 4 lsb from the correct code.

10.5.1.2 (FPBW) Full Power Input Bandwidth

Analog input frequency at which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale.

10.5.1.3 (SINAD) Signal to Noise and Distortion Ratio

Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale, to the RMS sum of all other spectral components, including the harmonics except DC.

10.5.1.4 (SNR) Signal to Noise Ratio

Ratio expressed in dB of the RMS signal amplitude, set to 1 dB below Full Scale, to the RMS sum of all other spectral components excluding the five first harmonics.

10.5.1.5 (THD) Total Harmonic Distortion

Ratio expressed in dBc of the RMS sum of the first five harmonic components, to the RMS value of the measured fundamental spectral component.

10.5.1.6 (SFDR) Spurious Free Dynamic Range

Ratio expressed in dB of the RMS signal amplitude, set at 1 dB below Full Scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (Radar systems, digital receiver, network analyzer, etc.). It may be reported in dBc (that is: degrades as signal levels is lowered), or in dBFS (that is: always related back to converter full scale).

10.5.1.7 (ENOB) Effective Number of Bits

$$ENOB = \frac{SINAD - 1.76 + 20 \log (A/V/2)}{6.02}$$

Where A is the actual input amplitude and V is the full scale range of the ADC under test.

10.5.1.8 (DNL) Differential Non Linearity

The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 lsb guarantees that there are no missing output codes and that the transfer function is monotonic.

10.5.1.9 (INL) Integral Nonlinearity

The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.

INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.

10.5.1.10 (DG) Differential Gain

The peak gain variation (in percent) at five different DC levels for an AC signal of 20% Full Scale peak to peak amplitude. F_{IN} = 5 MHz (TBC).

10.5.1.11 (DP) Differential Phase

Peak Phase variation (in degrees) at five different DC levels for an AC signal of 20% Full Scale peak to peak amplitude. F_{IN} = 5 MHz (TBC).

10.5.1.12 (TA) Aperture Delay

Delay between the rising edge of the differential clock inputs (CLK, CLKB) (zero crossing point), and the time at which (V_{IN}, V_{INB}) is sampled.

10.5.1.13 (JITTER) Aperture Uncertainty

Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.

10.5.1.14 (TS) Settling Time

Time delay to achieve 0.2% accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.

10.5.1.15 (ORT) Overvoltage Recovery Time

Time to recover 0.2% accuracy at the output, after a 150% full scale step applied on the input is reduced to midscale.

10.5.1.16 (TOD) Digital Data Output Delay

Delay from the falling edge of the differential clock inputs (CLK, CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.

10.5.1.17 (TD1) Time Delay from Data to Data Ready

Time delay from Data transition to Data ready.

10.5.1.18 (TD2) Time Delay from Data Ready to Data

General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period.

10.5.1.19 (TC) Encoding Clock Period

TC1 = Minimum clock pulse width (high) TC = TC1 + TC2

TC2 = Minimum clock pulse width (low)

10.5.1.20 (TPD) Pipeline Delay

Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD). For the TS8388B the TPD is 4 clock periods.

10.5.1.21 (TRDR) Data Ready Reset Delay

Delay between the falling edge of the Data Ready output asynchronous Reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR).

10.5.1.22 (TR) Rise Time

Time delay for the output DATA signals to rise from 20% to 80% of delta between low level and high level.

10.5.1.23 (TF) Fall Time

Time delay for the output DATA signals to fall from 80% to 20% of delta between low level and high level.

10.5.1.24 (PSRR) Power Supply Rejection Ratio

Ratio of input offset variation to a change in power supply voltage.

10.5.1.25 (NRZ) Non Return to Zero

When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the out-of-range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the out-of-range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).

10.5.1.26 (IMD) Intermodulation Distortion

The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. The input tones levels are at –7 dB Full Scale.

10.5.1.27 (NPR) Noise Power Ratio

The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.

11. Ordering Information

Table 11-1. Ordering Information

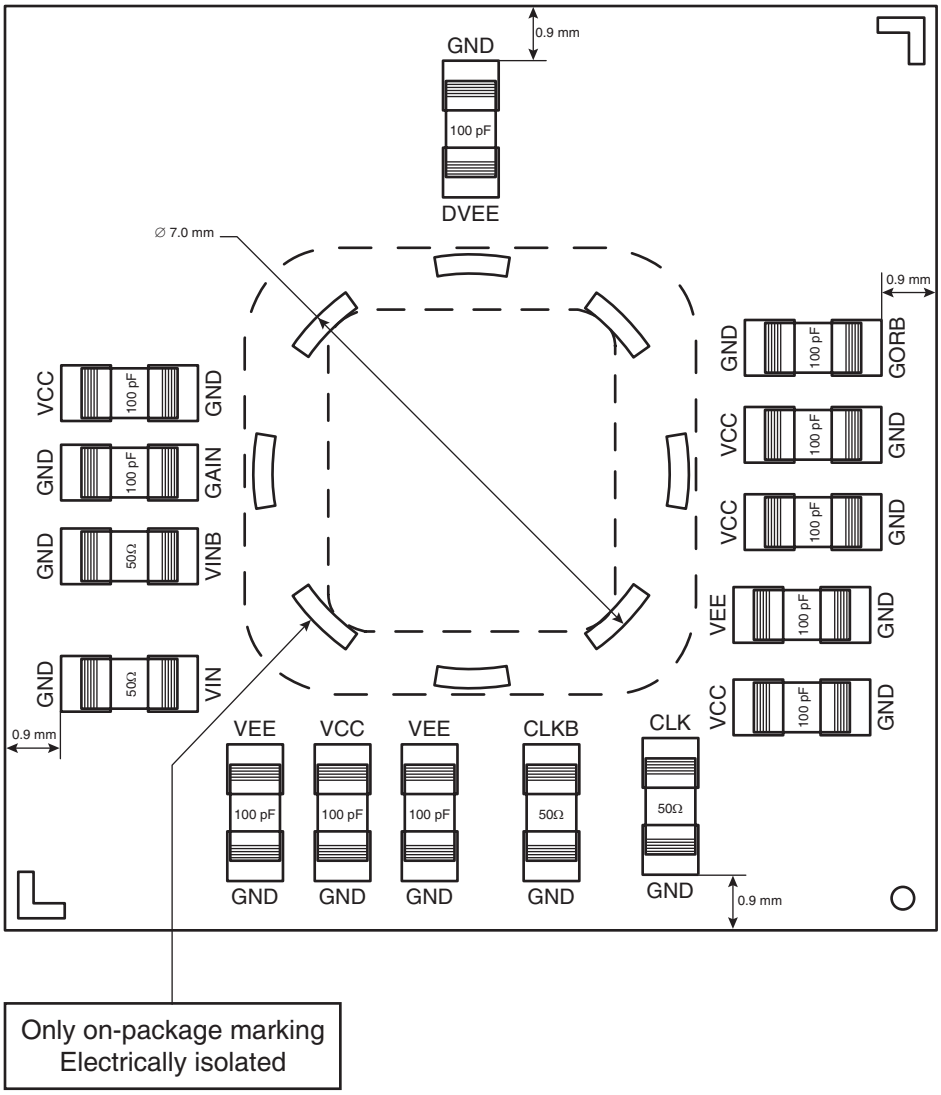
Part Number	Package	Temperature Range	Screening	Comments
JTS8388B-1V1B	Die	Ambient	Visual inspection	On request only (Please contact Marketing)
JTS8388B-1V2B	Die	Ambient and High temperature (T_J = 125°C)	Visual inspection	On request only (Please contact Marketing)
TS8388BCF	CQFP 68	"C" grade 0°C < Tc; T_J < 90°C	Standard	
TS8388BVF	CQFP 68	"V" grade –40°C < Tc; T_J< 110°C	Standard	
TS8388BMF	CQFP 68	"M" grade –55°C < Tc; T_J < 125°C	Standard	
TS8388BMF B/Q	CQFP 68	"M" grade –55°C < Tc; T_J < 125°C	Mil-PRF-38535, QML level Q	DSCC 5962-0050401QYC
TS8388BMF B/T	CQFP 68	"M" grade –55°C < Tc; T_J < 125°C	Standard + 3 temperatures test (min, ambient, max)	
TS8388BCFS	CQFP 68 with heatspreader	"C" grade 0°C < Tc; T_J < 90°C	Standard	
TS8388BVFS	CQFP 68 with heatspreader	"V" grade –40°C < Tc; T_J < 110°C	Standard	
TS8388BMFS	CQFP 68 with heatspreader	"M" grade –55°C < Tc; T_J < 125°C	Standard	
TS8388BMFS B/Q	CQFP 68 with heatspreader	"M" grade –55°C < Tc; T_J < 125°C	Mil-PRF-38535, QML level Q	DSCC 5962-0050401QXC
TS8388BMFS B/T	CQFP 68 with heatspreader	"M" grade –55°C < Tc; T_J< 125°C	Standard + 3 temperatures test (min, ambient, max)	
TS8388BMFS9NB1	CQFP 68 with heatspreader	"M" grade –55°C < Tc; T_J< 125°C	. ESA/SCC9000 Screening . Level B selection . Lot Acceptance Test 1, 2, 3	
TS8388BMFS9NB2	CQFP 68 with heatspreader	"M" grade –55°C < Tc; T_J < 125°C	. ESA/SCC9000 Screening . Level B selection . Lot Acceptance Test 2, 3	
TS8388BMFS9NB3	CQFP 68 with heatspreader	"M" grade –55°C < Tc; T_J < 125°C	. ESA/SCC9000 Screening . Level B selection . Lot Acceptance Test 3	
TS8388BCGL	CBGA 68	"C" grade 0°C < Tc; T_J < 90°C	Standard	
TS8388BVGL	CBGA 68	"V" grade –40°C < Tc; T_J < 110°C	Standard	
TSEV8388BF	CQFP 68	Ambient	Prototype	Evaluation board (delivered with heatsink)

Table 11-1. Ordering Information (Continued)

Part Number	Package	Temperature Range	Screening	Comments
TSEV8388BFZA2	CQFP 68	Ambient	Prototype	Evaluation board with digital receivers (delivered with heatsink)
TSEV8388BGL	CBGA 68	Ambient	Prototype	Evaluation board (delivered with heatsink)
TSEV8388BGLZA2	CBGA 68	Ambient	Prototype	Evaluation board with digital receivers (delivered with heatsink)

11.1 CBGA68 Capacitors and Resistors Implant

Figure 11-1. TS8388BGL Capacitors and Resistors Implant

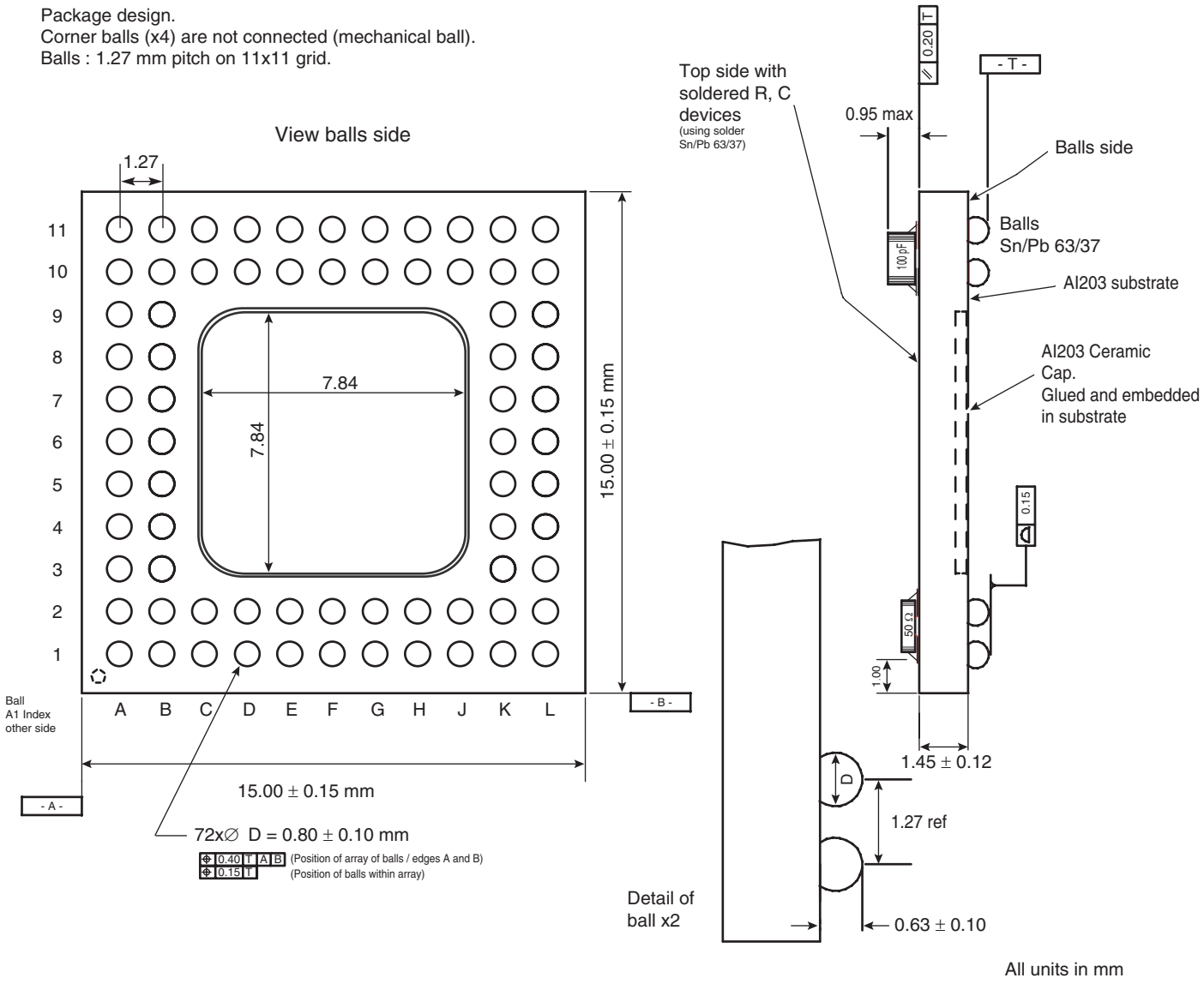


Note: R and C are discrete components of 0603 size (1.6 x 0.8 mm).

11.2 Outline Descriptions

Figure 11-2. Package Dimension – 68 Pins CBGA

CBGA 68 package.
AL203 substrate.
Package design.
Corner balls (x4) are not connected (mechanical ball).
Balls : 1.27 mm pitch on 11x11 grid.



11.3 Outline Dimensions

Figure 11-3. Package Dimension – 68-lead Ceramic Quad Flat Pack (CQFP)

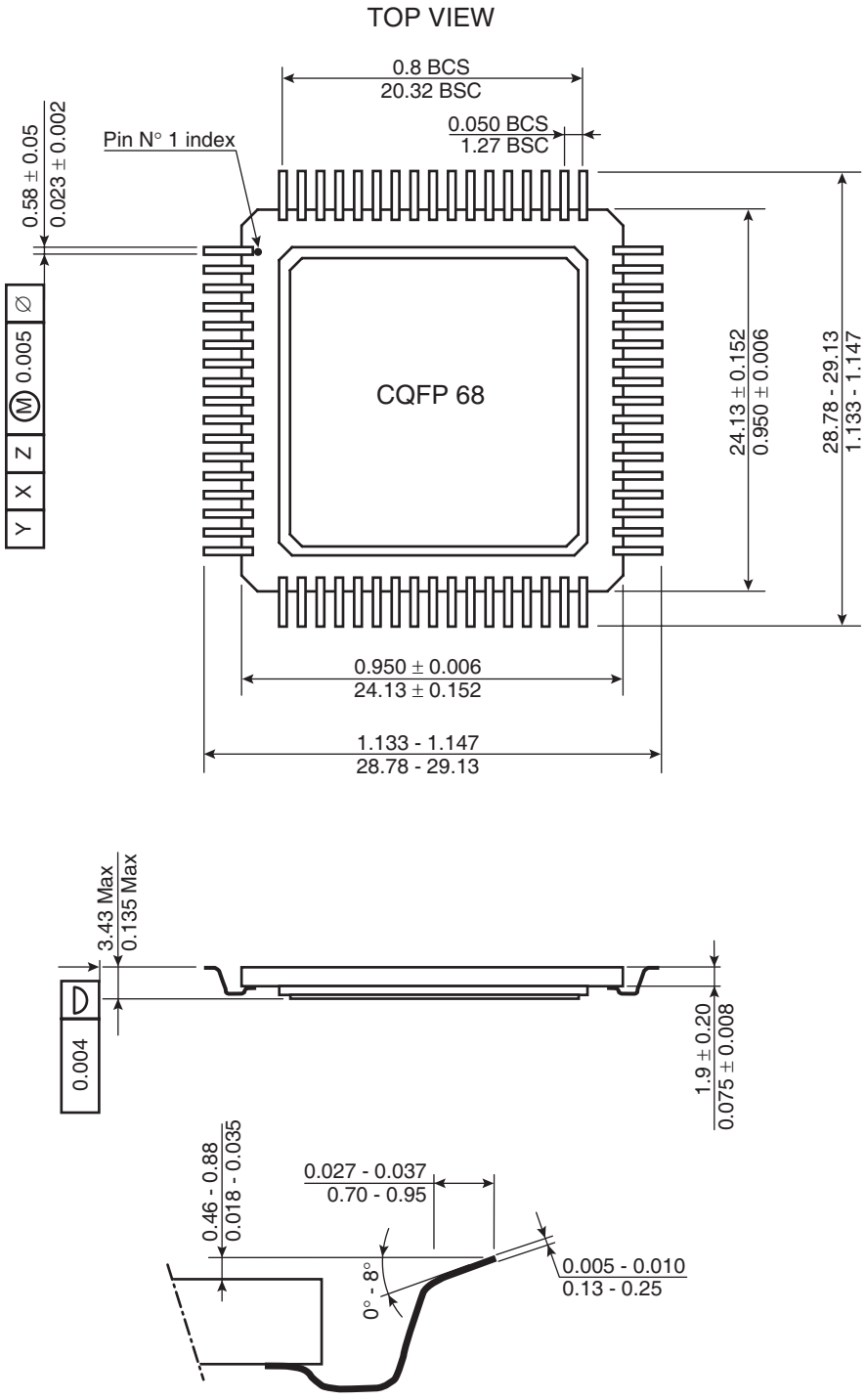
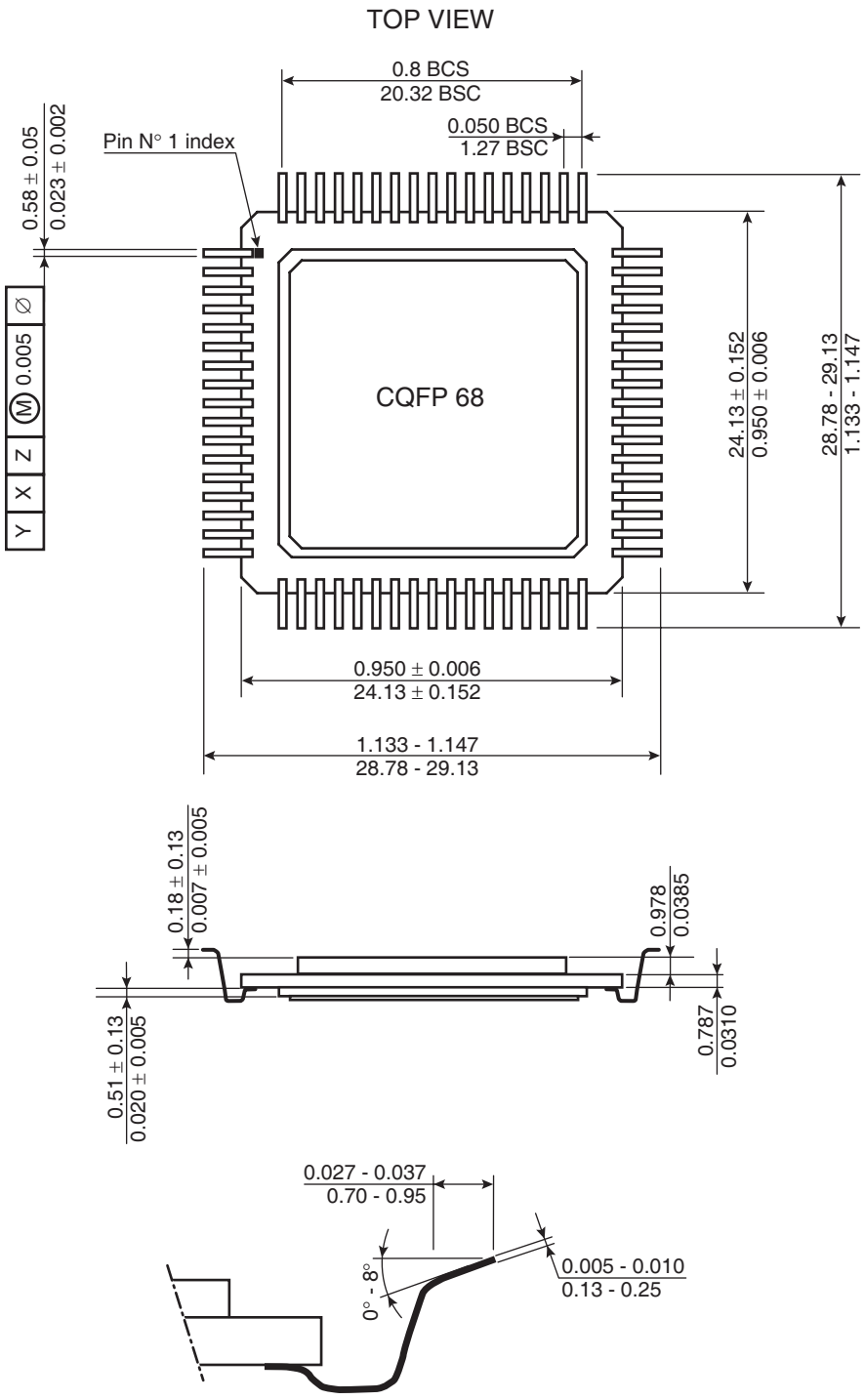


Figure 11-4. Package Dimension – 68-lead Enhanced CQFP with Heatspreder



12. Datasheet Status Description

Table 12-1. Datasheet Status

Datasheet Status		**Validity**
Objective specification	This datasheet contains target and goal specifications for discussion with customer and application validation.	Before design phase
Target specification	This datasheet contains target or goal specifications for product development.	Valid during the design phase
Preliminary specification α-site	This datasheet contains preliminary data. Additional data may be published later; could include simulation results.	Valid before characterization phase
Preliminary specification β-site	This datasheet contains also characterization results.	Valid before the industrialization phase
Product specification	This datasheet contains final product specification.	Valid for production purposes
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

12.1 Life Support Applications

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. e2v customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify e2v for any damages resulting from such improper use or sale.

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