Data Sheet

ADuM3100

Digital Isolator, Enhanced System-Level ESD Reliability

FEATURES

- Enhanced system-level ESD performance per IEC 61000-4-x
- High data rate: dc to 100 Mbps (NRZ)
- Compatible with 3.3 V and 5.0 V operation/level translation
- 105°C maximum operating temperature
- Low power operation
  - 5 V operation
    - 2.0 mA maximum @ 1 Mbps
    - 5.6 mA maximum @ 25 Mbps
    - 18 mA maximum @ 100 Mbps
  - 3.3 V operation
    - 1.1 mA maximum @ 1 Mbps
    - 4.2 mA maximum @ 25 Mbps
    - 8.3 mA maximum @ 50 Mbps
- RoHS-compliant, 8-lead SOIC
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL 1577
    - V_{ISO} = 2500 V rms for 1 minute
  - IEC / EN / CSA 62368-1
  - IEC / CSA 61010-1
  - CQC GB4943.1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 560 V peak

APPLICATIONS

- Digital fieldbus isolation
- Opto-isolator replacement
- Computer-peripheral interface
- Microprocessor system interface
- General instrumentation and data acquisition

FUNCTIONAL BLOCK DIAGRAM

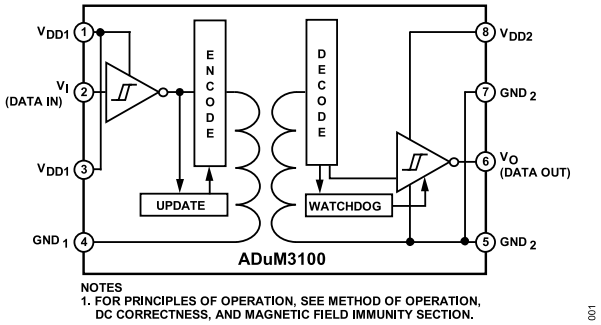

Figure 1.

GENERAL DESCRIPTION

The ADuM3100[1] is a digital isolator based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives, such as optocoupler devices.

Configured as a pin-compatible replacement for existing high speed optocouplers, the ADuM3100 supports data rates as high as 25 Mbps and 100 Mbps.

The ADuM3100 operates with a voltage supply ranging from 3.0 V to 5.5 V, boasts a propagation delay of <18 ns and an edge asymmetry of <2 ns, and is compatible with temperatures up to 105°C. It operates at very low power, less than 2.0 mA of quiescent current (sum of both sides), and a dynamic current of less than 160 µA per Mbps of data rate. Unlike other optocoupler alternatives, the ADuM3100 provides dc correctness with a patented refresh feature that continuously updates the output signal.

The ADuM3100 is offered in two grades. The ADuM3100AR and ADuM3100BR can operate up to a maximum temperature of 105°C and support data rates up to 25 Mbps and 100 Mbps, respectively.

In comparison to the ADuM1100 digital isolator, the ADuM3100 contains various circuit and layout changes to provide increased capability relative to system-level IEC 61000-4-x testing (ESD/burst/surge). The precise capability in these tests for either the ADuM1100 or ADuM3100 is strongly determined by the design and layout of the user's board or module. For more information, see the AN-793 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products.*

[1] Protected by U.S. Patents 5,952,849; 6,525,566; 6,922,080; 6,903,578; 6,873,065; 7,075,329 and other pending patents.

Rev. E

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REVISION HISTORY

1/2025—Rev. D to Rev. E

Changes to Features Section ... 1
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Added Maximum Data Rate and Minimum Pulse Width Options ... 17

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS, 5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DD1 (Q)}$		1.3	1.8	mA	V_I = 0 V or V_{DD1}
Output Supply Current, Quiescent	$I_{DD2 (Q)}$		0.15	0.25	mA	V_I = 0 V or V_{DD1}
Input Supply Current (25 Mbps) (See Figure 4)	$I_{DD1 (25)}$		3.2	4.5	mA	12.5 MHz logic signal freq.
Output Supply Current[1] (25 Mbps) (See Figure 5)	$I_{DD2 (25)}$		0.6	1.1	mA	12.5 MHz logic signal freq.
Input Supply Current (100 Mbps) (See Figure 4)	$I_{DD1 (100)}$		10	15	mA	50 MHz logic signal freq.
Output Supply Current[1] (100 Mbps) (See Figure 5)	$I_{DD2 (100)}$		2.1	2.9	mA	50 MHz logic signal freq., ADuM3100BRZ only
Input Current	I_I	−10	+0.01	+10	µA	0 V ≤ V_{IN} ≤ V_{DD1}
Logic High Output Voltage	V_{OH}	V_{DD2} − 0.1	5.0		V	I_O = −20 µA, V_I = V_{IH}
		V_{DD2} − 0.8	4.6		V	I_O = −4 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.03	0.1	V	I_O = 400 µA, V_I = V_{IL}
			0.3	0.8	V	I_O = 4 mA, V_I = V_{IL}
SWITCHING SPECIFICATIONS						
For ADuM3100ARZ						
Minimum Pulse Width[2]	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		25			Mbps	C_L = 15 pF, CMOS signal levels
For ADuM3100BRZ						
Minimum Pulse Width[3]	PW		6.7	10	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		100	150		Mbps	C_L = 15 pF, CMOS signal levels
For All Grades						
Propagation Delay Time to Logic Low Output[4, 5] (See Figure 6)	t_{PHL}		10.5	18	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Time to Logic High Output[4, 5] (See Figure 6)	t_{PLH}		10.5	18	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion $\|t_{PLH} - t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature[6]			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature)[5, 7]	t_{PSK1}			8	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature,Supplies)[5, 7]	t_{PSK2}			6	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time	t_R, t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic Low/High Output[8]	$\|CM_L\|$, $\|CM_H\|$	25	35		kV/µs	V_I = 0 V or V_{DD1}, V_{CM} = 1000 V
Input Dynamic Supply Current[9]	$I_{DDI (D)}$		0.09		mA/Mbps	
Output Dynamic Supply Current[9]	$I_{DDO (D)}$		0.02		mA/Mbps	

[1] Output supply current values are with no output load present. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

[4] t_{PHL} is measured from the 50% level of the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} is measured from the 50% level of the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.

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[5] Because the input thresholds of the ADuM3100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulse-width distortion can be affected by slow input rise/fall times. See the System-Level ESD Considerations and Enhancements section and Figure 13 to for information on the impact of given input rise/fall times on these parameters.

[6] Pulse-width distortion change vs. temperature is the absolute value of the change in pulse-width distortion for a 1°C change in operating temperature.

[7] t_{PSK1} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature and output load within the recommended operating conditions. t_{PSK2} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[8] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common mode is slewed.

[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

See notes on Page 6.

ELECTRICAL SPECIFICATIONS, 3.3 V OPERATION

All voltages are relative to their respective ground. 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DD1 (Q)}$		0.7	0.9	mA	V_I = 0 V or V_{DD1}
Output Supply Current, Quiescent	$I_{DD2 (Q)}$		0.1	0.2	mA	V_I = 0 V or V_{DD1}
Input Supply Current (25 Mbps) (See Figure 4)	$I_{DD1 (25)}$		2.6	3.4	mA	12.5 MHz logic signal freq.
Output Supply Current[1] (25 Mbps) (See Figure 5)	$I_{DD2 (25)}$		0.4	0.8	mA	12.5 MHz logic signal freq.
Input Supply Current (50 Mbps) (See Figure 4)	$I_{DD1 (50)}$		4.6	6.6	mA	25 MHz logic signal freq.,ADuM3100BRZ only
Output Supply Current[1] (50 Mbps) (See Figure 5)	$I_{DD2 (50)}$		0.7	1.7	mA	25 MHz logic signal freq., ADuM3100BRZ only
Input Current	I_I	−10	+0.01	+10	µA	0 V ≤ V_{IN} ≤ V_{DD1}
Logic High Output Voltage	V_{OH}	V_{DD2} − 0.1	3.3		V	I_O = −20 µA, V_I = V_{IH}
		V_{DD2} − 0.5	3.0		V	I_O = −2.5 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = 20 µA, V_I = V_{IL}
			0.04	0.1	V	I_O = 400 µA, V_I = V_{IL}
			0.3	0.4	V	I_O = 2.5 mA, V_I = V_{IL}
SWITCHING SPECIFICATIONS						
For ADuM3100ARZ						
Minimum Pulse Width[2]	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		25			Mbps	C_L = 15 pF, CMOS signal levels
For ADuM3100BRZ						
Minimum Pulse Width[2]	PW		10	20	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		50	100		Mbps	C_L = 15 pF, CMOS signal levels
For All Grades						
Propagation Delay Time to Logic Low Output[4, 5] (See Figure 7)	t_{PHL}		14.5	28	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Time to Logic High Output[4, 5] (See Figure 7)	t_{PLH}		15.0	28	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion $\|t_{PLH} - t_{PHL}\|$[5]	PWD		0.5	3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature[6]			10		ps/°C	C_L = 15 pF, CMOS signal levels

SPECIFICATIONS

Table 2. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Propagation Delay Skew (Equal Temperature)[5, 7]	t_{PSK1}			15	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature, Supplies)[5, 7]	t_{PSK2}			12	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time	t_R, t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic Low/High Output[8]	$\|CM_L\|$, $\|CM_H\|$	25	35		kV/µs	V_I = 0 V or V_{DD1}, V_{CM} = 1000 V, transient magnitude = 800 V
Input Dynamic Supply Current[9]	$I_{DDI (D)}$		0.08		mA/Mbps	
Output Dynamic Supply Current[9]	$I_{DDO (D)}$		0.01		mA/Mbps	

1 Output supply current values are with no output load present. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

2 The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

3 The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

4 t_{PHL} is measured from the 50% level of the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} is measured from the 50% level of the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.

5 Because the input thresholds of the ADuM3100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulse-width distortion can be affected by slow input rise/fall times. See the System-Level ESD Considerations and Enhancements section and Figure 13 to for information on the impact of given input rise/fall times on these parameters.

6 Pulse-width distortion change vs. temperature is the absolute value of the change in pulse-width distortion for a 1°C change in operating temperature.

7 t_{PSK1} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature and output load within the recommended operating conditions. t_{PSK2} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

8 CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common mode is slewed.

9 Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

ELECTRICAL SPECIFICATIONS, MIXED 5 V/3 V OR 3 V/5 V OPERATION

All voltages are relative to their respective ground. 5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V or V_{DD1} = 5 V, V_{DD2} = 3.3 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI (Q)}$					
5 V/3 V Operation			1.3	1.8	mA	
3 V/5 V Operation			0.7	0.9	mA	
Output Supply Current[1], Quiescent	$I_{DDO (Q)}$					
5 V/3 V Operation			0.1	0.2	mA	
3 V/5 V Operation			0.15	0.25	mA	
Input Supply Current, 25 Mbps	$I_{DDI (25)}$					
5 V/3 V Operation			3.2	4.5	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			2.6	3.4	mA	12.5 MHz logic signal freq.
Output Supply Current[1], 25 Mbps	$I_{DDO (25)}$					
5 V/3 V Operation			0.4	0.8	mA	12.5 MHz logic signal freq.
3 V/5 V Operation			0.6	1.1	mA	12.5 MHz logic signal freq.
Input Supply Current, 50 Mbps	$I_{DDI (50)}$					

SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
5 V/3 V Operation			5.5	8.0	mA	25 MHz logic signal freq.
3 V/5 V Operation			4.6	6.6	mA	25 MHz logic signal freq.
Output Supply Current[1], 50 Mbps	$I_{DDO (50)}$					
5 V/3 V Operation			0.7	1.7	mA	25 MHz logic signal freq.
3 V/5 V Operation			1.1	1.6	mA	25 MHz logic signal freq.
Input Currents	I_{IA}	−10	+0.01	+10	μA	$0 \le V_{IA}, V_{IB}, V_{IC}, V_{ID} \le V_{DD1}$ or V_{DD2}
Logic High Output Voltage, 5 V/3 V Operation	V_{OH}	V_{DD2} − 0.1	3.3		V	I_O = −20 μA, $V_I = V_{IH}$
		V_{DD2} − 0.5	3.0		V	I_O = −2.5 mA, $V_I = V_{IH}$
Logic Low Output Voltage, 5 V/3 V Operation	V_{OL}		0.0	0.1	V	I_O = 20 μA, $V_I = V_{IL}$
			0.04	0.1	V	I_O = 400 μA, $V_I = V_{IL}$
			0.3	0.4	V	I_O = 2.5 mA, $V_I = V_{IL}$
Logic High Output Voltage, 3 V/5 V Operation	V_{OH}	V_{DD2} − 0.1	5.0		V	I_O = −20 μA, $V_I = V_{IH}$
		V_{DD2} − 0.8	4.6		V	I_O = −4 mA, $V_I = V_{IH}$
Logic Low Output Voltage, 3 V/5 V Operation	V_{OL}		0.0	0.1	V	I_O = 20 μA, $V_I = V_{IL}$
			0.03	0.1	V	I_O = 400 μA, $V_I = V_{IL}$
			0.3	0.8	V	I_O = 4 mA, $V_I = V_{IL}$
SWITCHING SPECIFICATIONS						
For ADuM3100ARZ						
Minimum Pulse Width[2]	PW			40	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		25			Mbps	C_L = 15 pF, CMOS signal levels
For ADuM3100BRZ						
Minimum Pulse Width[2]	PW			20	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[3]		50			Mbps	C_L = 15 pF, CMOS signal levels
For All Grades						
Propagation Delay Time to Logic Low/High Output[4, 5]	t_{PHL}, t_{PLH}					
5 V/3 V Operation (See Figure 8)			13	21	ns	C_L = 15 pF, CMOS signal levels
3 V/5 V Operation (See Figure 9)			16	26	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[5]	PWD					
5 V/3 V Operation			0.5	2	ns	C_L = 15 pF, CMOS signal levels
3 V/5 V Operation			0.5	3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature[6]						
5 V/3 V Operation			3		ps/°C	C_L = 15 pF, CMOS signal levels
3 V/5 V Operation			10		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature)[5, 7]	t_{PSK1}					
5 V/3 V Operation				12	ns	C_L = 15 pF, CMOS signal levels
3 V/5 V Operation				15	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew (Equal Temperature,Supplies)[5, 7]	t_{PSK2}					
5 V/3 V Operation				9	ns	C_L = 15 pF, CMOS signal levels
3 V/5 V Operation				12	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R, t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic Low/High Output[8]	$\lvert CM_L \rvert$, $\lvert CM_H \rvert$	25	35		kV/μs	V_I = 0 V or V_{DD1}, V_{CM} = 1000 V, transient magnitude = 800 V
Input Dynamic Supply Current per Channel[9]	$I_{DDI (D)}$					
5 V/3 V Operation			0.09		mA/Mbps	
3 V/5 V Operation			0.08		mA/Mbps	
Output Dynamic Supply Current per Channel[9]	$I_{DDO (D)}$					
5 V/3 V Operation			0.01		mA/Mbps	
3 V/5 V Operation			0.02		mA/Mbps	

SPECIFICATIONS

[1] Output supply current values are with no output load present. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

[2] The minimum pulse width is the shortest pulse width at which the specified pulse-width distortion is guaranteed.

[3] The maximum data rate is the fastest data rate at which the specified pulse-width distortion is guaranteed.

[4] t_{PHL} is measured from the 50% level of the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} is measured from the 50% level of the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.

[5] Because the input thresholds of the ADuM3100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulse-width distortion can be affected by slow input rise/fall times. See the System-Level ESD Considerations and Enhancements section and Figure 13 to for information on the impact of given input rise/fall times on these parameters.

[6] Pulse-width distortion change vs. temperature is the absolute value of the change in pulse-width distortion for a 1°C change in operating temperature.

[7] t_{PSK1} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature and output load within the recommended operating conditions. t_{PSK2} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[8] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common mode is slewed.

[9] Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 4 and Figure 5 for information on supply current variation with logic signal frequency. See the Power Consumption section for guidance on calculating the input and output supply currents for a given data rate and output load.

PACKAGE CHARACTERISTICS

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	θ_{JCI}		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	θ_{JCO}		41		°C/W	
Package Power Dissipation	P_{PD}			240	mW	

[1] The device is considered a 2-terminal device; Pin 1, Pin 2, Pin 3, and Pin 4 are shorted together, and Pin 5, Pin 6, Pin 7, and Pin 8 are shorted together.

[2] Input capacitance is measured at Pin 2 (VI).

REGULATORY INFORMATION

The ADuM3100 certifications approvals are listed in Table 5.

Table 5.

UL	CSA	CQC	VDE
UL 1577[1]	IEC / EN / CSA 62368-1	CQC GB 4943.1	DIN EN IEC 60747-17 (VDE 0884-17)[2]
Single Protection, 2500 V rms	Basic Insulation, 400 V rms	Basic Insulation, 400 V rms	Reinforced insulation, 560 V peak
	Reinforced Insulation, 150 V rms	Reinforced Insulation, 150 V rms	
	IEC / CSA 61010-1		
	Basic Insulation, 300 V rms		
	Reinforced Insulation, 150 V rms		
File E214100	File 205078	Certificate No. CQC14001117248	Certificate No. 40011599

[1] In accordance with UL 1577, each ADuM3100 is proof tested by applying an insulation test voltage ≥3000 V rms for 1 second (current leakage detection limit = 5 µA).

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each ADuM3100 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC).

SPECIFICATIONS

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	4[1, 2]	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		18	µm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group per IEC 60664-1

[1] In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 meters.

[2] Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits. The asterisk (*) on the package denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 7.

Description	Conditions	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
≤ 150 V rms			I to IV	
≤ 300 V rms			I to III	
≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	560	V peak
Maximum Working Insulation Voltage		V_{IOWM}	396	V rms
Input-to-Output Test Voltage, Method B1	V_{IORM} × 1.875 = $V_{pd(m)}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V peak
Input-to-Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	V_{IORM} × 1.6 = $V_{pd(m)}$, t_m = 60 sec, partial discharge < 5 pC	$V_{pd(m)}$	896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = $V_{pd(m)}$, t_m = 60 sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V peak
Maximum Transient Isolation Voltage	V_{TEST} = 1.2 × V_{IOTM}, t =1s (100% production)	V_{IOTM}	4000	V peak
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	4000	V peak
Maximum Surge Isolation Voltage	V_{TEST} ≥ 1.3 × V_{IMP} (sample test), tested in oil, waveform per IEC 61000-4-5	V_{IOSM}	10000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	170	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

SPECIFICATIONS

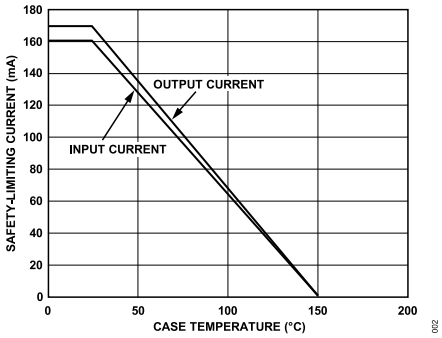


Figure 2. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

RECOMMENDED OPERATING CONDITIONS

Table 8.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.0	5.5	V
Logic High Input Voltage, 5 V Operation (See Figure 10 and Figure 11)	V_{IH}	2.0	V_{DD1}	V
Logic Low Input Voltage, 5 V Operation[1, 2] (See Figure 10 and Figure 11)	V_{IL}	0.0	0.8	V
Logic High Input Voltage, 3.3 V Operation[1, 2] (See Figure 10 and Figure 11)	V_{IH}	1.5	V_{DD1}	V
Logic Low Input Voltage, 3.3 V Operation[1, 2] (See Figure 10 and Figure 11)	V_{IL}	0.0	0.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective ground.

[2] Input switching thresholds have 300 mV of hysteresis. See the Method of Operation, DC Correctness, and Magnetic Field Immunity section, Figure 18, and Figure 19 for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Min	Max	Unit
Storage Temperature (T_{ST})	−55	+150	°C
Ambient Operating Temperature (T_A)	−40	+105	°C
Supply Voltages (V_{DD1}, V_{DD2})[1]	−0.5	+6.5	V
Input Voltage (V_I)[1]	−0.5	V_{DD1} + 0.5	V
Output Voltage (V_O)[1]	−0.5	V_{DD2} + 0.5	V
Average Current, per Pin[2]			
Temperature ≤ 105°C	−25	+25	mA
Common-Mode Transients[3]	−100	+100	kV/µs

[1] All voltages are relative to their respective ground.

[2] See Figure 2 for information on maximum allowable current for various temperatures.

[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

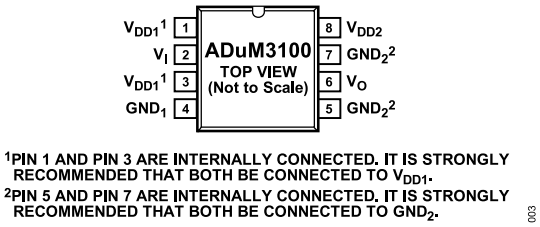
TRUTH TABLE

Table 10. Truth Table

V_I Input	V_{DD1} State	V_{DD2} State	V_O Output
H	Powered	Powered	H
L	Powered	Powered	L
X	Unpowered	Powered	H[1]
X	Powered	Unpowered	X1

[1] V_O returns to V_I state within 1 µs of power restoration.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



[1]PIN 1 AND PIN 3 ARE INTERNALLY CONNECTED. IT IS STRONGLY RECOMMENDED THAT BOTH BE CONNECTED TO V_{DD1}.
[2]PIN 5 AND PIN 7 ARE INTERNALLY CONNECTED. IT IS STRONGLY RECOMMENDED THAT BOTH BE CONNECTED TO GND_2.

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Input Supply Voltage, 3.0 V to 5.5 V
2	V_I	Logic Input
3	V_{DD1}	Input Supply Voltage, 3.0 V to 5.5 V
4	GND_1	Input Ground
5	GND_2	Output Ground
6	V_O	Logic Output
7	GND_2	Output Ground
8	V_{DD2}	Output Supply Voltage, 3.0 V to 5.5 V

TYPICAL PERFORMANCE CHARACTERISTICS

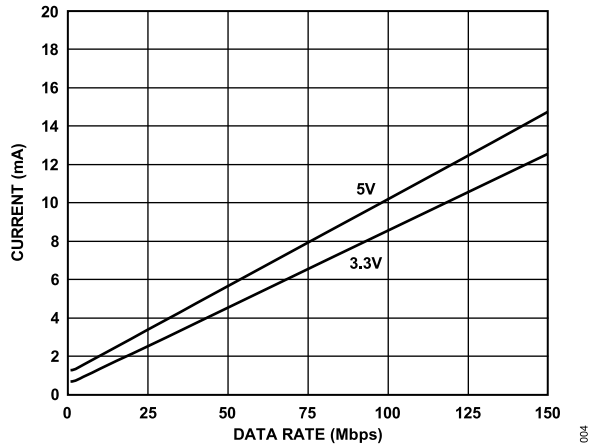


Figure 4. Typical Input Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation

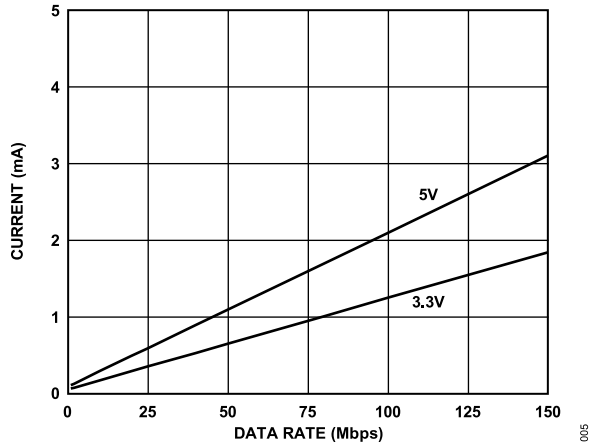


Figure 5. Typical Output Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation

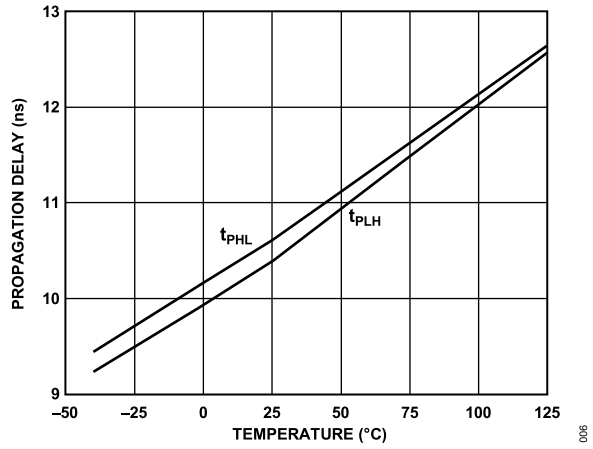


Figure 6. Typical Propagation Delays vs. Temperature, 5 V Operation

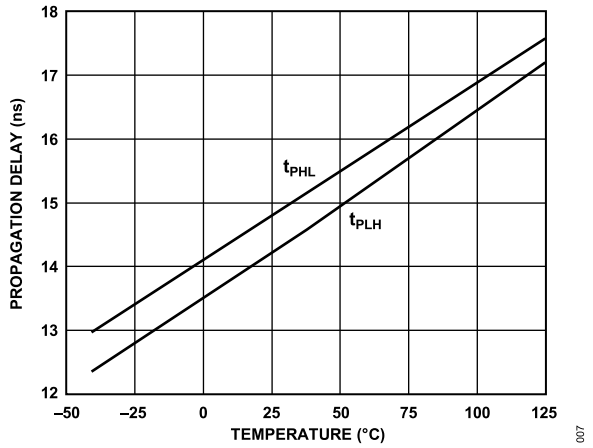


Figure 7. Typical Propagation Delays vs. Temperature, 3.3 V Operation

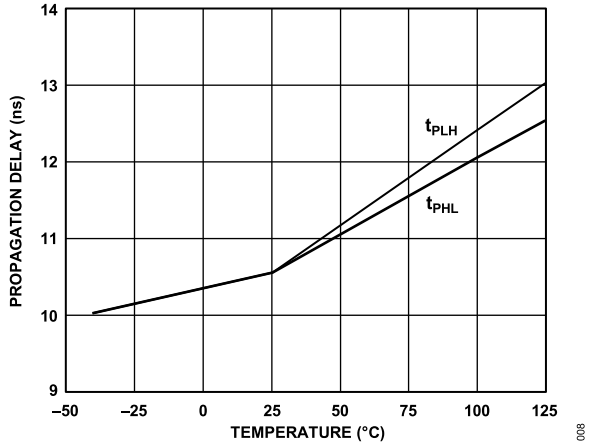


Figure 8. Typical Propagation Delays vs. Temperature, 5 V/3 V Operation

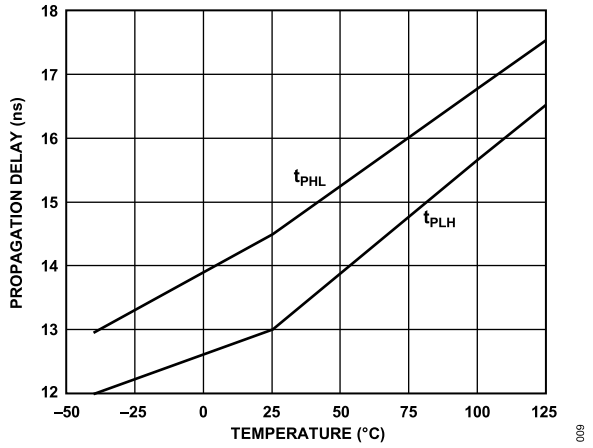


Figure 9. Typical Propagation Delays vs. Temperature, 3 V/5 V Operation

TYPICAL PERFORMANCE CHARACTERISTICS

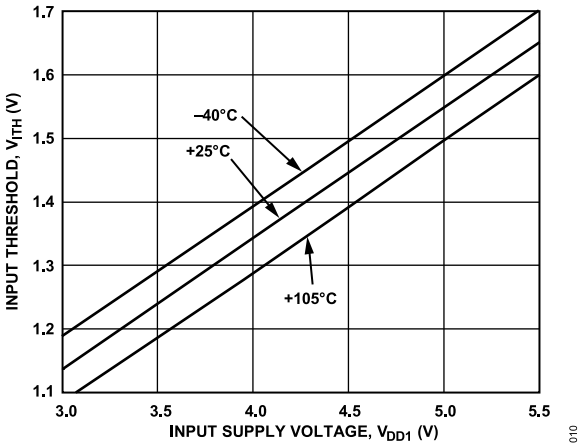


Figure 10. Typical Input Voltage Switching Threshold, Low-to-High Transition

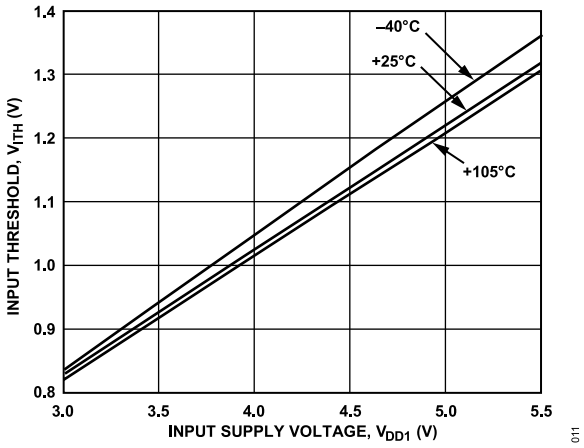


Figure 11. Typical Input Voltage Switching Threshold, High-to-Low Transition

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM3100 digital isolator requires no external interface circuitry for the logic interfaces. A bypass capacitor is recommended at the input and output supply pins. The input bypass capacitor can conveniently connect between Pin 3 and Pin 4 (see Figure 12). Alternatively, the bypass capacitor can be located between Pin 1 and Pin 4. The output bypass capacitor can be connected between Pin 7 and Pin 8 or Pin 5 and Pin 8. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm.

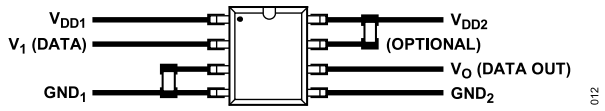


Figure 12. Recommended Printed Circuit Board Layout

See the AN-1109 Application Note for board layout guidelines.

SYSTEM-LEVEL ESD CONSIDERATIONS AND ENHANCEMENTS

System-level ESD reliability (for example, per IEC 61000-4-x) is highly dependent on system design, which varies widely by application. The ADuM3100 incorporates many enhancements to make ESD reliability less dependent on system design. The enhancements include

- ESD protection cells added to all input/output interfaces.
- Key metal trace resistances reduced using wider geometry and paralleling of lines with vias.
- The SCR effect inherent in CMOS devices minimized by use of guarding and isolation techniques between PMOS and NMOS devices.
- Areas of high electric field concentration eliminated using 45° corners on metal traces.
- Supply pin overvoltage prevented with larger ESD clamps between each supply pin and its respective ground.

While the ADuM3100 improves system-level ESD reliability, it is no substitute for a robust system-level design. See the AN-1109 Application Note, *ESD/Latch-Up Considerations with iCoupler Isolation Products* for detailed recommendations on board layout and system-level design.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay time describes the length of time it takes for a logic signal to propagate through a component. Propagation delay time to logic low output and propagation delay time to logic high output refer to the duration between an input signal transition and the respective output signal transition (see Figure 13).

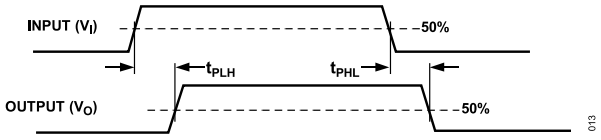


Figure 13. Propagation Delay Parameters

Pulse-width distortion is the maximum difference between t_{PLH} and t_{PHL} and provides an indication of how accurately the input signal timing is preserved in the component output signal. Propagation delay skew is the difference between the minimum and maximum propagation delay values among multiple ADuM3100 components operated at the same operating temperature and having the same output load.

Depending on the input signal rise/fall time, the measured propagation delay based on the input 50% level can vary from the true propagation delay of the component (as measured from its input switching threshold). This is due to the fact that the input threshold, as is the case with commonly used optocouplers, is at a different voltage level than the 50% point of typical input signals. This propagation delay difference is

$$\Delta_{LH} = t'_{PLH} - t_{PLH} = (t_r/0.8\ V_I)(0.5\ V_1 - V_{ITH\ (L\text{-}H)})$$

$$\Delta_{HL} = t'_{PHL} - t_{PHL} = (t_f/0.8\ V_I)(0.5\ V_1 - V_{ITH\ (H\text{-}L)})$$

where:
t_{PLH}, t_{PHL} are propagation delays as measured from the input 50%.
t'_{PLH}, t'_{PHL} are propagation delays as measured from the input switching thresholds.
t_r, t_f are input 10% to 90% rise/fall time. V_I is the amplitude of input signal (0 V to V_I levels assumed).
$V_{ITH\ (L-H)}$, $V_{ITH\ (H-L)}$ are input switching thresholds.

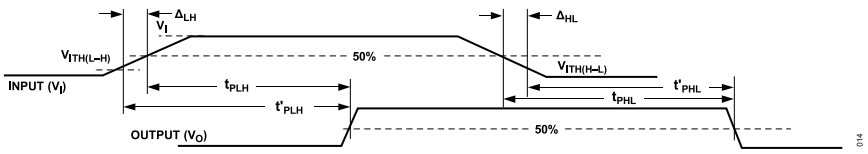


Figure 14. Impact of Input Rise/Fall Time on Propagation Delay

APPLICATIONS INFORMATION

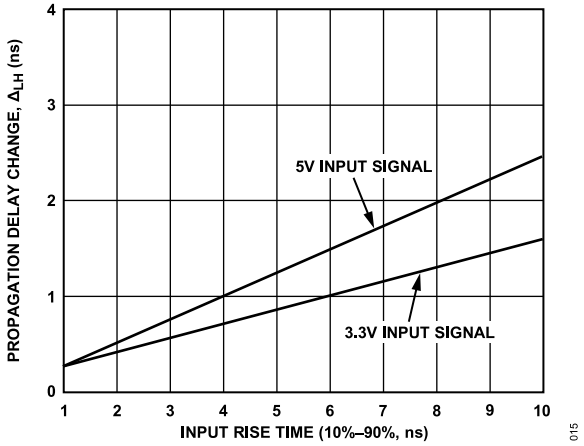


Figure 15. Typical Propagation Delay Change Due to Input Rise Time Variation (for V_{DD1} = 3.3 V and 5 V)

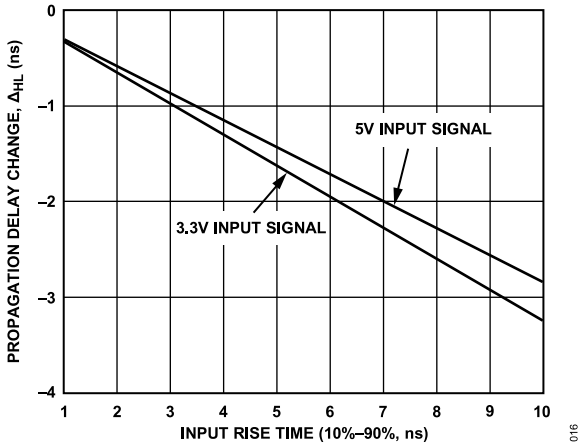


Figure 16. Typical Propagation Delay Change Due to Input Fall Time Variation (for V_{DD1} = 3.3 V and 5 V)

The impact of the slower input edge rates can also affect the measured pulse-width distortion as based on the input 50% level. This impact can either increase or decrease the apparent pulse-width distortion depending on the relative magnitudes of t_{PHL}, t_{PLH}, and PWD. The case of interest here is the condition that leads to the largest increase in pulse-width distortion. The change in this case is given by

$\Delta_{PWD} = PWD' - PWD = \Delta_{LH} - \Delta_{HL} =$

$(t/0.8\ V_1)(V - V_{ITH\ (L\text{-}H)} - V_{ITH\ (H\text{-}L)})$, (for $t = t_r = t_f$)

where:
$PWD = |t_{PLH} - t_{PHL}|$.
$PWD' = |t'_{PLH} - t'_{PHL}|$.

This adjustment in pulse-width distortion is plotted as a function of input rise/fall time in Figure 17.

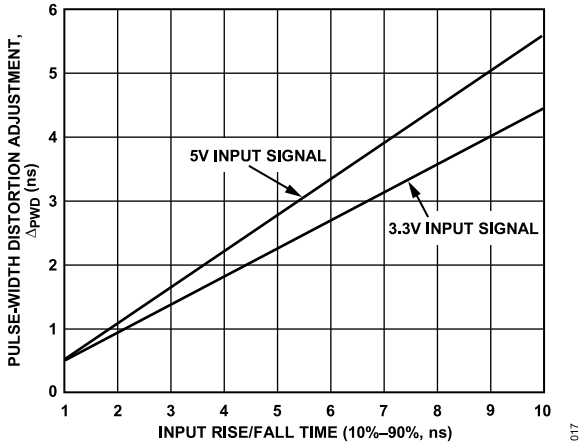


Figure 17. Typical Pulse-Width Distortion Adjustment Due to Input Rise/Fall Time Variation (for V_{DD1} = 3.3 V and 5 V)

METHOD OF OPERATION, DC CORRECTNESS, AND MAGNETIC FIELD IMMUNITY

Referring to Figure 1, the two coils act as a pulse transformer. Positive and negative logic transitions at the isolator input cause narrow (2 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and therefore either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic update pulse of the appropriate polarity is sent to ensure dc correctness at the output. If the decoder does not receive any of these update pulses for more than approximately 5 µs, the input side is assumed unpowered or nonfunctional, in which case the isolator output is forced to a logic high state by the watchdog timer circuit.

The limitation on the ADuM3100 magnetic field immunity is set by the condition in which induced voltage in the transformer-receiving coil is sufficiently large to either falsely set or reset the decoder. The analysis that follows defines the conditions under which this can occur. The ADuM3100 3.3 V operating condition is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output are greater than 1.0 V in amplitude. The decoder has sensing thresholds at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$V = (-d\beta/dt) \sum \pi r_n^2,\ n = 1, 2, \ldots, N$

where:
β is magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of *nth* turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM3100 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 18.

APPLICATIONS INFORMATION

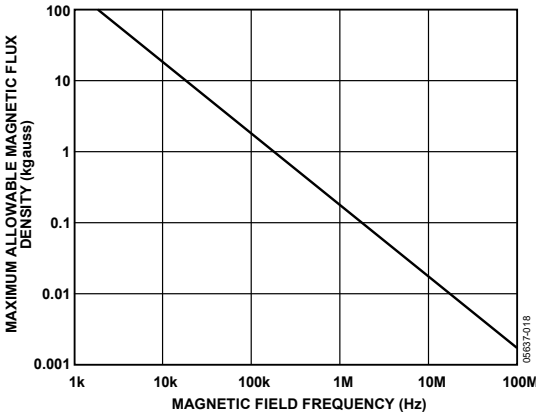


Figure 18. Maximum Allowable External Magnetic Field

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3100 transformers. Figure 19 shows the allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM3100 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted, a current of 0.5 kA would have to be placed 5 mm away from the ADuM3100 to affect the component's operation.

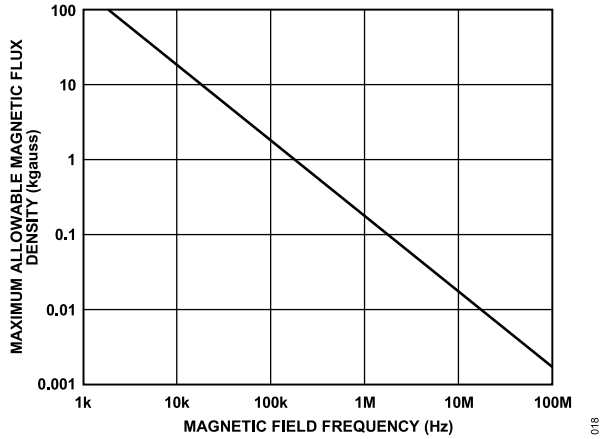


Figure 19. Maximum Allowable Current for Current-to-ADuM3100 Spacing

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current of the ADuM3100 isolator is a function of the supply voltage, the input data rate, and the output load.

The input supply current is given by

$$I_{DDI} = I_{DDI\,(Q)}\ f \leq 0.5 f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)}\ f > 0.5 f_r$$

The output supply current is given by

$$I_{DDO} = I_{DDO\,(Q)}\ f \leq 0.5 f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)}\ f > 0.5 f_r$$

where:
$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
C_L is output load capacitance (pF).
V_{DDO} is the output supply voltage (V).
f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).
f_r is the input stage refresh rate (Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
R-8	SOIC_N	8-Lead Standard Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM3100ARZ	−40°C to +105°C	8-Lead SOIC_N	Tube, 98	R-8
ADuM3100ARZ-RL7	−40°C to +105°C	8-Lead SOIC_N	Reel, 1000	R-8
ADuM3100BRZ	−40°C to +105°C	8-Lead SOIC_N	Tube, 98	R-8
ADuM3100BRZ-RL7	−40°C to +105°C	8-Lead SOIC_N	Reel, 1000	R-8

[1] Z = RoHS Compliant Part.

MAXIMUM DATA RATE AND MINIMUM PULSE WIDTH OPTIONS

Model[1]	Maximum Data Rate (Mbps)	Minimum Pulse Width (ns)
ADuM3100ARZ	25	40
ADuM3100ARZ-RL7	25	40
ADuM3100BRZ	100	10
ADuM3100BRZ-RL7	100	10

[1] Z = RoHS Compliant Part.