User Guide

EVAL-LTC7067-AZ

150V Dual High-Side MOSFET Gate Driver

General Description

The EVAL-LTC7067-AZ features the LTC®7067 in a flexible configuration as a non-synchronous step-down or as a non-synchronous step-up converter. EVAL-LTC7067-AZ also has a default set up to test LTC7067 only with a load capacitor. As both Gate returns are floating, LTC7067 can be configured to drive dual-high side MOSFET, or to drive high-side and low-side MOSFET. Typical performance is shown in *Table 1*.

This demo board features LTC7067, 150V Dual high-side MOSFET gate driver with overvoltage and undervoltage protections in a 12-pin MSE package. Refer to the LTC7067 data sheet for more detailed information.

Evaluation Circuit Photo

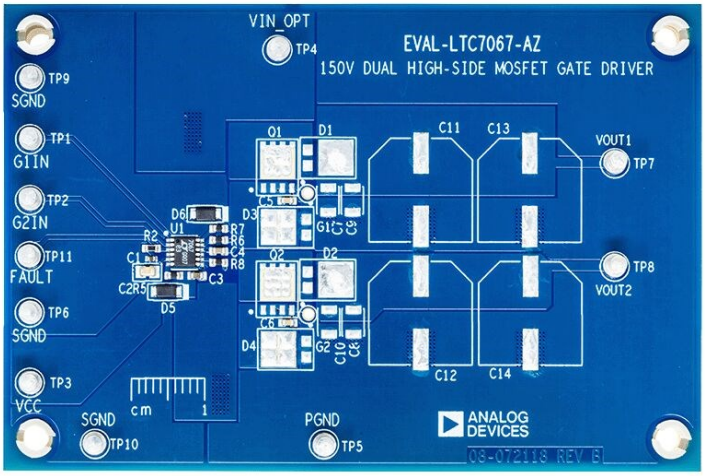

Table 1. Performance Summary (T_A = 25˚C)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN_OPT	V_{CC} = 10V			140	V
V_{CC}		4.5	10	14	V
G1IN/G2IN	V_{CC} = 10V	-0.3	5	6	V
G1 to G1RTN/G2 to G2RTN	VCC = 10V	9.4	9.6	9.8	V
G1IN/G2IN rising threshold				1.75	V
G1IN/G2IN falling threshold		0.5			V
Propagation delay	Rising		19		ns
	Falling		21		
Rise Time	V_{CC} = 10V, C_{LOAD} = 3.3nF		17		ns
Fall Time			15		ns

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Quick Start Procedure

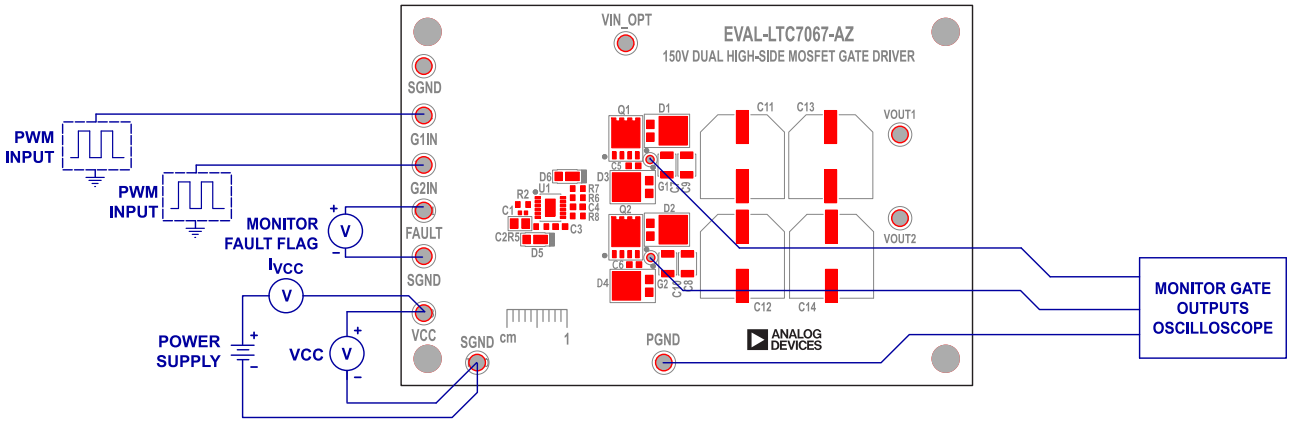


Figure 1. Test Set up

Caution: Do not turn on the power supply until all connections are completed.

- Connect the power supply to V_{CC} and GND.
- Connect one signal generator output to G1IN and GND, another to G2IN and GND. G1 and G2 can be tested altogether or separately.
- Turn on the power supply and adjust it to 10V.
- Adjust the signal generator to a pulse waveform of 50% duty cycle, 0-5V, 200kHz, turn on the signal generator.
- Connect the probes of an oscilloscope to G1/G2 and GND, G1IN/G2IN and GND for waveforms measurement.
- Verify the G1/G2 amplitude is 9.6V and follow the G1IN/G2IN inputs duty cycle and frequency. Adjust the frequency/duty cycle of G1IN/G2IN, expect the corresponding change of G1/G2.

Test with Default Load Capacitor

The board has a default set up to test the driver LTC7067 with load capacitors C5 and C6. The typical value of these capacitors are 3.3nF. Typical waveforms of rising/falling time, propagation delays are below.

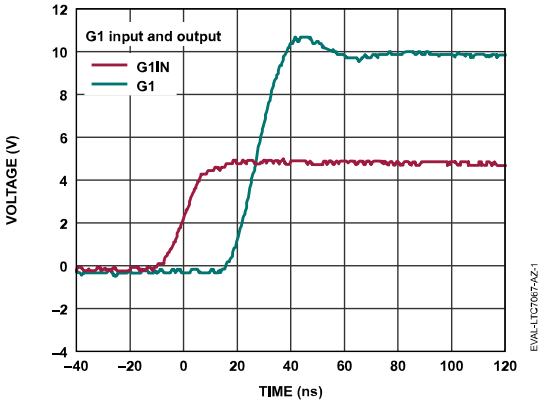


Figure 2. G1IN and G1 Rising, C_{LOAD} = 3.3nF

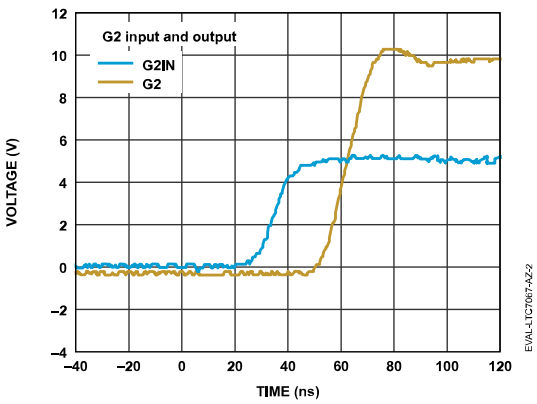


Figure 3. G2IN and G2 Rising, C_{LOAD} = 3.3nF

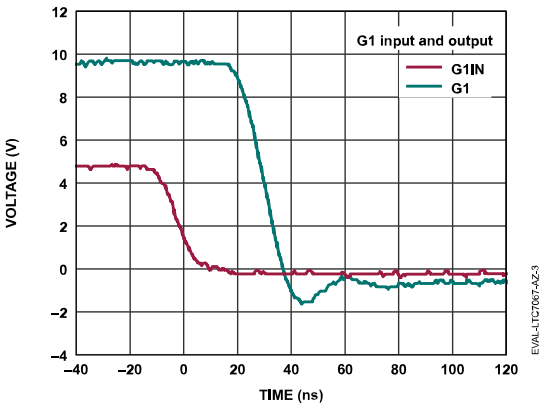


Figure 4. G1IN and G1 Falling, C_{LOAD} = 3.3nF

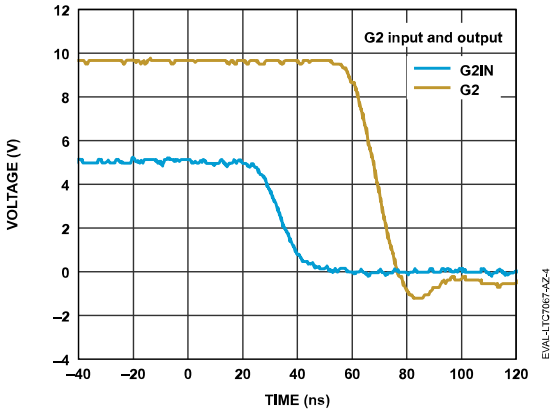


Figure 5. G2IN and G2 Falling, C_{LOAD} = 3.3nF

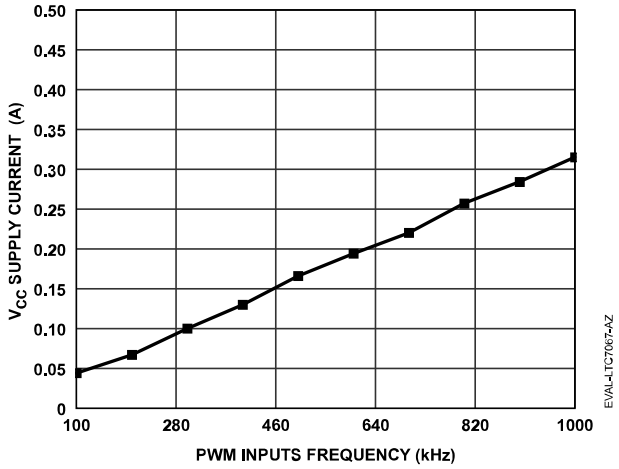


Figure 6. V_{CC} Supply Current vs. PWM Inputs Frequency, V_{CC} = 10V, C_{LOAD} = 3.3nF

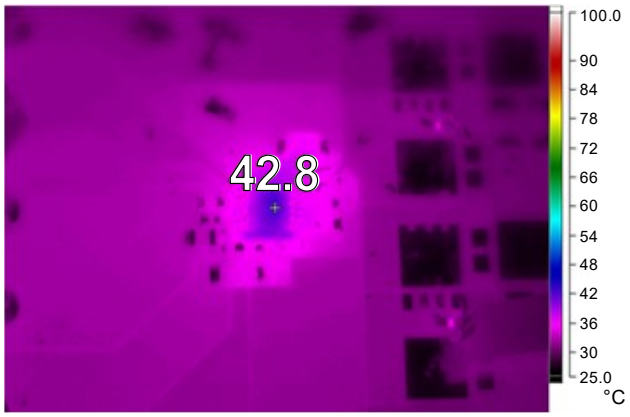


Figure 7. Thermal Picture at V_{CC} =10V, Both G1 and G2 are running at 2MHz, C_{LOAD} = 3.3nF, no forced air flow

Test in Non-synchronous Step-down Converter

The EVAL-LTC7067-AZ can be configured as a simple open-loop non-synchronous buck converter. To set up, populate Q1, D3, and cut the copper on D3 to isolate the cathode of D3 from GND, Q1 will be the control MOSFET of buck, and D3 will conduct the freewheeling inductor current when Q1 is off. Set the corresponding duty cycle and frequency of G1IN, populate inductor across Q1 source to VOUT1, and simply short VIN_OPT to Q1 drain. Choose the output capacitors, switching frequency, duty cycle, and sinking current by design. VOUT1 is the output. VIN_OPT is the input, to test EVAL-LTC7067-AZ in a buck configuration, another power supply connected to VIN_OPT and GND is needed, choose input capacitors by design. Note that the G1_RTN will see VIN_OPT voltage and G1VCC will see VIN_OPT+VCC-V_{DIODE}, where V_{DIODE} is the forward voltage drop of D6, both G1RTN and G1VCC shouldn't exceed 150V.

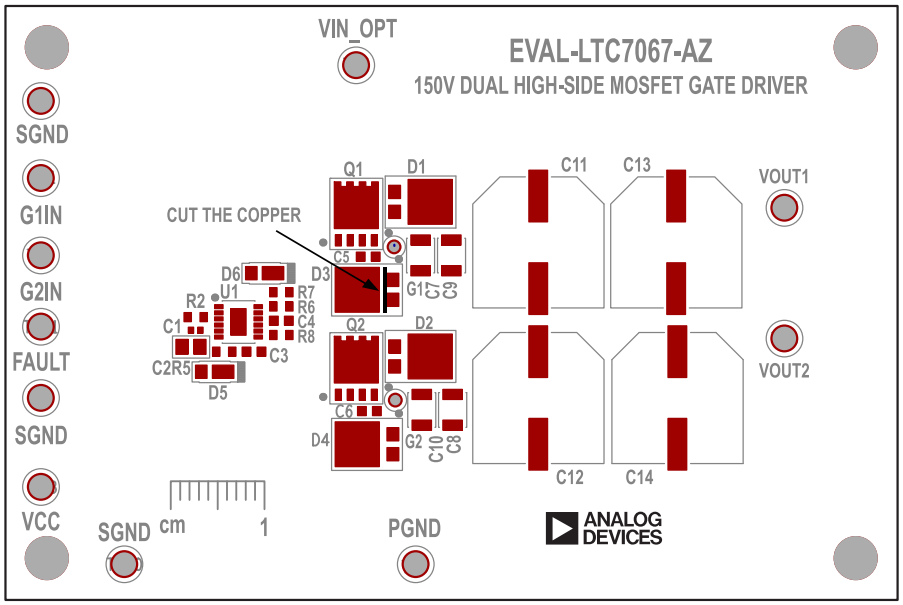


Figure 8. Test with Buck Converter Set up

Test in Non-synchronous Step-up Converter

The EVAL-LTC7067-AZ can be configured as a simple open-loop non-synchronous boost converter. To set up, populate Q2, D2. Populate inductor from V_{IN} to Q2 drain. Set the corresponding duty cycle and frequency of G2IN. Choose the output capacitors, switching frequency, duty cycle, and sinking current by design. VOUT2 is the output. VIN_OPT is the input, to test EVAL-LTC7067-AZ in a boost configuration, another power supply connected to VIN_OPT and GND is needed, choose input capacitors by design.

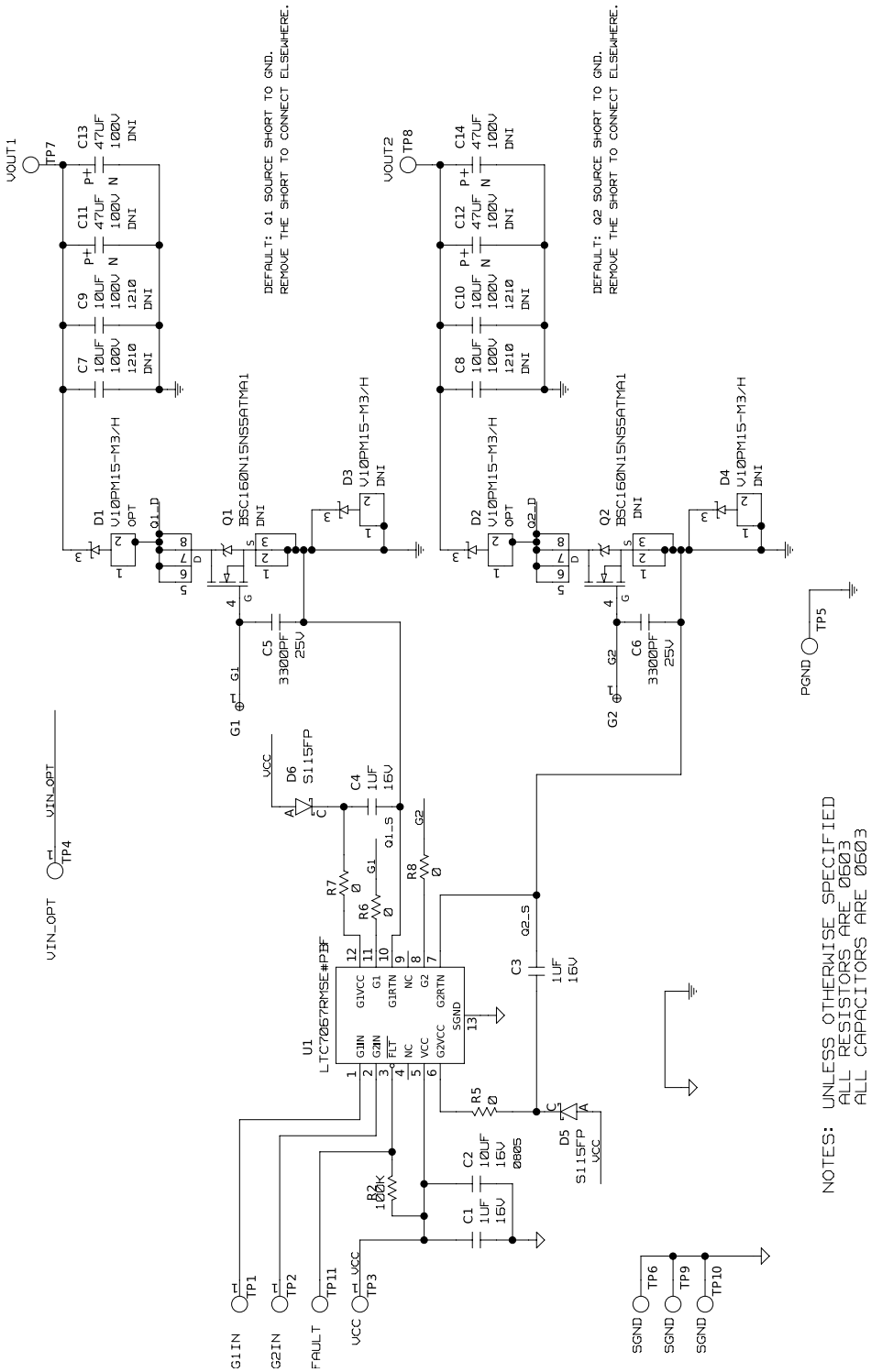
FAULT

FAULT is an open drain output of an internal N-channel MOSFET, there is a pull-up resistor from FAULT to V_{CC} on board. FAULT will be pulled low during V_{CC} UVLO/OVLO, typical V_{CC} UVLO voltage is 4.3V, V_{CC} OVLO voltage is 14.6V, or over temperature (180˚C). After all the faults are cleared, FAULT will be pulled up to V_{CC}.

EVAL-LTC7067-AZ Bill of Materials

ITEM	QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	1	C1	CAP CER 1uF 16V 20% X5R 0402	MURATA GRM155R61C105MA12D
2	1	C2	CAP CER 10uF 16V 10% X5R 0805	MURATA GRM21BR61C106KE15L
3	2	C3,C4	CAP CER 1uF 16V 10% X7R 0603	AVX 0603YC105KAT2A2
4	2	C5,C6	CAP CER 3300PF 25V 10% X7R 0603	WALSIN TECHNOLOGY 0603B332K250CT
5	2	D5,D6	DIO SCHOTTKY 150V 1A SOD123HE AEC-Q101	ONSEMI S115FP
6	1	R2	RES SMD 100K Ohm 1% 1/10W 0603 AEC-Q200	PANASONIC ERJ-3EKF1003V
7	4	R5,R6,R7,R8	RES SMD 0 Ohm 0603 AEC-Q200	VISHAY CRCW0603000ZRT1
8	1	U1	IC-ADI 150V DUAL HIGH SIDE MOSFET GATE DRIVER	ANALOG DEVICES LTC7067RMSE#PBF
OPTIONAL CIRCUIT COMPONENTS				
1	4	C7,C8,C9,C10	CAP CER 10UF 100V 10% X7S 1210	MURATA GRM32EC72A106KE05L
2	4	C11,C12,C13,C14	CAP ALUM ELECT 47UF 100V 20% 12.5X13.5MM AEC-Q200 500MA 5000H	PANASONIC EEV-FK2A470Q
3	2	D1,D2,D3,D4	DIODE SCHOTTKY TMBS 10A 150V SMP	VISHAY V10PM15-M3/H
4	2	Q1,Q2	TRAN MOSFET N-CH 150V 56A 8LD TDSON EP	INFINEON TECHNOLOGIES BSC160N15NS5ATMA1
HARDWARE – FOR DEMO BOARD ONLY				
1	11	TP1,TP2,TP3,TP4,TP5,TP6 ,TP7,TP8,TP9,TP10,TP11	CONN-PCB SOLDER TERMINAL TURRETS	MILL-MAX 2501-2-00-80-00-00-07-0
2	4		STANDOFF, BRD SPT SNAP FIT 9.53MM LENGTH, EVAL BOARD MTG	KEYSTONE 8832

EVAL-LTC7067-AZ Schematic



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/23	Initial release	—