N-Channel Power MOSFET

FEATURES

- Super-Junction technology
- High performance good FOM
- High ruggedness performance
- High commutation performance
- 100% UIS & Rg tested
- RoHS Compliant
- Halogen-free

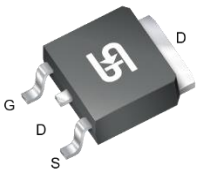
APPLICATIONS

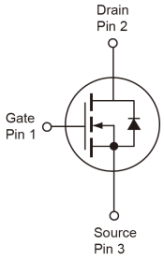
- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS		
PARAMETER	**VALUE**	**UNIT**
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on)}$ (max)	1.5	Ω
$Q_{g,typ}$	8	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

TO-252 (DPAK)





Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	600	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	3	A
	T_C = 100°C		2	A
Pulsed Drain Current (Note 2)		I_{DM}	9	A
Total Power Dissipation @ T_C = 25°C		P_D	55	W
Single Pulse Avalanche Energy (Note 3)		E_{AS}	100	mJ
Single Pulse Avalanche Current (Note 3)		I_{AS}	2	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Case Thermal Resistance	$R_{\Theta JC}$	2.2	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	52	°C/W

Thermal Performance Note: $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\Theta JA}$ is guaranteed by design while $R_{\Theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 4)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 1mA	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	$V_{GS(TH)}$	3.5	4.2	5.5	V
Gate Body Leakage	V_{GS} = ± 20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	100	μA
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 1A	$R_{DS(on)}$	--	1.3	1.5	Ω
Dynamic (Note 5)						
Total Gate Charge	V_{DS} = 300V, I_D = 3A, V_{GS} = 10V	Q_g	--	8.1	--	nC
Gate-Source Charge		Q_{gs}	--	2.5	--	
Gate-Drain Charge		Q_{gd}	--	3.4	--	
Input Capacitance	V_{DS} = 300V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	235	--	pF
Output Capacitance		C_{oss}	--	16	--	
Reverse Transfer Capacitance		C_{rss}	--	10	--	
Gate Resistance	f = 1.0MHz	R_g	0.84	2.8	5.6	Ω
Switching (Note 6)						
Turn-On Delay Time	V_{DD} = 300V, R_G = 10Ω, I_D = 1.5A, V_{GS} = 10V	$t_{d(on)}$	--	18	--	ns
Turn-On Rise Time		t_r	--	17	--	
Turn-Off Delay Time		$t_{d(off)}$	--	33	--	
Turn-Off Fall Time		t_f	--	40	--	
Source-Drain Diode (Note 4)						
Body-Diode Continuous Forward Current		I_S	--	--	3	A
Body-Diode Pulsed Current		I_{SM}	--	--	9	A
Forward Voltage	I_S = 3A, V_{GS} = 0V	V_{SD}	--	--	1.5	V
Reverse Recovery Time	V_{DD} = 300V, I_S = 3A, dI_F/dt = 100A/μs	t_{rr}	--	250	--	ns
Reverse Recovery Charge		Q_{rr}	--	1.9	--	μC

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. L = 50mH, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. Pulse test: PW ≤ 300μs, duty cycle ≤ 2%.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

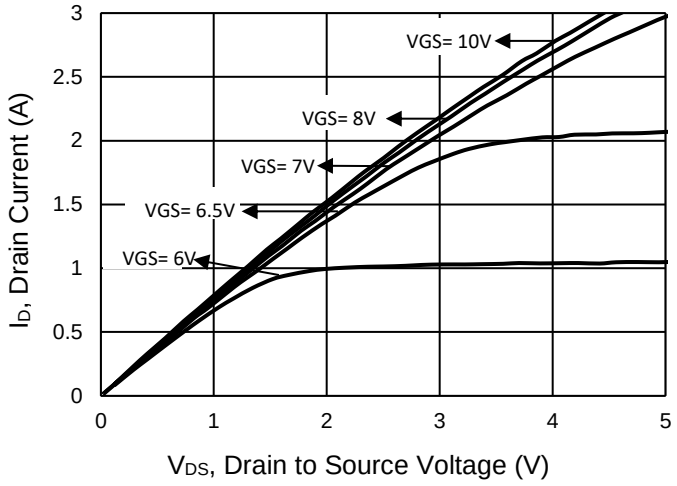
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM60NC1R5CP ROG	TO-252 (DPAK)	2500pcs / 13”Reel

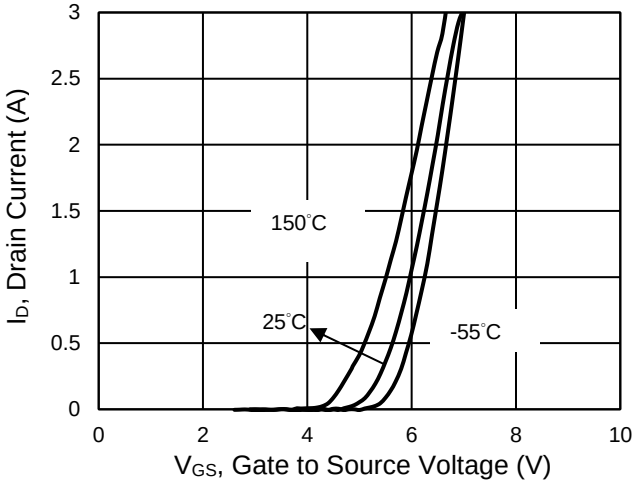
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

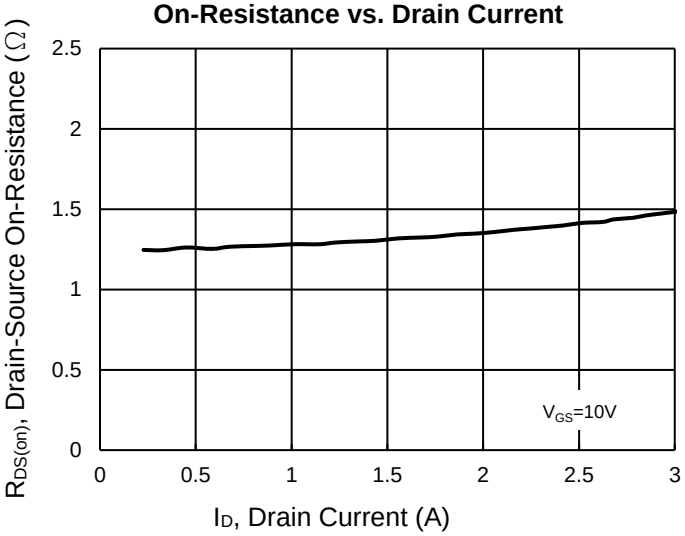
Output Characteristics



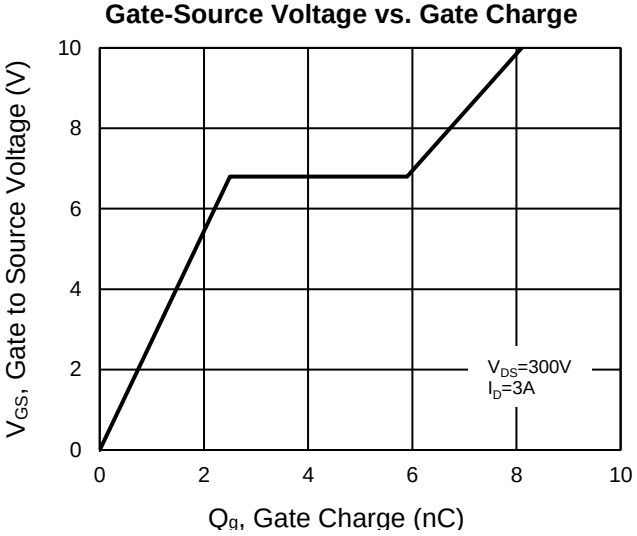
Transfer Characteristics



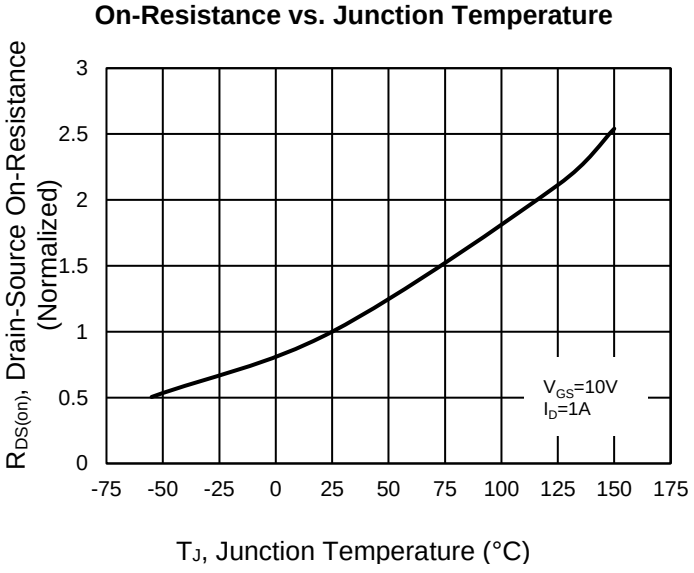
On-Resistance vs. Drain Current



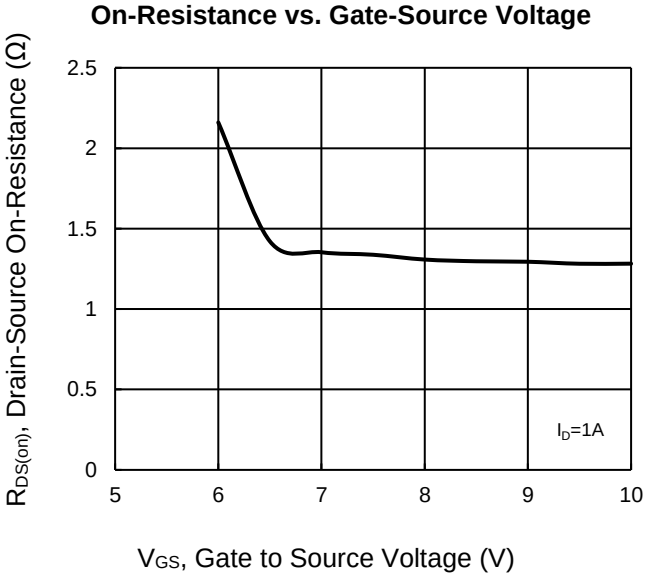
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



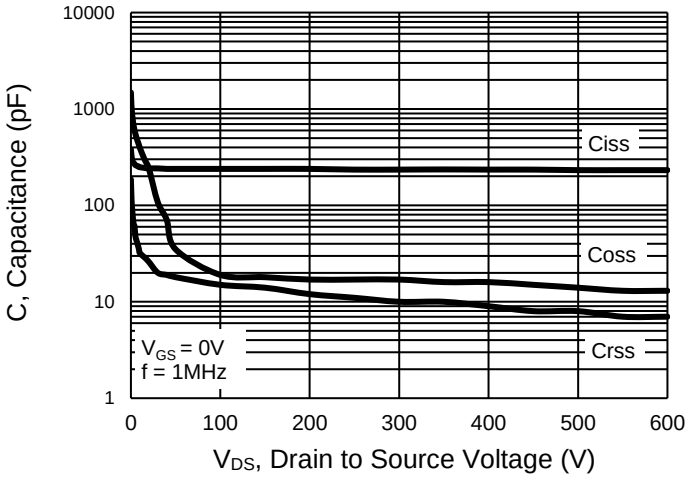
On-Resistance vs. Gate-Source Voltage



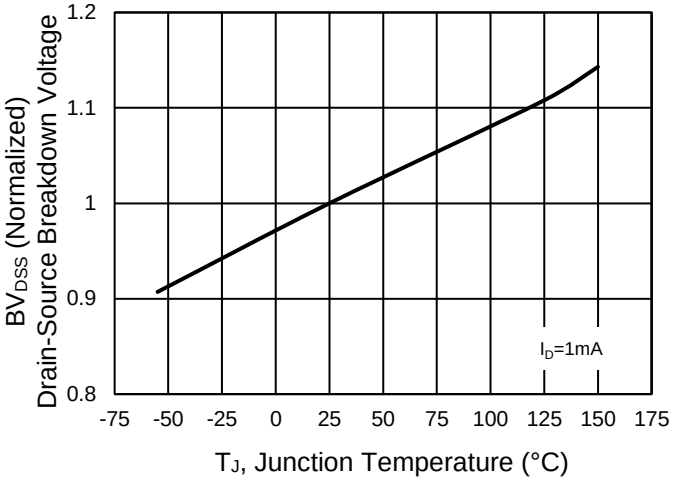
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

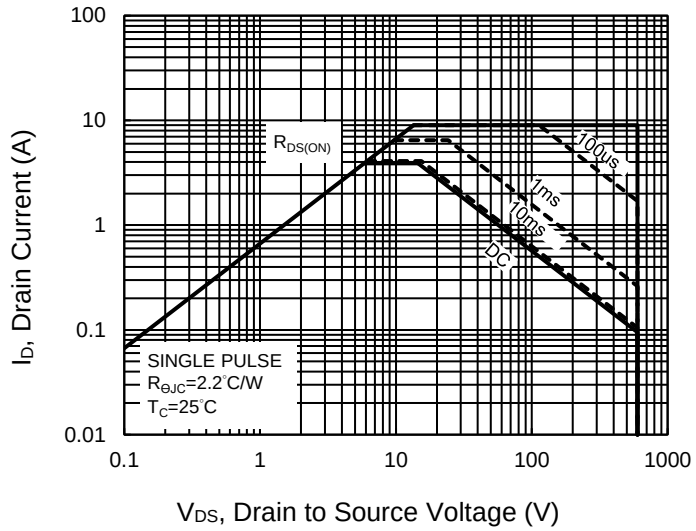
Capacitance vs. Drain-Source Voltage



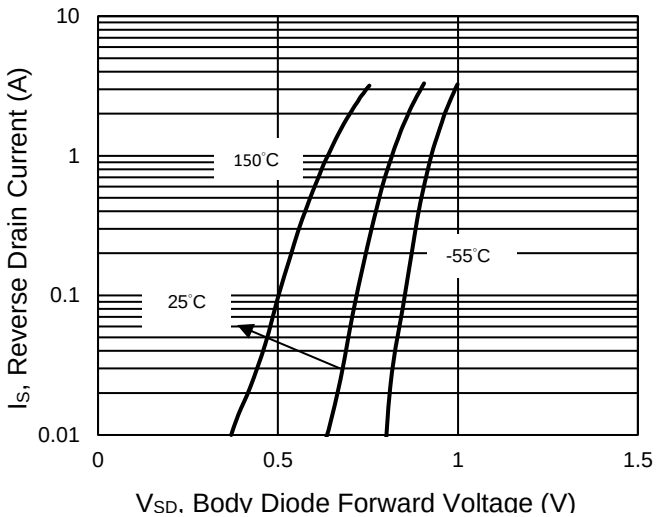
BV_{DSS} vs. Junction Temperature



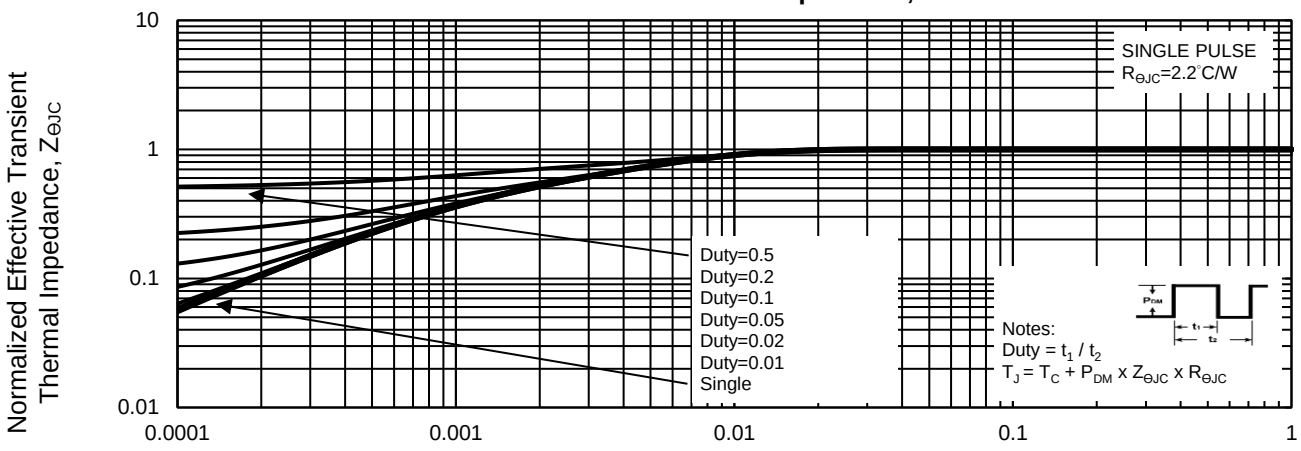
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

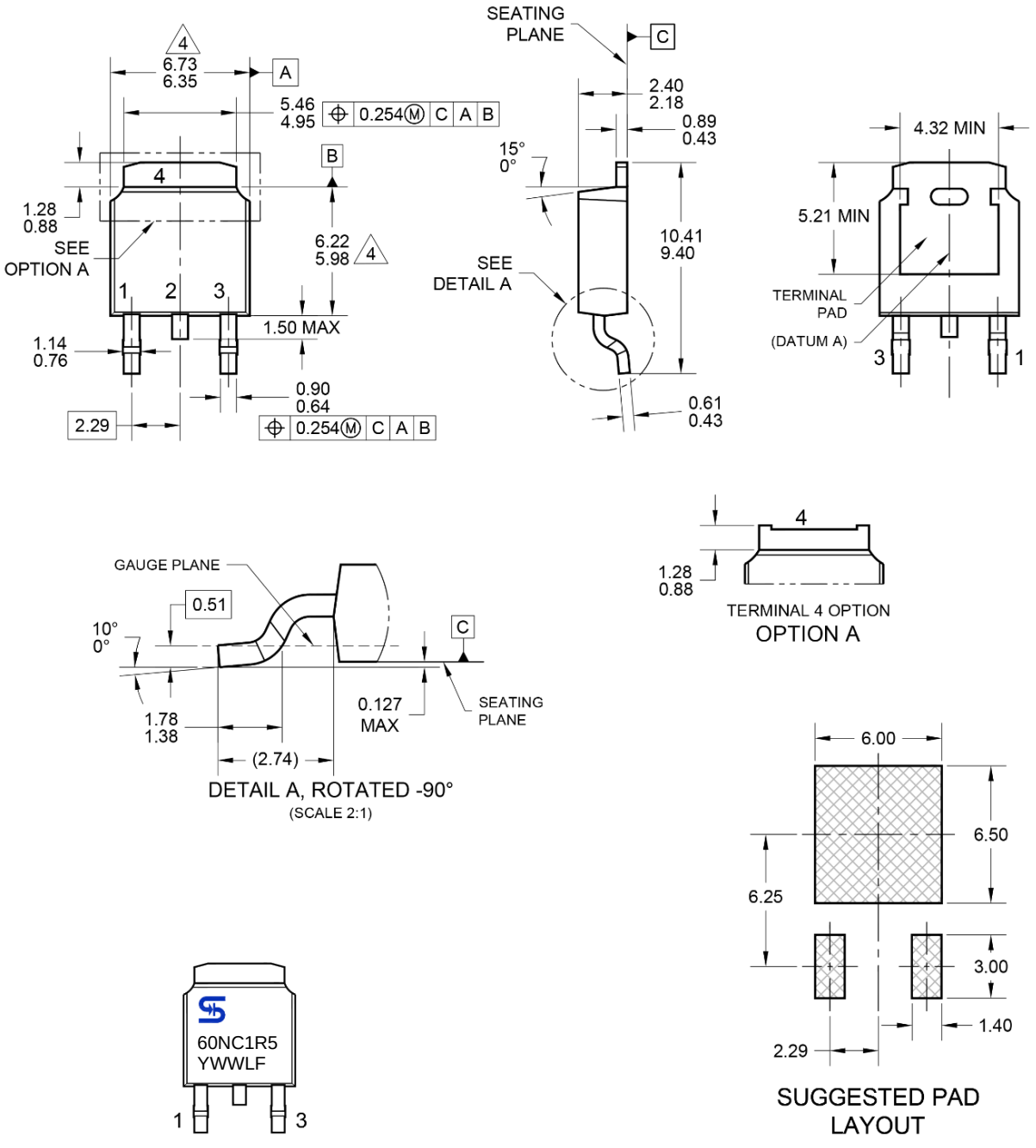


Normalized Thermal Transient Impedance, Junction-to-Case



PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-252



MARKING DIAGRAM

60NC1R5	= Device marking
Y	= Year Code
WW	= Week Code (01~52)
L	= Lot Code (1~9,A~Z)
F	= Factory Code

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC TO-252, VARIATION AA, ISSUE F.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
5. DWG NO. REF: HQ2SD07-TO252AA-013 REV B.

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