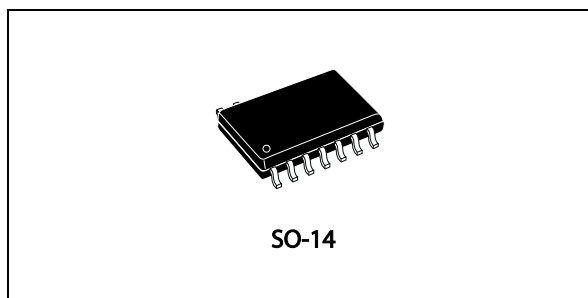


Advanced IGBT/MOSFET driver

Datasheet - production data



Features

- 1.5 A source/2.3 A sink (typ.) gate drive
- Active Miller clamp feature
- Two-level turn-off with adjustable level and delay
- Desaturation detection
- Fault status output
- Negative gate drive capability
- Input compatible with pulse transformer or optocoupler
- Separate sink and source outputs for easy gate driving
- UVLO protection
- 2 kV ESD protection (HBM)

Applications

- 1200 V, 3-phase inverters
- Motor control
- UPS systems

Description

The TD350E device is an advanced gate driver for IGBTs and power MOSFETs. Control and protection functions are included and allow the design of high reliability systems.

The innovative active Miller clamp function eliminates the need for negative gate drive in most applications and allows the use of a simple bootstrap supply for the high side driver.

The device includes a two-level turn-off feature with adjustable level and delay. This function protects against excessive overvoltage at turn-off in case of overcurrent or short-circuit conditions. The same delay set in the two-level turn-off feature is applied at turn-on to prevent pulse width distortion.

The device also includes IGBT desaturation protection and a FAULT status output, and is compatible with both pulse transformer and optocoupler signals.

Table 1. Device summary

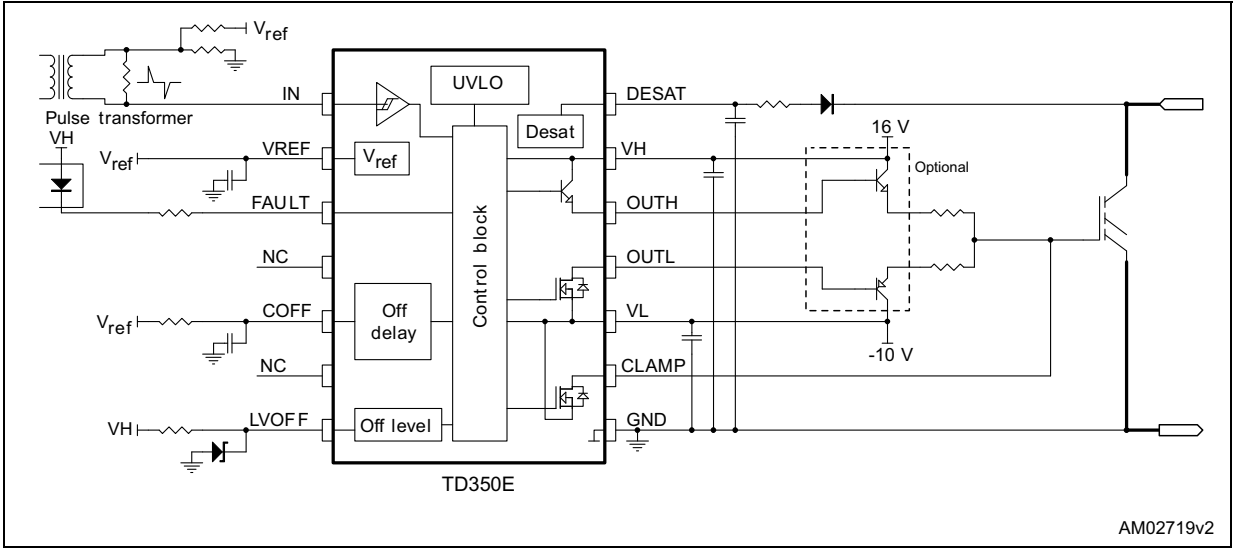
Order code	Temperature range	Package	Packaging
TD350E	-40, +125 °C	SO-14	Tube
TD350ETR			Tape and reel

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1 Block diagram

Figure 1. Functional block diagram



AM02719v2

2 Pin connections

Figure 2. Pin connections (top view)

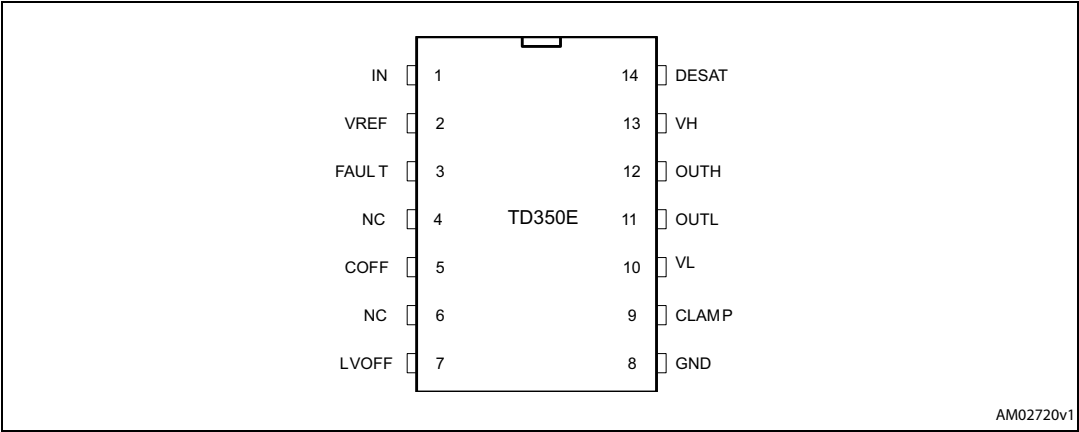


Table 2. Pin description

Name	Pin number	Type	Function
IN	1	Analog input	Input
VREF	2	Analog output	+5 V reference voltage
FAULT	3	Digital output	Fault status output
NC	4	Not connected	
COFF	5	Timing capacitor	Turn-off delay
NC	6	Not connected	
LVOFF	7	Analog input	Turn-off level
GND	8	Power supply	Signal ground
CLAMP	9	Analog output	Miller clamp
VL	10	Power supply	Negative supply
OUTL	11	Analog output	Gate drive output (sink)
OUTH	12	Analog output	Gate drive output (source)
VH	13	Power supply	Positive supply
DESAT	14	Analog input	Desaturation protection

3 Absolute maximum ratings

Table 3. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{HL}	Maximum supply voltage (V _H - V _L)	28	V
V _H	Maximum V _H voltage vs. GND	28	V
V _L	Minimum V _L voltage vs. GND	-12	V
V _{out}	Voltage on OUTH, OUTL, CLAMP pins	V _L - 0.3 to V _H + 0.3	V
V _{des}	Voltage on DESAT, FAULT, LVOFF pin	-0.3 to V _H + 0.3	V
V _{other}	Voltage on other pins (IN, COFF, VREF)	-0.3 to 7	V
P _d	Power dissipation	500	mW
T _{stg}	Storage temperature	-55 to 150	°C
T _j	Maximum junction temperature	150	°C
R _{thja}	Thermal resistance junction-ambient	125	°C/W
R _{thjc}	Thermal resistance junction-case	22	°C/W
ESD	Electrostatic discharge (HBM)	2	kV

Table 4. Operating conditions

Symbol	Parameter	Value	Unit
V _H	Positive supply voltage vs. GND	UVLO to 26	V
V _L	Negative supply voltage vs. GND	0 to -10	V
V _{H-VL}	Maximum total supply voltage	26	V
T _{oper}	Operating free air temperature range	-40 to 125	°C

4 Electrical characteristics

$T_A = -20$ to $125\text{ }^{\circ}\text{C}$, $V_H = 16\text{ V}$, $V_L = -10\text{ V}$ (unless otherwise specified).

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input						
V_{ton}	IN turn-on threshold voltage		0.8	1.0		V
V_{toff}	IN turn-off threshold voltage			4.0	4.2	V
t_{onmin}	Minimum pulse width		100	135	220	ns
I_{inp}	IN input current				1	μA
Voltage reference⁽¹⁾						
V_{ref}	Voltage reference	$T = 25\text{ }^{\circ}\text{C}$ $T_{min} < T < T_{max}$	4.85 4.77	5.00	5.15 5.22	V V
I_{ref}	Maximum output current		10			mA
Desaturation protection						
V_{des}	Desaturation threshold		6.5	7.2	7.9	V
I_{des}	Source current			250		μA
Fault output						
t_{fault}	Delay for fault detection				500	ns
V_{FL}	FAULT low voltage	$I_{FLsink} = 10\text{ mA}$			1	V
Clamp						
V_{tclamp}	CLAMP pin voltage threshold			2.0		V
V_{CL}	Clamp low voltage	$T = 25\text{ }^{\circ}\text{C}$; $I_{CLsink} = 500\text{ mA}$ $T_{min} < T < T_{max}$; $I_{CLsink} = 500\text{ mA}$			VL + 2.5 VL + 3.0	V V
Off delay						
V_{tdel}	Voltage threshold		2.35	2.50	2.65	V
R_{del}	Discharge resistor	$I = 1\text{ mA}$			500	Ω
Off levels						
I_{blvoff}	LVOFF peak input current (sink)	LVOFF = 12 V		120	200	μA
V_{iolv}	Offset voltage	LVOFF = 12 V	-0.3	-0.15	0	V
Outputs						
V_{OL1}	Output low voltage	$I_{osink} = 20\text{ mA}$			VL + 0.35	V
V_{OL2}	Output low voltage	$T = 25\text{ }^{\circ}\text{C}$; $I_{osink} = 200\text{ mA}$ $T_{min} < T < T_{max}$; $I_{osink} = 200\text{ mA}$			VL + 1.0 VL + 1.5	V V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL3}	Output low voltage	$T = 25\text{ }^{\circ}\text{C}$, $I_{\text{osink}} = 500\text{ mA}$ $T_{\text{min}} < T < T_{\text{max}}$, $I_{\text{osink}} = 500\text{ mA}$			$V_L + 2.5$ $V_L + 3.0$	V V
V_{OH1}	Output high voltage 1	$I_{\text{osource}} = 20\text{ mA}$	$V_H - 2.5$			V
V_{OH2}	Output high voltage 2	$I_{\text{osource}} = 200\text{ mA}$	$V_H - 3.0$			V
V_{OH3}	Output high voltage 3	$I_{\text{osource}} = 500\text{ mA}$	$V_H - 4.0$			V
t_r	Rise time	$C_L = 1\text{ nF}$, 10% to 90% $V_L = 0$ $V_L = -10\text{ V}$			130 175	ns ns
t_f	Fall time ⁽²⁾	$C_L = 1\text{ nF}$, 90% to 10% $V_L = 0$ $V_L = -10\text{ V}$			75 90	ns ns
$t_{\text{pd_on}}$	Turn-on propagation delay	10% output change; $T = 25\text{ }^{\circ}\text{C}$	400	500	600	ns
		10% output change; $T_{\text{min}} < T < T_{\text{max}}$	350		650	ns
$t_{\text{pd_off}}$	Turn-off propagation delay	10% output change; $T = 25\text{ }^{\circ}\text{C}$	350	450	570	ns
		10% output change; $T_{\text{min}} < T < T_{\text{max}}$	300		620	ns
ΔT_w	Input to output pulse distortion	10% output change	25	50	120	ns
Undervoltage lockout (UVLO)						
UVLOH	UVLO top threshold		10	11	12	V
UVLOL	UVLO bottom threshold		9	10	11	V
V_{hyst}	UVLO hysteresis	UVLOH - UVLOL	0.5	1		V
Supply current						
I_{in}	Quiescent current	Output = 0 V, no load			5	mA

1. Recommended capacitor range on VREF pin is 10 nF to 100 nF.

2. 2-step turn-off disabled.

5 Functional description

5.1 Input

The input is compatible with optocouplers or pulse transformers. The input is triggered by the signal edge and allows the use of a small-sized, low cost pulse transformer. Input is active low (output is high when input is low) to ease the use of the optocoupler. When driven by a pulse transformer, the input pulse (positive and negative) width must be larger than the minimum pulse width t_{onmin} .

5.2 Voltage reference

A voltage reference is used to create accurate timing for the two-level turn-off with external resistor and capacitor.

5.3 Desaturation protection

Desaturation protection ensures the protection of the IGBT in the event of overcurrent. When the DESAT voltage goes higher than 7 V, the output is driven low (with 2-level turn-off, if applicable). The FAULT output is activated. The FAULT state is exited at the next falling edge of IN input.

A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by an internal current source and external capacitor.

DESAT input can also be used with an external comparator for overcurrent or overtemperature detection.

5.4 Active Miller clamp

A Miller clamp allows the control of the Miller current during a high dV/dt situation and can eliminate the need for a negative supply voltage.

During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2 V (relative to GND). The clamp voltage is $V_L + 3$ V max. for a Miller current up to 500 mA. The clamp is disabled when the IN input is triggered again.

5.5 Two-level turn-off

The two-level turn-off is used to increase the reliability of the application.

During turn-off, gate voltage can be reduced to a programmable level in order to reduce the IGBT current (in the event of overcurrent). This action prevents both dangerous overvoltage across the IGBT and RBSOA problems, especially at short-circuit turn-off.

The two-level turn-off (T_a) delay is programmable through an external resistor and capacitor for accurate timing (refer to [Equation 1](#)).

Turn-off delay (T_a) is also used to delay the input signal to prevent distortion of input pulse width.

Equation 1

$$T_a [\mu s] \cong 0.7 \cdot R_{off} [k\Omega] \cdot C_{off} [nF]$$

5.6 Minimum ON time

In order to ensure the proper operation of the 2-level turn-off function, the input ON time (T_{win}) must be greater than the T_{winmin} value:

Equation 2

$$T_{winmin} = T_a + 2 \cdot R_{del} \cdot C_{off}$$

R_{del} is the internal discharge resistor and C_{off} is the external timing capacitor.

Input signals smaller than T_a are ignored. Input signals larger than T_{winmin} are transmitted to the output stage after the T_a delay with minimum width distortion ($\Delta T_w = T_{wout} - T_{win}$).

For an input signal width T_{win} between T_a and T_{winmin} , the output width T_{wout} is reduced below T_{win} (pulse distortion) and the IGBT could be partially turned on. These input signals should be avoided during normal operation.

5.7 Output

The output stage is able to sink 2.3 A and source 1.5 A (typ.) at 25 °C (1.2 A/0.75 A minimum over the full temperature range). Separate sink and source outputs allow independent gate charge and discharge control without an extra external diode.

5.8 Fault status output

Fault output is used to signal a fault event (desaturation, UVLO) to a controller. The fault pin is designed to drive an optocoupler.

5.9 Undervoltage protection

Undervoltage detection protects the application in the event of a low V_H supply voltage (during startup or a fault situation). During undervoltage, the OUTH pin is open and the OUTL pin is driven low (active pull-down for $V_H > 2$ V, passive pull-down for $V_H < 2$ V). Fault output signals the undervoltage state and is reset only when undervoltage state disappears.

Figure 3. Undervoltage protection

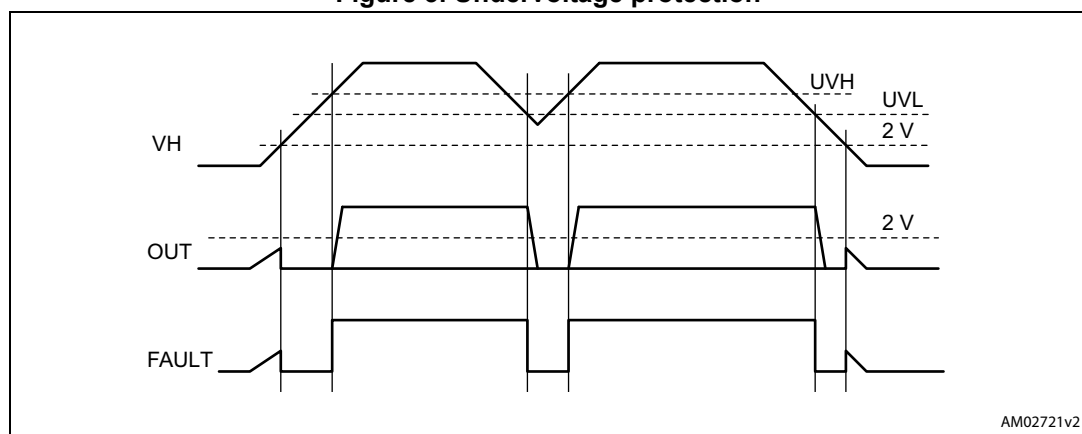
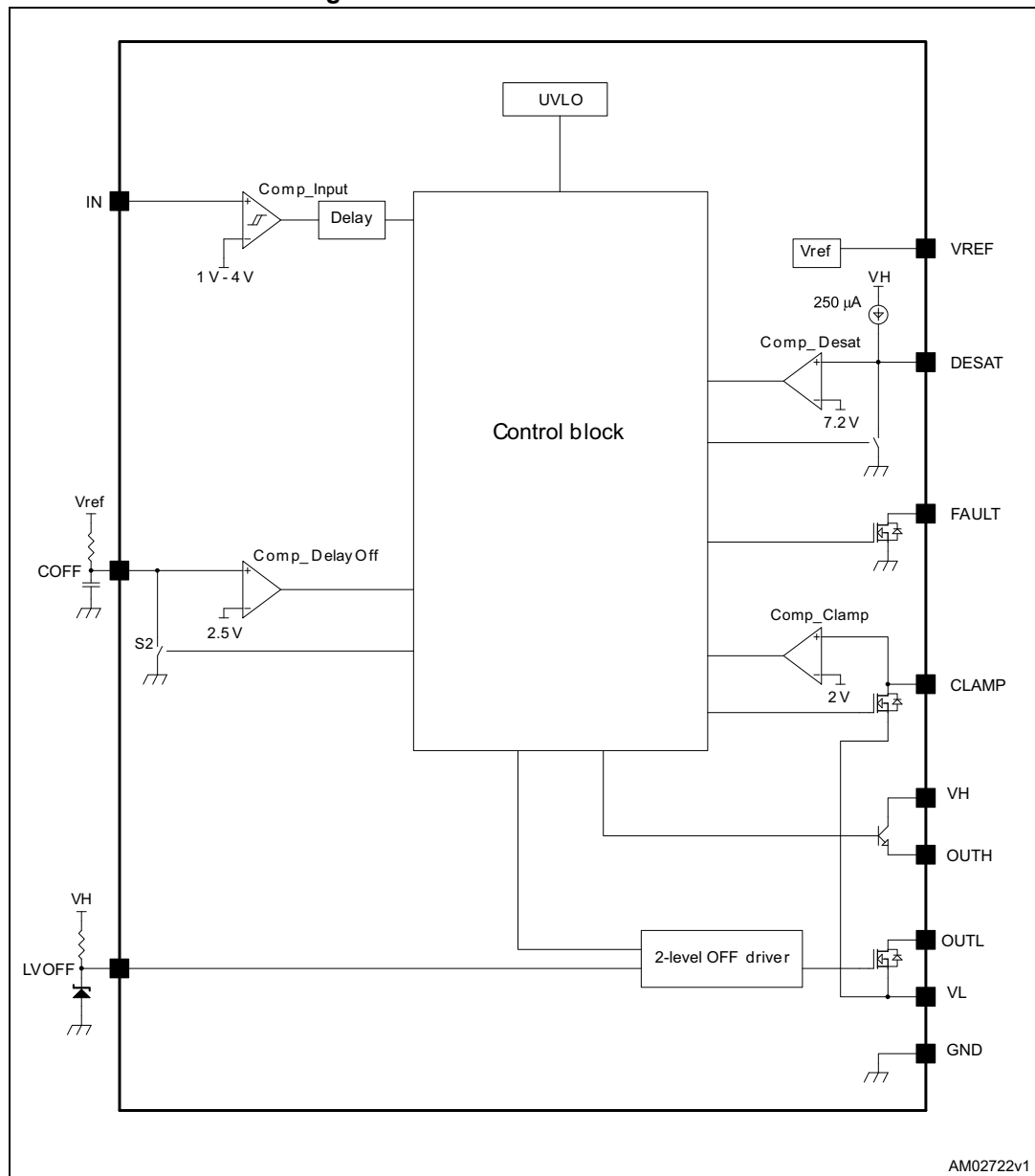


Figure 4. Detailed internal schematic



6 Timing diagrams

Figure 5. Turn-on and turn-off

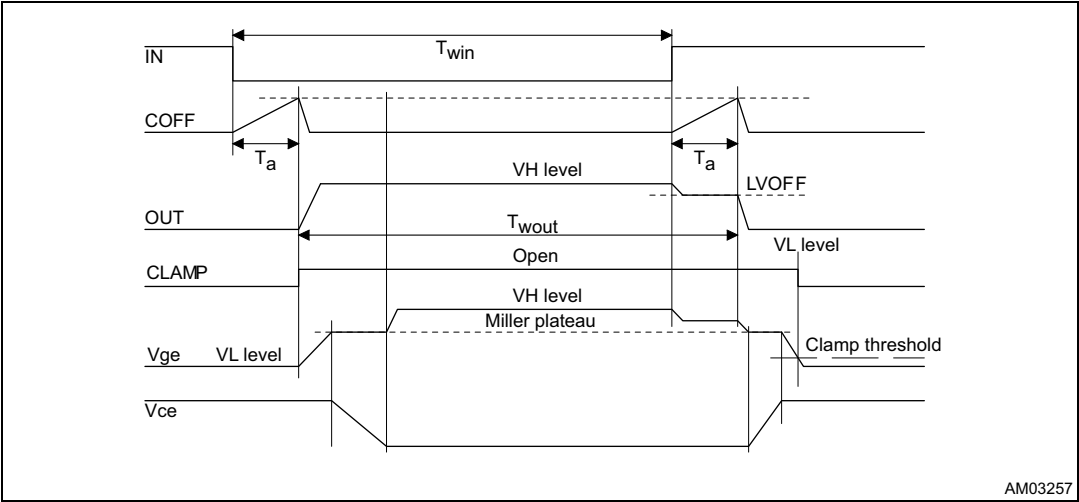


Figure 6. Minimum ON time

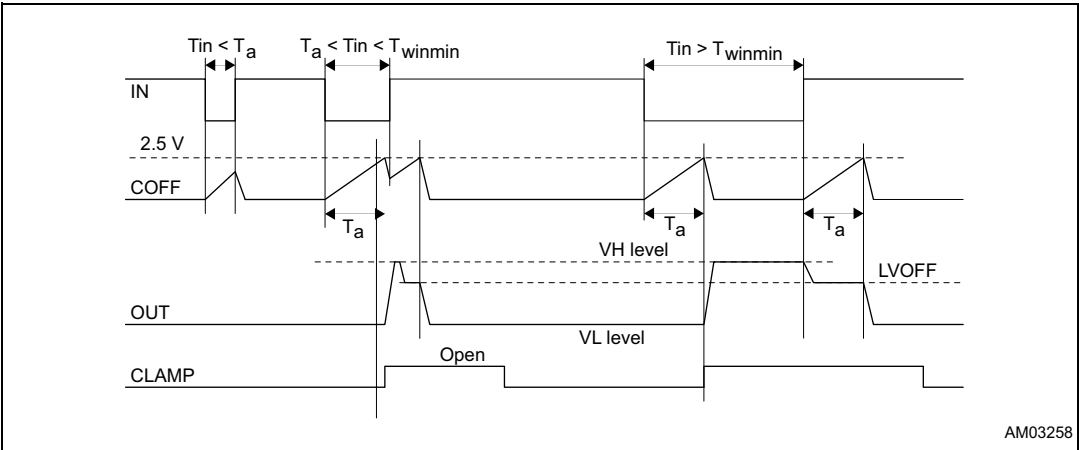
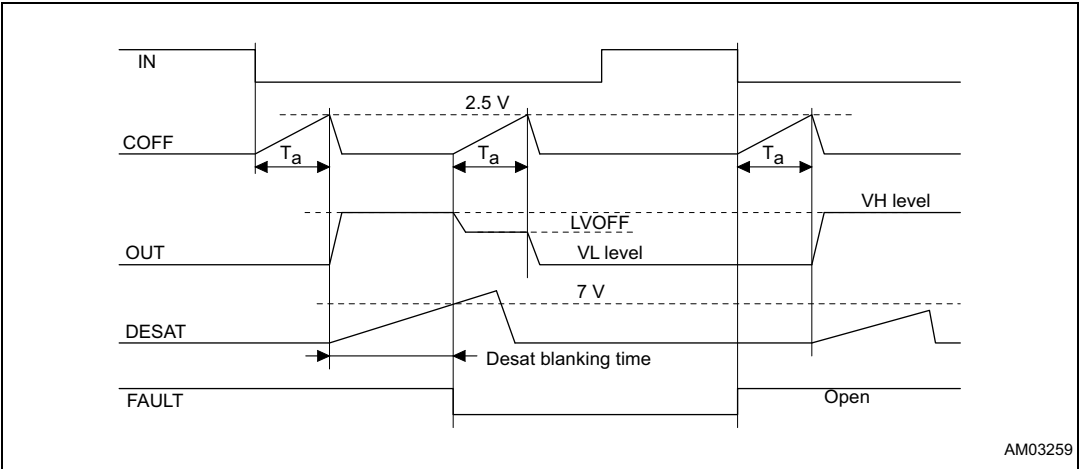


Figure 7. Desaturation fault



7 Typical performance curves

Figure 8. Supply current vs. temperature

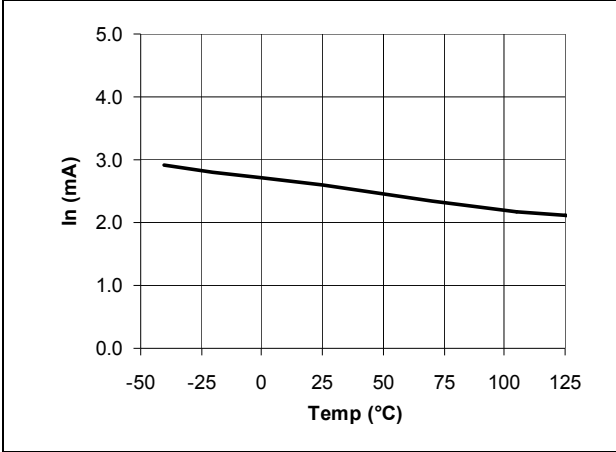


Figure 9. Low level output voltage vs. temp.

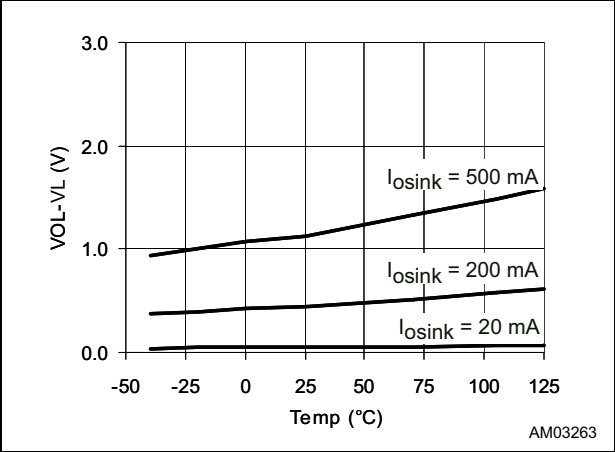


Figure 10. Desaturation threshold vs. temp.

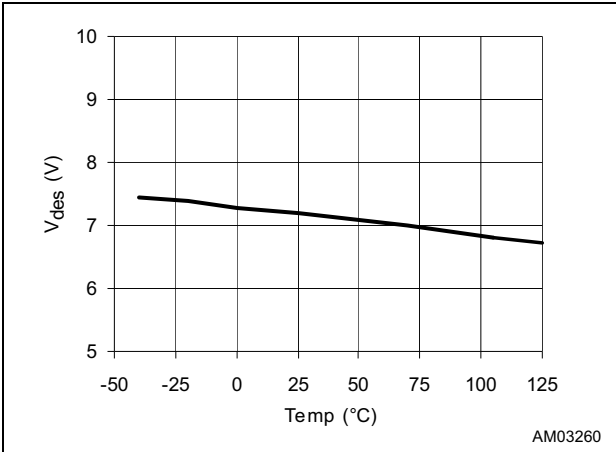


Figure 11. Voltage reference vs. temperature

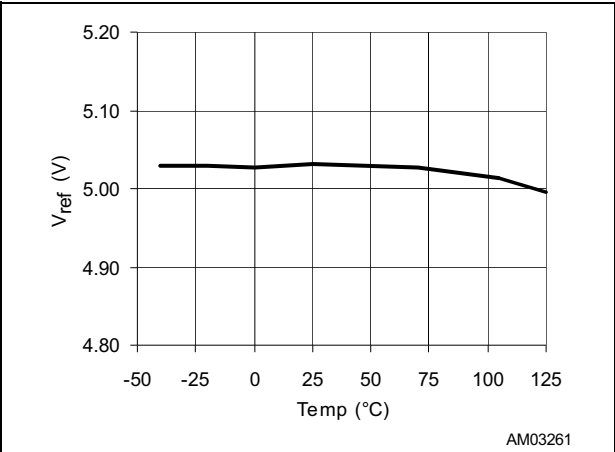


Figure 12. High level output voltage vs. temperature

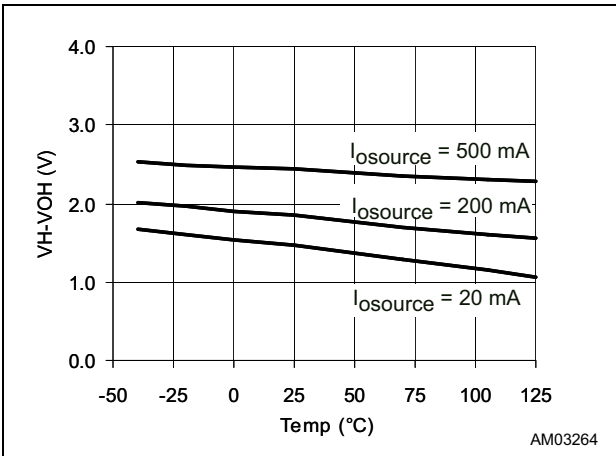
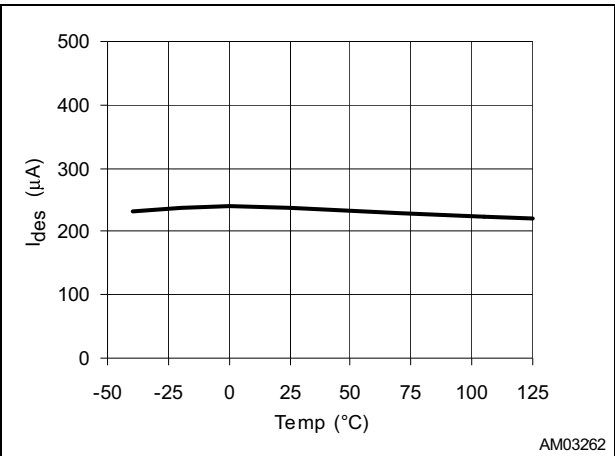


Figure 13. Desaturation source current vs. temperature



8 Application diagrams

Figure 14. Single supply IGBT drive with active Miller clamp and 2-level turn-off

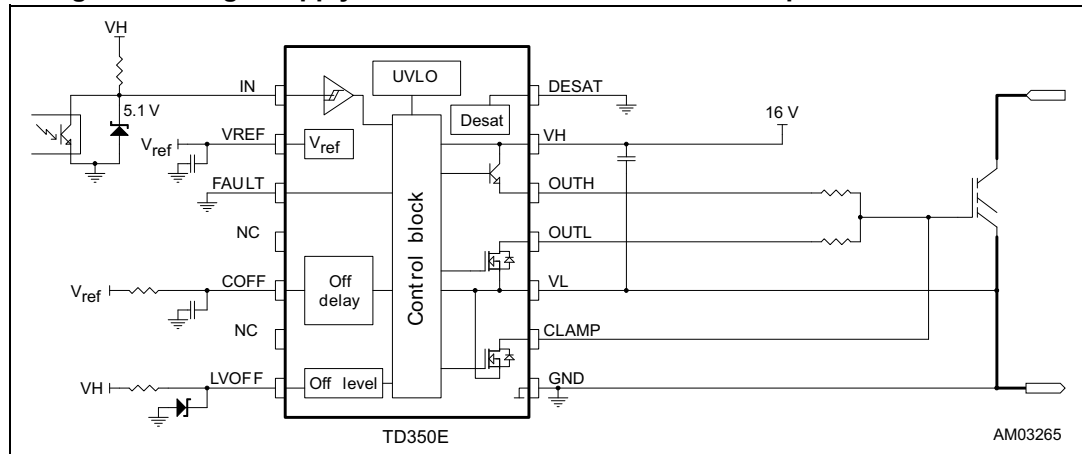


Figure 15. Large IGBT drive with negative gate drive and desaturation detection

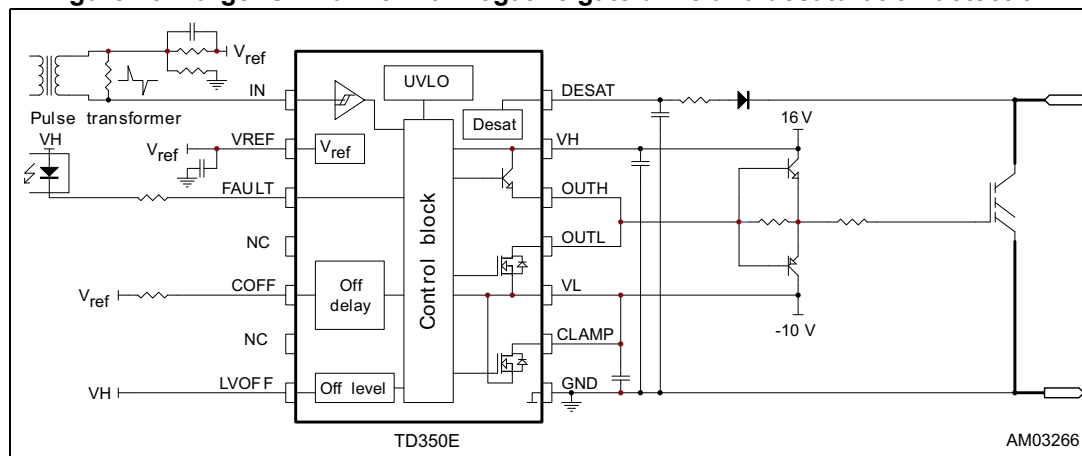
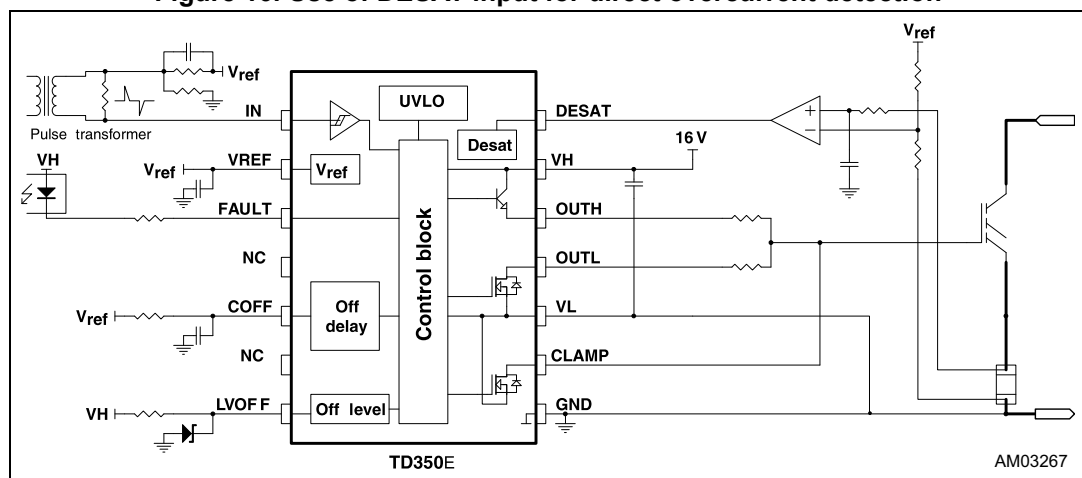


Figure 16. Use of DESAT input for direct overcurrent detection



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 17. Package SO-14 package outline

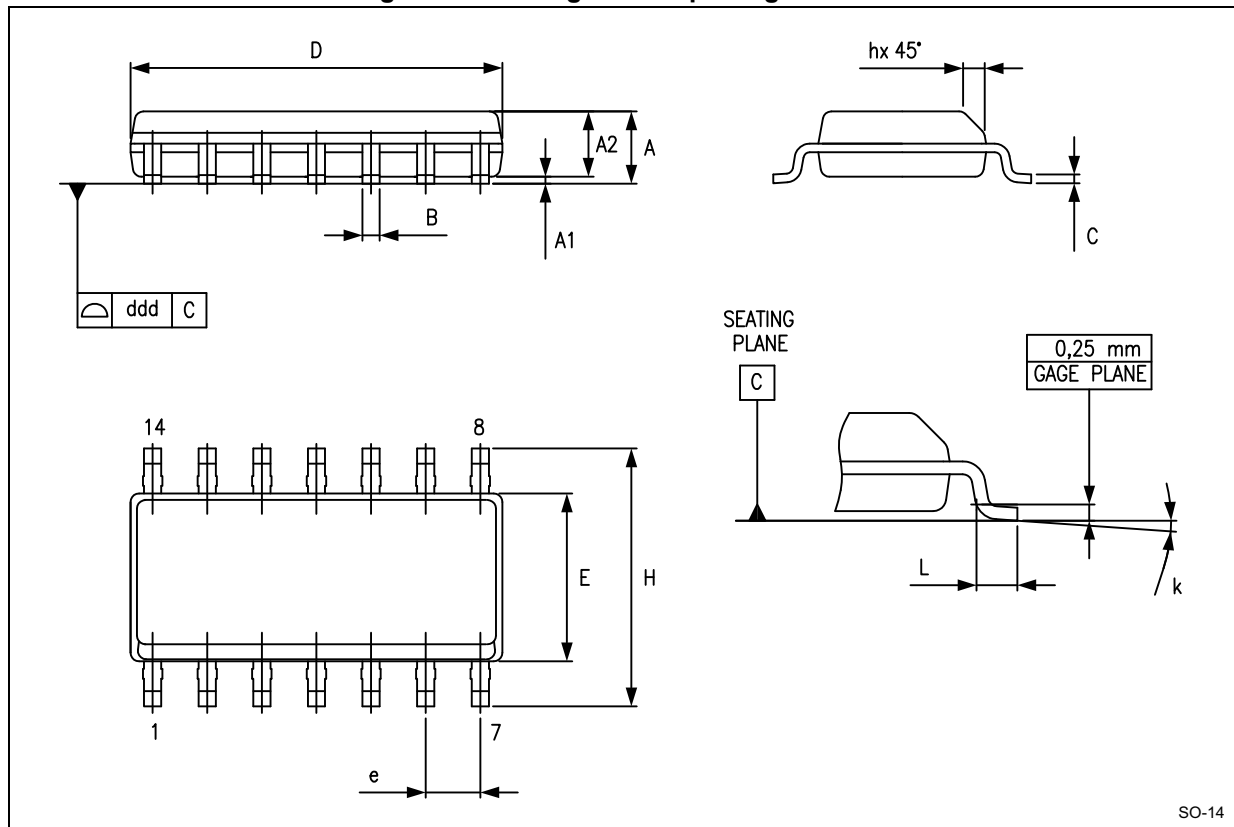


Table 6. SO-14 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	1.35		1.75
A1	0.10		0.25
A2	1.10		1.65
B	0.33		0.51
C	0.19		0.25
D	8.55		8.75
E	3.80		4.00
e		1.27	
H	5.80		6.20
h	0.25		0.50
L	0.40		1.27
k	0		8
ddd			0.10

10 Revision history

Table 7. Document revision history

Date	Revision	Changes
08-Mar-2011	1	First release.
21-Sep-2011	2	– Updated Table 1 – Minor text changes throughout the document
13-Jun-2013	3	Updated Figure 1, Figure 4 to Figure 7, Figure 9 to Figure 16 (minor corrections). Updated Figure 3 (replaced “VCCmin” by “2 V”). Updated Table 5 (moved “I_{osink}” for “V_{OL1/2/3}” symbols to “Test condition”). Updated Section 5.5 (replaced “Turn-off” by “The two-level turn-off”, added Equation 1). Updated Section 5.6 (added heading for Equation 2). Updated Table 6 (updated data, reversed order of Figure 17 and Table 6). Minor corrections throughout document.

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