AF Control LSI

LC898229XI

WLCSP
6 BUMP
CASE 567UK

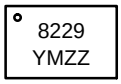
Overview

This LSI is Closed−Auto Focus control LSI equipped with hall sensor. It consists of 1 system of feedback circuit and constant current driver. It has also a built−in EEPROM and temperature sensor.

Features

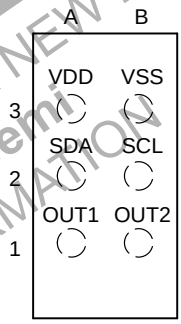
- Built−in Equalizer Circuit Using Digital Operation
  - AF Control Equalizer Circuit
  - Any Coefficient can be Specified by 2−wire Serial I/F (TWIF)
- 2−wire Serial Interface (The communication protocol is compatible with I^2C)
- Built−in A/D Converter
- Built−in D/A Converter
  - Hall Offset
  - Constant Current Bias
- Built−in Hall Sensor
  - Si Hall Sensor
- Built−in EEPROM
  - 64byte (16byte/page)
- Built−in OSC
- Built−in Constant Current Driver
  - 110 mA
- Package
  - WL−CSP 6−pin (2 x 3pin) , Thickness Max 0.29 mm, with Backside Coat
  - Lead−free, Halogen−free
- Supply voltage
  - V_{DD} (2.6 V to 3.3 V)

DEVICE MARKING INFORMATION



8229= Specific Device Code
Y = Year
M = Month
ZZ = Assembly Lot

PIN LAYOUT



(Top View)

Circuit Name	Number of PINs
Driver	2
Power	2
Logic	2

ORDERING INFORMATION

Device	Package	Shipping†
LC898229XI	WLCSP6	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Pin Description

Type	
I	Input
O	Output
B	Bidirection
P	Power supply, GND
NC	Not Connected

2−wire Serial Interface		
SCL	I	2−wire serial interface clock pin
SDA	B	2−wire serial interface data pin

Driver Interface		
OUT1	O	Driver output (to Actuator)
OUT2	O	Driver output (to Actuator)

Power Supply Pin		
V_{DD}	P	Power supply
V_{SS}	P	GND

***Process when Pins are Not Used**

PIN TYPE “O” – Ensure that it is set to OPEN.

PIN TYPE “I” – OPEN is inhibited. Ensure that it is connected to the VDD or VSS even when it is unused.

(Please contact **onsemi** for more information about selection of VDD or VSS.)

PIN TYPE “B” – If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

Table 1. ABSOLUTE MAXIMUM RATING (VSS = 0 V)

Item	Symbol	Condition	Rating	Unit
Supply voltage	$V_{DD}33$ max	Ta ≤ 25°C	−0.3〜4.6	V
Input/output voltage	V_I33, V_O33	Ta ≤ 25°C	−0.3〜$V_{DD}33$+0.3	V
Storage ambient temperature	Tstg		−55〜125	°C
Operating ambient temperature	Topr		−30〜70	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. ACCEPTABLE OPERATION RANGE at Ta = −30 ~ 70°C, VSS = 0 V

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{DD}33$	2.6	2.8	3.3	V
Input voltage range	V_{IN}	0		$V_{DD}33$	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. DC CHARACTERISTICS: Input/output level at VSS = 0 V, VDD = 2.6 V ~ 3.3V, Ta = −30 ~ 70°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pins
High−level input voltage	V_{IH}	CMOS compliant Schmidt	1.4			V	SCL, SDA
Low−level input voltage	V_{IL}				0.4	V	
Low−level output voltage	V_{OL}	IOL = 2 mA			0.2	V	SDA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 4. DRIVER OUTPUT (OUT1, OUT2) at VSS = 0 V, VDD = 2.8 V, Ta = 25°C

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Pins
Maximum current	I_{full}		105	110	115	mA	OUT1, OUT2

Table 5. NON−VOLATILE MEMORY CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Applicable Circuit
Endurance	EN				1000	Cycles	EEPROM
Data retention	RT		10			Years	
Write time	t_{WT}				20	ms	

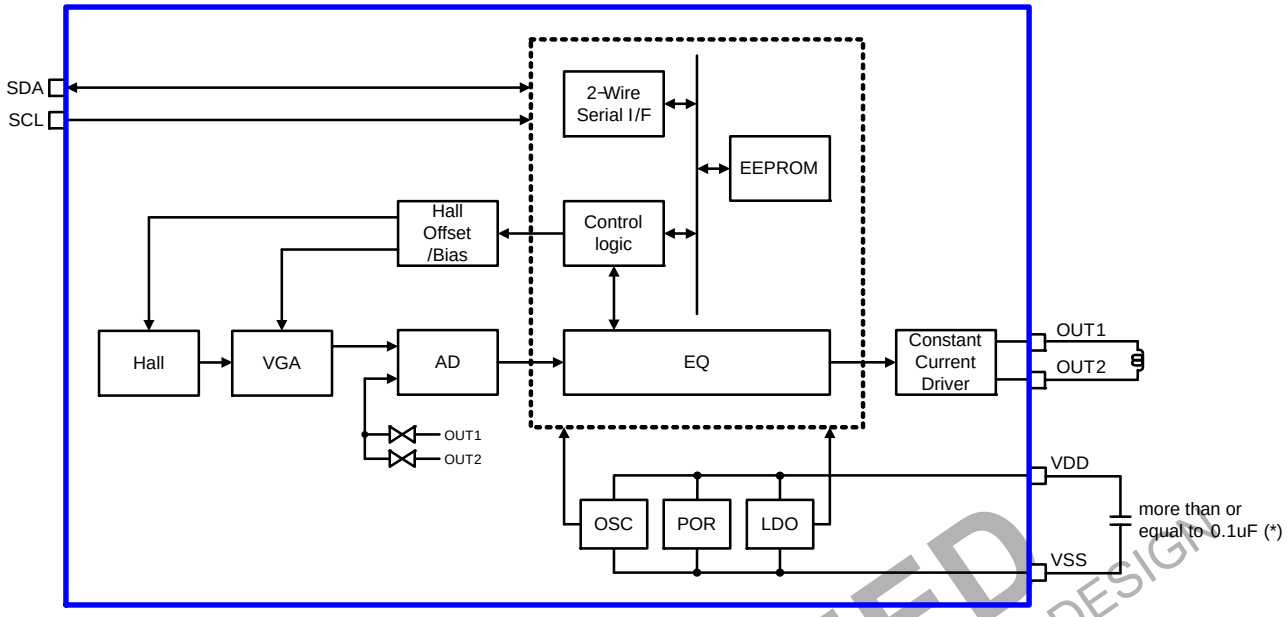


Figure 1. Block Diagram

NOTE: Consider capacitance of capacitor between V_{DD} and V_{SS}. According to power source environment, attach an additional capacitor in camera module.

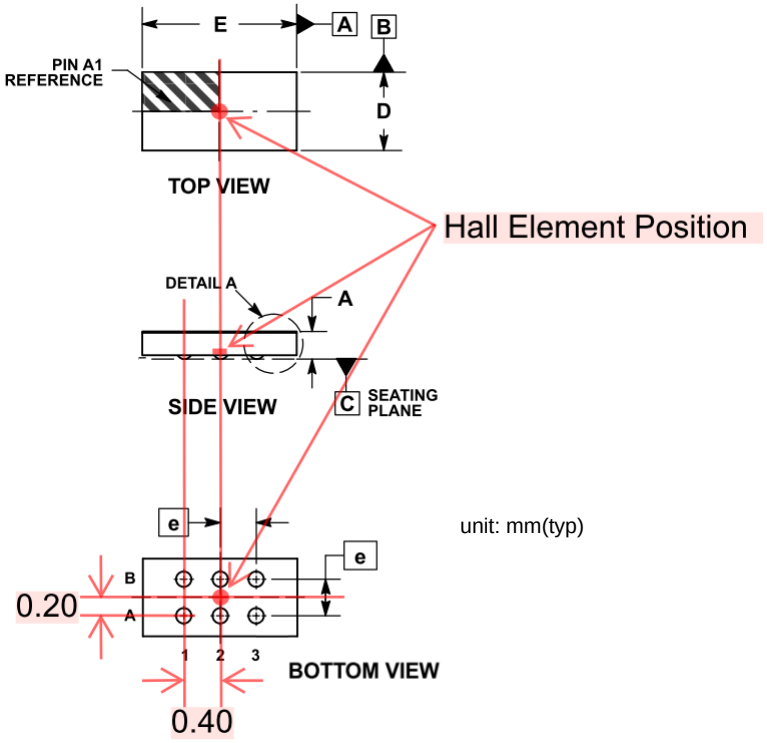


Figure 2. Hall Element Position

NOTE: Please refer to package diagram for each dimension.

AC Characteristics

VDD Supply Timing

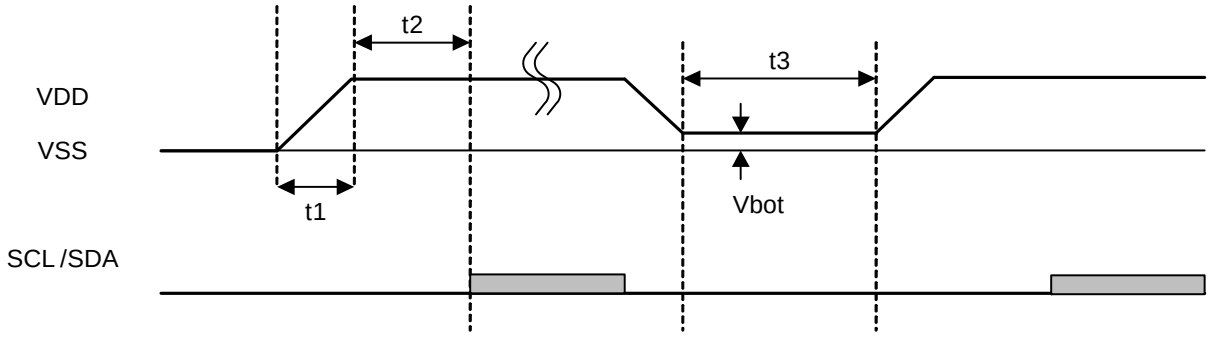


Figure 3. VDD Supply Timing

It is available to use 2−wire serial interface 5ms later for Power On Reset of VDD.

Item	Symbol	Min	Typ	Max	Unit
V_{DD} turn on time	t1			3	ms
2−wire serial interface start time from VDD on	t2	5			ms
V_{DD} off time	t3	100			ms
Bottom Voltage	Vbot			0.1	V

AC Specification

Figure 4 shows interface timing definition and Table 6 shows electric characteristics.

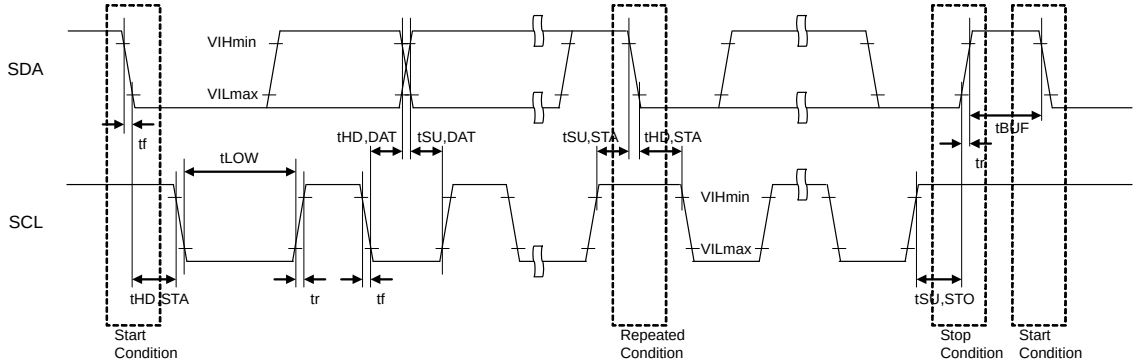


Figure 4. 2−wire Serial Interface Timing Definition

Table 6. ELECTRIC CHARACTERISTICS for 2−wire Serial Interface (AC Characteristics)

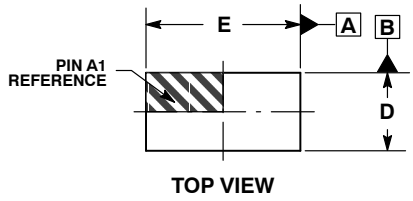
Item	Symbol	Pin Name	Fast−mode			Fast−mode Plus			Units
			Min	Typ	Max	Min	Typ	Max	
SCL clock frequency	FSCL	SCL			400			1000	KHz
START condition hold time	t_{HD}, STA	SCL, SDA	0.6			0.26			µs
SCL clock Low period	t_{LOW}	SCL	1.3			0.5			µs
SCL clock High period	t_{HIGH}	SCL	0.6			0.26			µs
Setup time for repetition START condition	t_{SU}, STA	SCL, SDA	0.6			0.26			µs
Data hold time	t_{HD}, DAT	SCL, SDA	0 (Note 1)		0.9	0 (Note 1)			µs
Data setup time	t_{SU}, DAT	SCL, SDA	100			50			ns
SDA, SCL rising time	t_r	SCL, SDA			300			120	ns
SDA, SCL falling time	t_f	SCL, SDA			300			120	ns
STOP condition setup time	t_{SU}, STO	SCL, SDA	0.6			0.26			µs
Bus free time between STOP and START	t_{BUF}	SCL, SDA	1.3			0.5			µs

1. This LSI is designed for a condition with typ. 20 ns of hold time. If SDA signal is unstable around falling point of SCL signal, please implement an appropriate treatment on board, such as inserting a resistor.

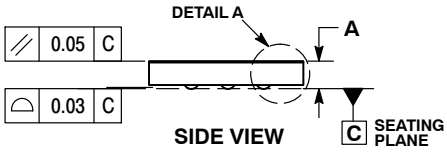
SCALE 4:1

WLCSP6 0.86x1.70x0.265
CASE 567UK
ISSUE A

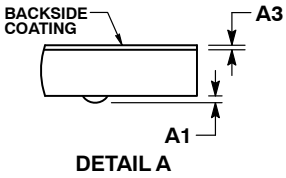
DATE 22 MAY 2017



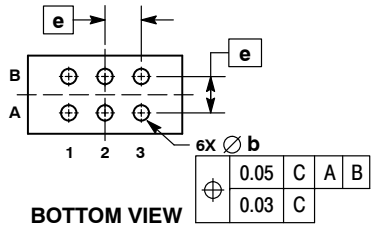
TOP VIEW



SIDE VIEW

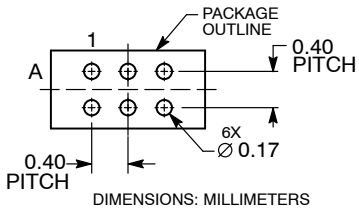


DETAIL A



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*



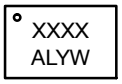
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF CONTACT BALLS.
4. COPLANARITY APPLIES TO SPHERICAL CROWNS OF CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.24	0.265	0.29
A1		0.04 REF	
A3		0.025 REF	
b	0.12	0.17	0.22
D	0.81	0.86	0.91
E	1.65	1.70	1.75
e		0.40 BSC	

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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