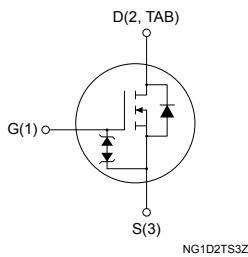
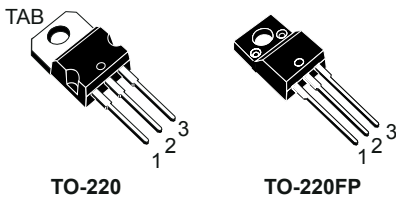


N-channel 800 V, 1.9 Ω typ., 4.3 A SuperMESH Power MOSFET in a TO-220 and TO-220FP packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP5NK80Z	800 V	2.4 Ω	4.3 A
STP5NK80ZFP			

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status links

[STP5NK80Z](#)

[STP5NK80ZFP](#)

Product summary

Order code	STP5NK80Z
Marking	P5NK80Z
Package	TO-220
Packing	Tube
Order code	STP5NK80ZFP
Marking	P5NK80ZFP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage	800		V
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	4.3	4.3 ⁽¹⁾	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	2.7	2.7 ⁽¹⁾	
$I_{DM}^{(2)}$	Drain current (pulsed)	17.2	17.2 ⁽¹⁾	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	110	30	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	3.5		kV
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_C = 25\text{ °C}$)	-	2.5	kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range			°C

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 4.3\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	1.14	4.2	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	4.3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	190	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	800	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$, $T_C = 125\text{ °C}^{(1)}$	-	-	50	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.15\text{ A}$	-	1.9	2.4	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	910	-	pF
C_{oss}	Output capacitance		-	98	-	pF
C_{riss}	Reverse transfer capacitance		-	20	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	40	-	pF
Q_g	Total gate charge	$V_{DD} = 640\text{ V}$, $I_D = 4.3\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 16. Test circuit for gate charge behavior)	-	32.4	45.5 ⁽²⁾	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Specified by design, not tested in production.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	18	-	ns
t_r	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	45	-	ns
t_f	Fall time		-	30	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	4.3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	17.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.3 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.3 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$,	-	500	-	ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 40 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	3	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	12	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for TO-220

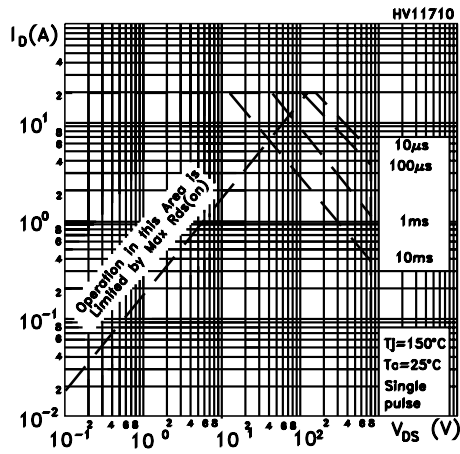


Figure 2. Normalized transient thermal impedance for TO-220

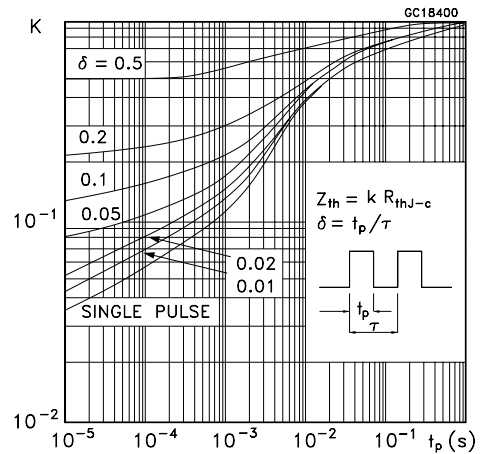


Figure 3. Safe operating area for TO-220FP

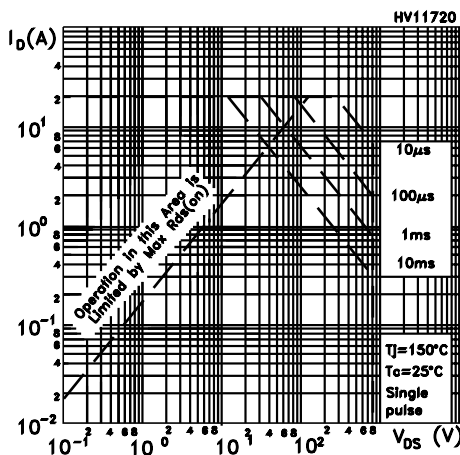


Figure 4. Normalized transient thermal impedance for TO-220FP

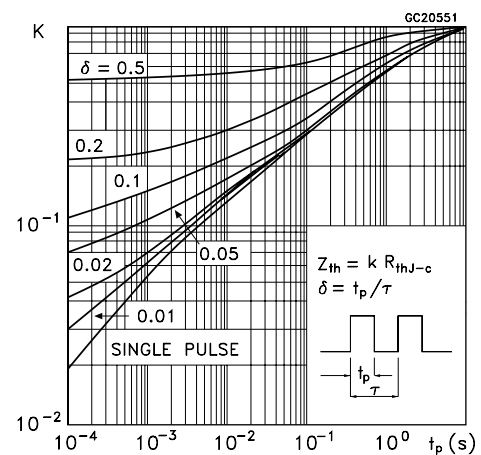


Figure 5. Typical output characteristics

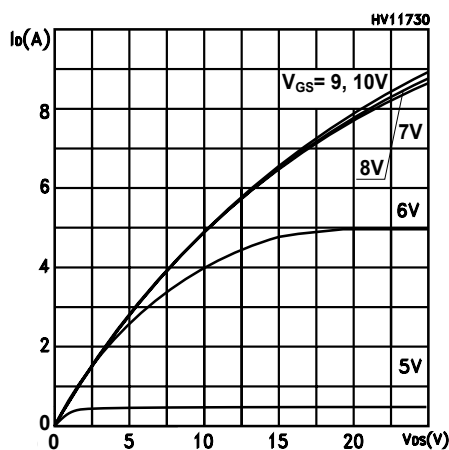


Figure 6. Typical transfer characteristics

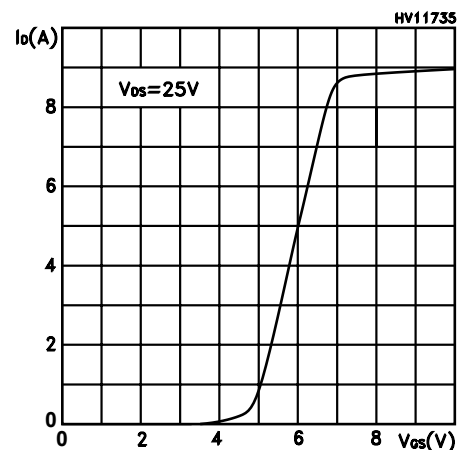


Figure 7. Typical static drain-source on-resistance

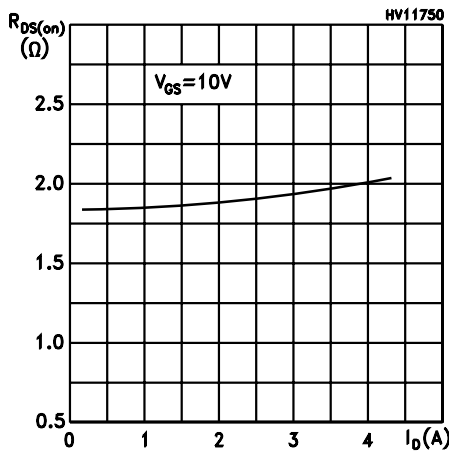


Figure 8. Typical gate charge characteristics

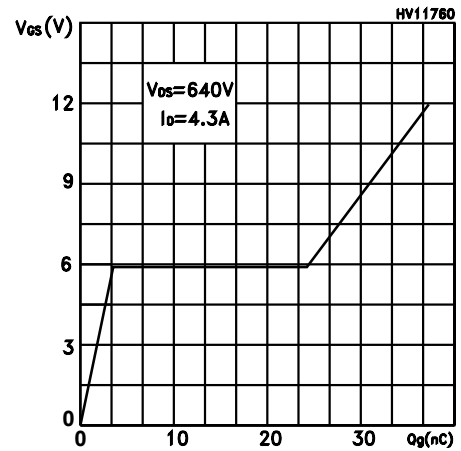


Figure 9. Typical capacitance variations

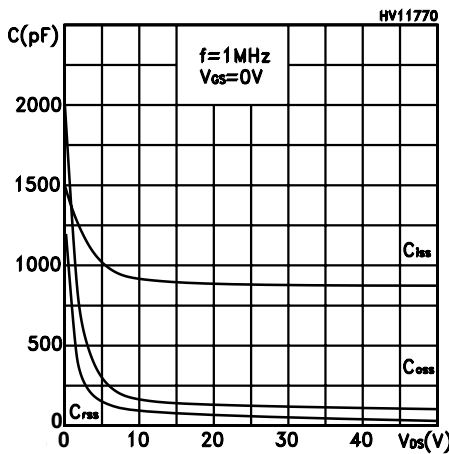


Figure 10. Normalized gate threshold vs temperature

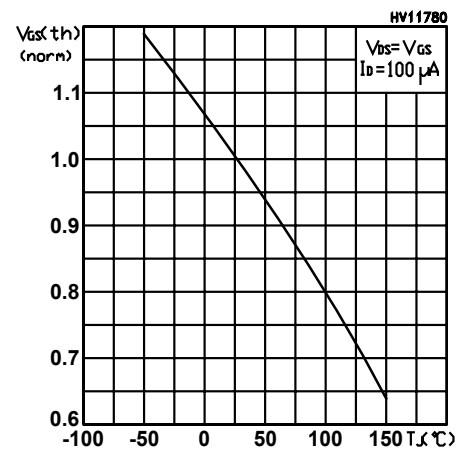


Figure 11. Normalized on-resistance vs temperature

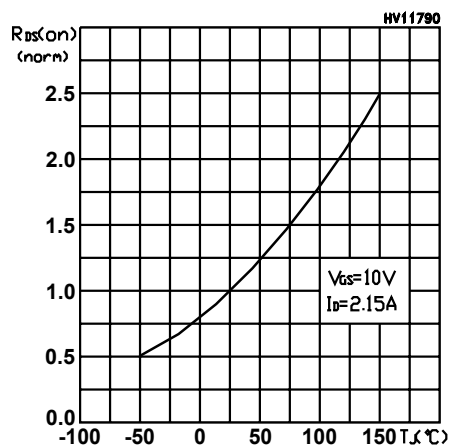


Figure 12. Typical reverse diode forward characteristics

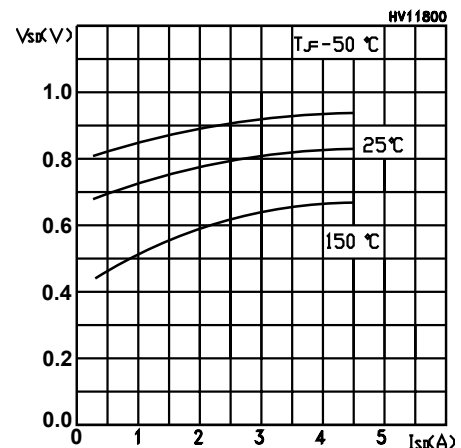


Figure 13. Normalized breakdown voltage vs temperature

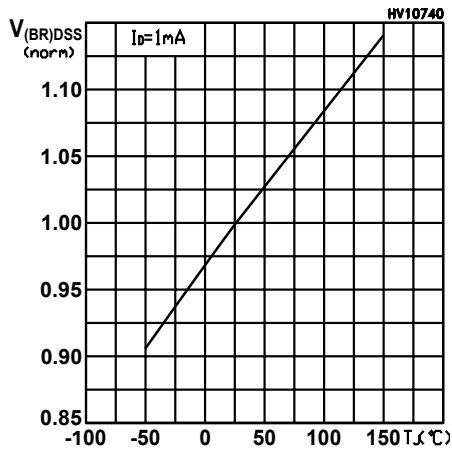
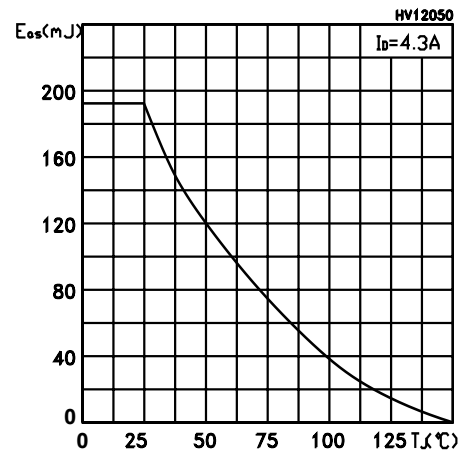
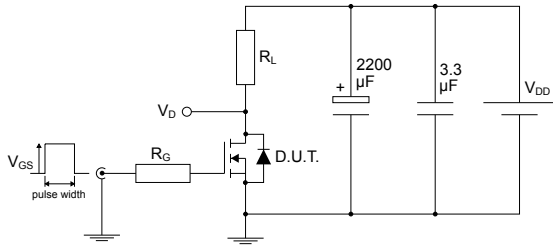


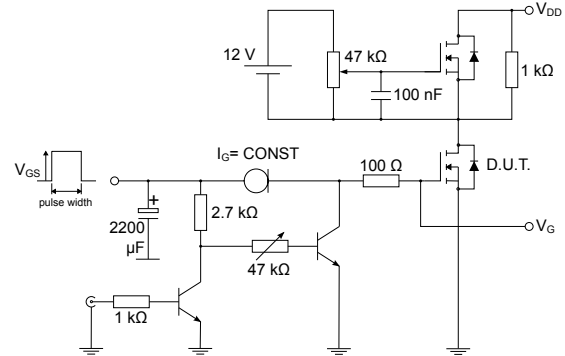
Figure 14. Maximum avalanche energy vs temperature



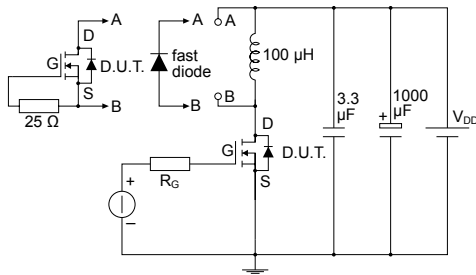
3 Test circuits

Figure 15. Test circuit for resistive load switching times


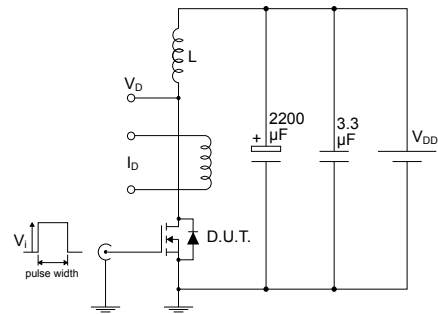
AM01468v1

Figure 16. Test circuit for gate charge behavior


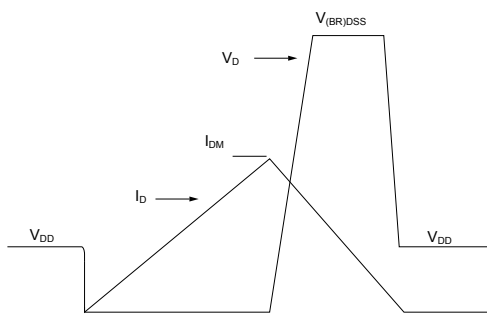
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Figure 17. Test circuit for inductive load switching and diode recovery times


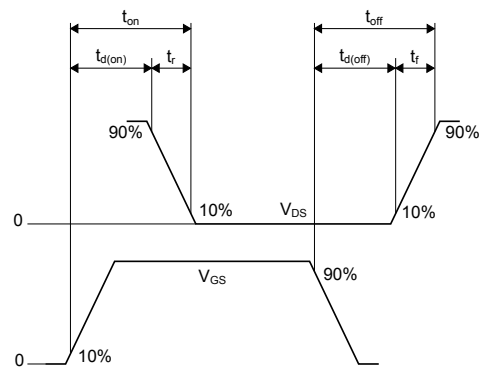
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Figure 18. Unclamped inductive load test circuit


AM01471v1

Figure 19. Unclamped inductive waveform


AM01472v1

Figure 20. Switching time waveform


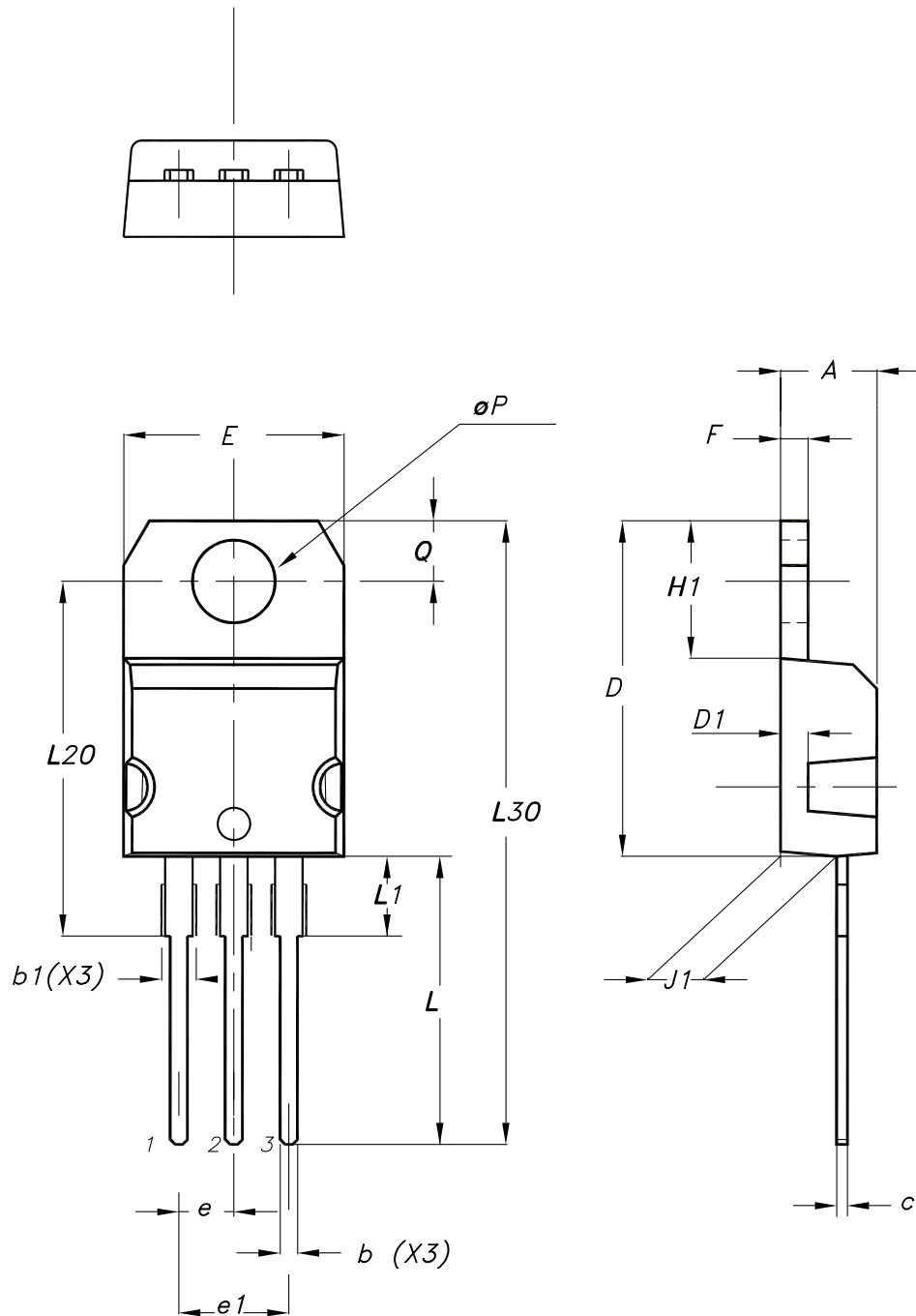
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 21. TO-220 type A package outline



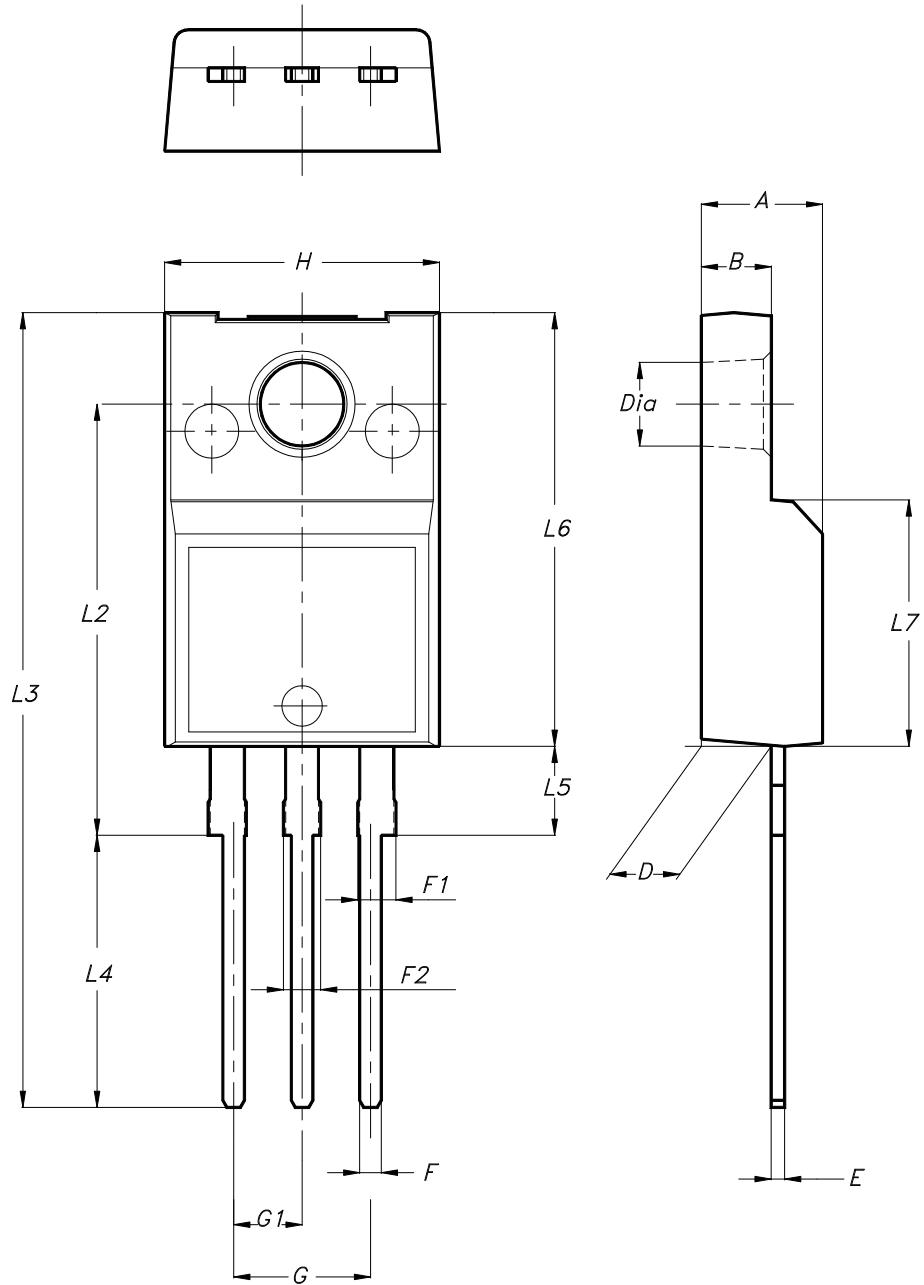
0015988_typeA_Rev_24

Table 8. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.2 TO-220FP type B package information

Figure 22. TO-220FP type B package outline



7012510_B_rev.14

Table 9. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 10. Document revision history

Date	Version	Changes
09-Sep-2004	2	Preliminary version.
06-Sep-2005	3	Final version.
16-Aug-2006	4	New template, no content change.
24-Mar-2026	5	Updated Section 4: Package information . Minor text changes.



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