CeraLink

Capacitor for fast-switching semiconductors

Series/Type: **Flex Assembly (FA) series**
Ordering code: **B58035U***

Date: 2023-08-20
Version: 6.4

Applications

- Power converters and inverters
- DC link/snubber capacitor for power converters and inverters

Features

- High ripple current capability
- High temperature robustness
- Low equivalent serial inductance (ESL)
- Low equivalent serial resistance (ESR)
- Low power loss
- Low dielectric absorption
- Optimized for high frequencies up to several MHz
- Increasing capacitance with DC bias up to operating voltage
- High capacitance density
- Minimized dielectric loss at high temperatures
- Qualification based on AEC-Q200 rev. D
- Suitable for reflow soldering only

Construction

- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate)
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper-invar leadframe
- Epoxy resin adhesive

General technical data

Dissipation factor	$\tan\delta$	< 0.02	
Insulation resistance	$R_{ins,typ}$ *)	> 0.1	GΩ
Operating device temperature	T_{device}	-40 … +150	°C

*) Typical insulation resistance, measured at operating voltage V_{op} and measurement time > 240 s, +25 °C

Overview of available types

$C_{nom,typ}$ (µF)	$V_{R,Tmax}$ (V_{DC}) 500	700	900
0.5			FA2
0.75			FA3
1		FA2	
1.5		FA3	
2	FA2		
2.5			FA10
3	FA3		
5		FA10	
10	FA10		

Electrical specifications and ordering codes

Type	$V_{pk,max}$ V	$V_{R,Tmax}$ *) V	V_{op} V	$C_{nom,typ}$ µF	$C_{eff,typ}$ µF	C_0 µF	Ordering code
FA2	650	500	400	2	1.20	0.70 ±20%	B58035U5205M062 B58035U5205M052 **)
	1000	700	600	1	0.50	0.28 ±20%	B58035U7105M062 B58035U7105M052 **)
	1300	900	800	0.5	0.26	0.14 ±20%	B58035U9504M062 ***) B58035U9504M052 **) ***)
FA3	650	500	400	3	1.80	1.05 ±20%	B58035U5305M062 B58035U5305M052 **)
	1000	700	600	1.5	0.75	0.42 ±20%	B58035U7155M062 B58035U7155M052 **)
	1300	900	800	0.75	0.39	0.21 ±20%	B58035U9754M062 ***) B58035U9754M052 **) ***)
FA10	650	500	400	10	6.00	3.50 ±20%	B58035U5106M001
	1000	700	600	5	2.50	1.40 ±20%	B58035U7505M001
	1300	900	800	2.5	1.30	0.70 ±20%	B58035U9255M001 ***)

*) $V_{R,Tmax}$ denotes the permissible rated voltage for the maximum device temperature T_{max} = +150 °C. Operation at higher rated voltage $V_R > V_{R,Tmax}$ is possible, where the permissible rated voltage V_R can be extracted from the temperature derating curves on the next page.

**) smaller packaging unit (180-mm reel), see section "Packaging" for details

***) This part is affected by "Dual Use" regulations according to the law of the country the production site is located in. Deliveries of such products are subject to prior approval of the respective local authorities based on customer declarations. The delivery to certain countries may be restricted.

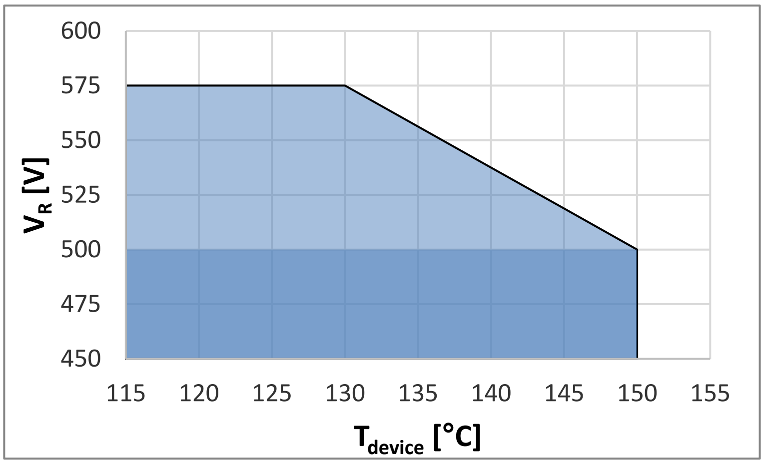
Aging

The capacitance has an aging behavior which shows a decrease of capacitance with time.
The typical aging rate is about 2.5% per logarithmic decade in hours.

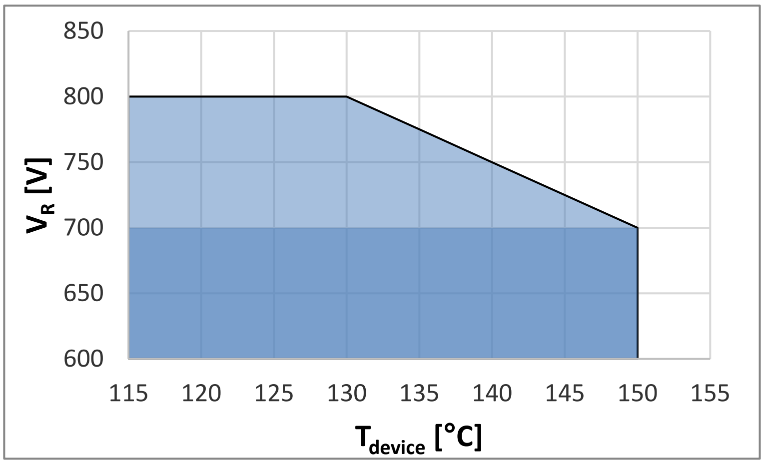
Rated voltage V_R and temperature derating

The CeraLink® FA series can be operated at elevated rated voltage, i.e. $V_R \geq V_{R,Tmax}$. However, the device temperature of the component should be kept within the temperature-derated conditions detailed in the following graphs. Higher device temperatures are permissible at reduced lifetime.

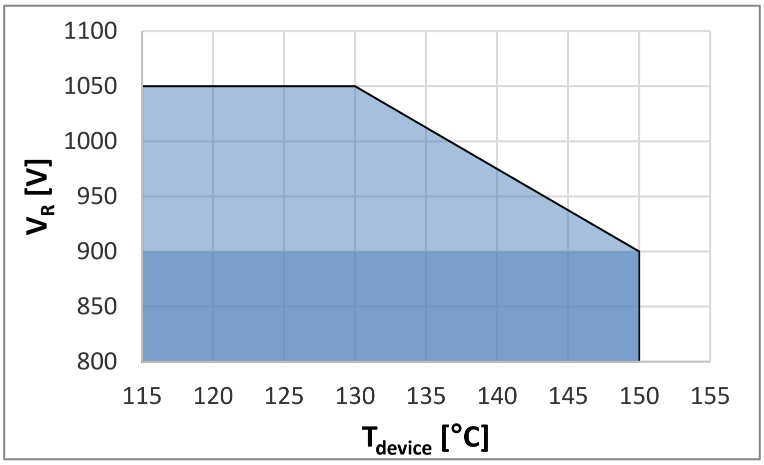
$V_{R,Tmax}$ = 500 V (B58035U5*)



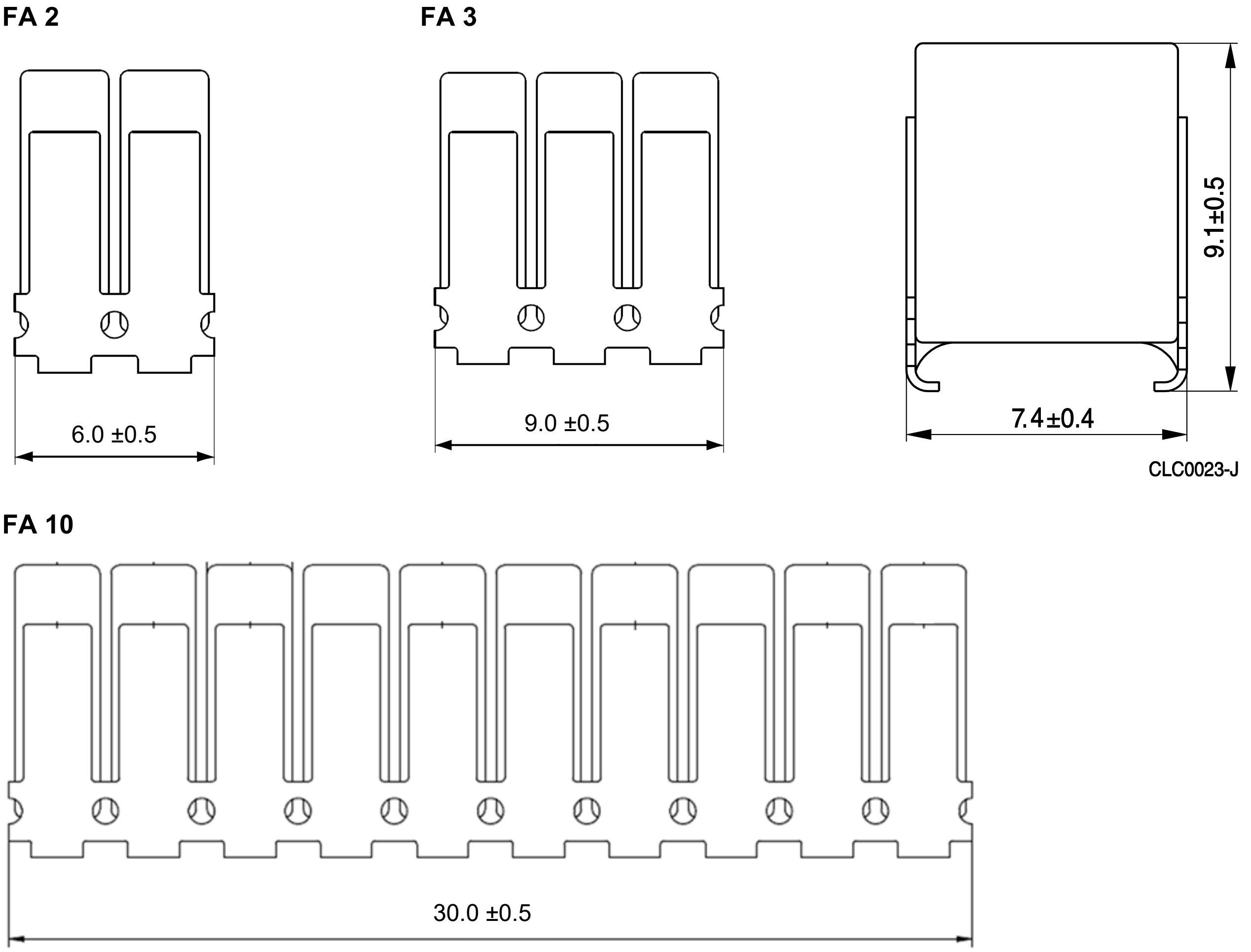
$V_{R,Tmax}$ = 700 V (B58035U7*)



$V_{R,Tmax}$ = 900 V (B58035U9*)

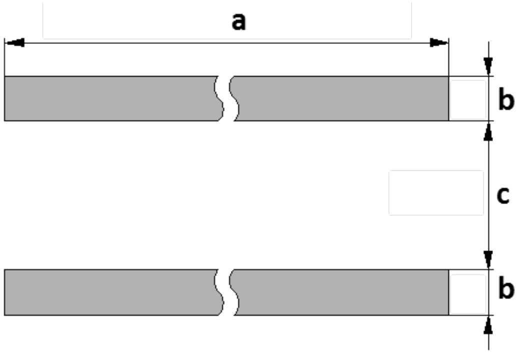


Dimensional drawings



Dimensions in mm

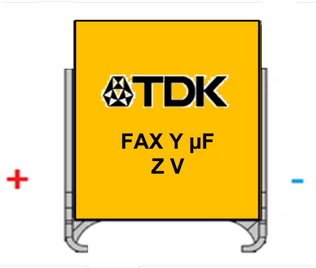
Recommended solder pads



Type	a	b	c
FA2	7	2.85	5
FA3	10	2.85	5
FA10	31	2.85	5

Dimensions in mm

Polarity and marking of components



Manufacturer’s logo
X = CeraLink FA type (e.g. FA2)
Y = Nominal capacitance
Z = Rated voltage

Note that polarity is only for incoming inspection purposes, and it does not affect operation. If put under reverse rated voltage V_R, CeraLink is repoled and works identically, see our *CeraLink Technical Guide* for further details.

Typical values as a design reference for CeraLink applications

Type	**$V_{R,Tmax}$** **V**	**Weight** **G**	**ESR** 0 V DC, 0.5 V AC (RMS), 25 °C, 1 kHz **Ω**	**ESR** 0 V DC, 0.5 V AC (RMS), 25 °C, 1 MHz **mΩ**	**ESL** **nH**	**I_{op} *)** V_{op}, 100 kHz, T_{amb} = 85 °C **A_{RMS}**	**I_{op} *)** V_{op}, 100 kHz, T_{amb} = 105 °C **A_{RMS}**
FA2		2.3	3	5	3	17	14
FA3	500	3.5	2	4		20	17
FA10		11.5	1	3	2	47	38
FA2		2.3	6	17	3	12	11
FA3	700	3.5	4	12		16	13
FA10		11.5	1	5	2	39	30
FA2		2.3	11	29	3	8	7
FA3	900	3.5	7	20		11	9
FA10		11.5	2	7	2	32	23

*) Normal operating current without forced cooling at T_{device} = +150 °C. Higher values permissible at reduced lifetime.

Application Notes

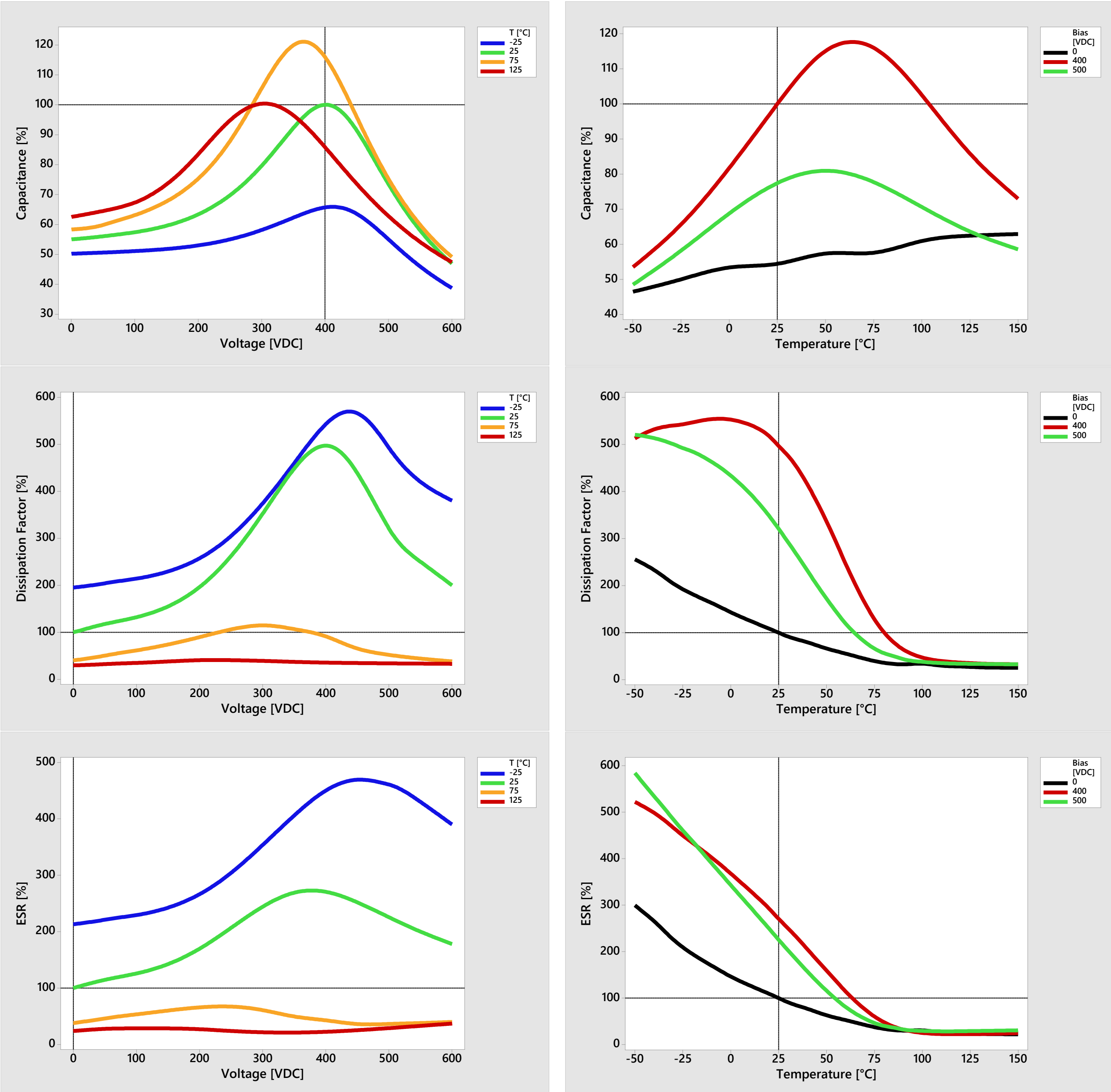
Further typical electrical characteristics as a design reference for CeraLink applications

Typical characteristics as a function of temperature and voltage – $V_{R,Tmax}$ = 500 V

(0.5 V AC (RMS), frequency = 1 kHz)

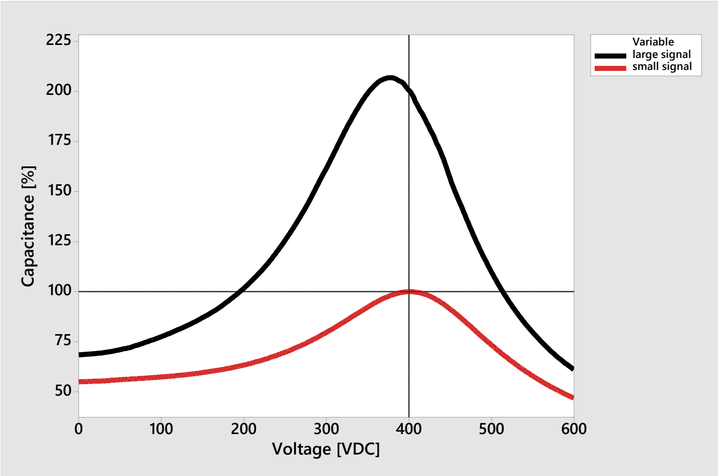
All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100%-values correspond to tanδ, $C_{eff,typ}$ and ESR_{1kHz} which are given on page 2, 3 and 6 of this data sheet.



Typical capacitance values as a function of voltage – $V_{R,Tmax}$ = 500 V

(valid for FA2, FA3 and FA10)



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at V_{op}.

See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

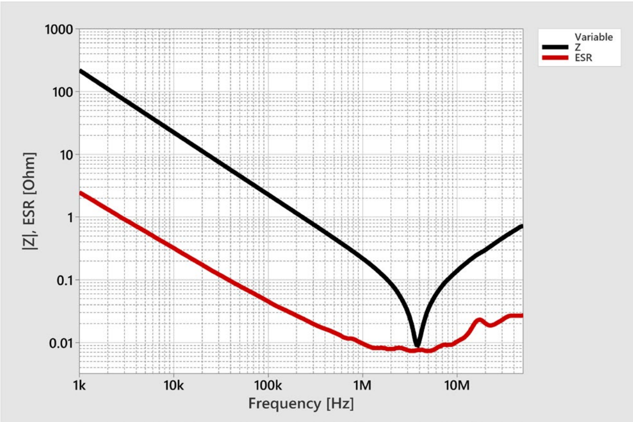
The effective capacitance is defined as the small signal capacitance at V_{op}.

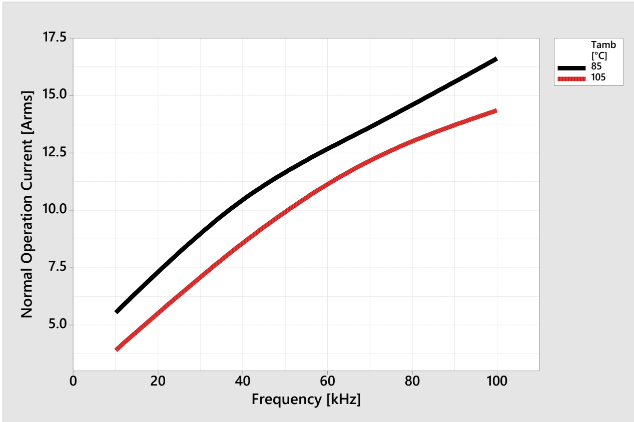
Typical impedance, ESR and permissible current as a function of frequency – $V_{R,Tmax}$ = 500 V

0 V DC, 0.5 V AC (RMS), T_{device} = +25 °C

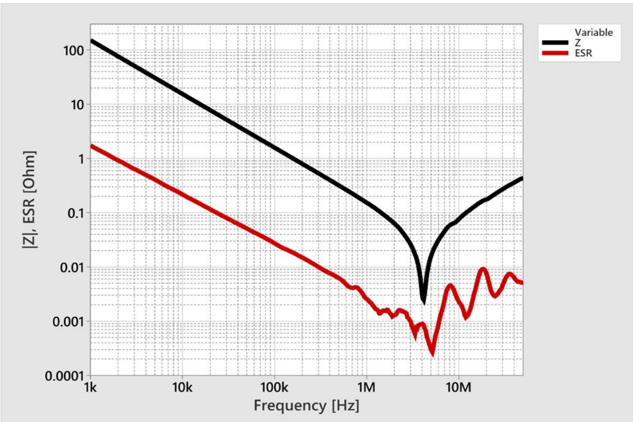
Measurements performed at V_{op}.
The values correspond to a device temperature of +150 °C. No forced cooling was used.

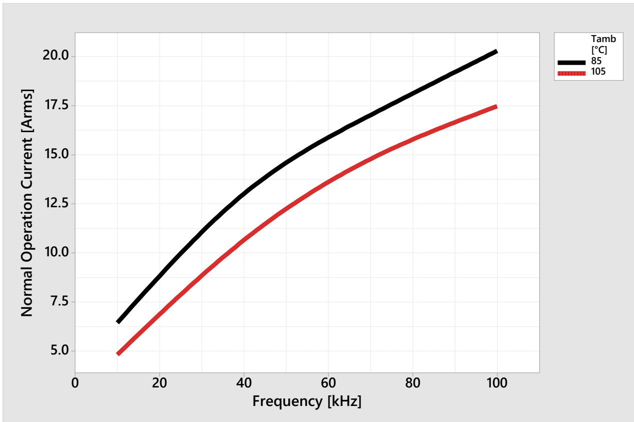
FA2



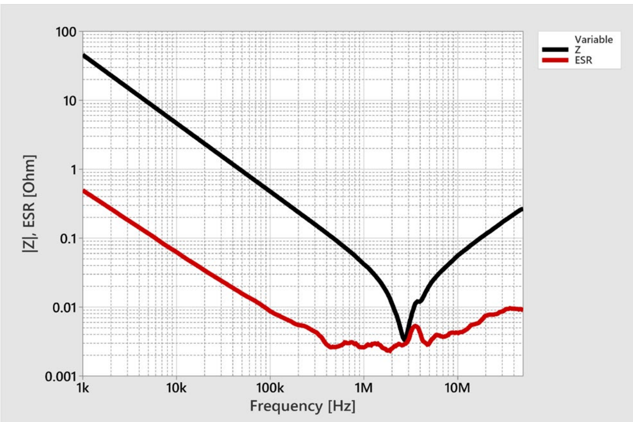


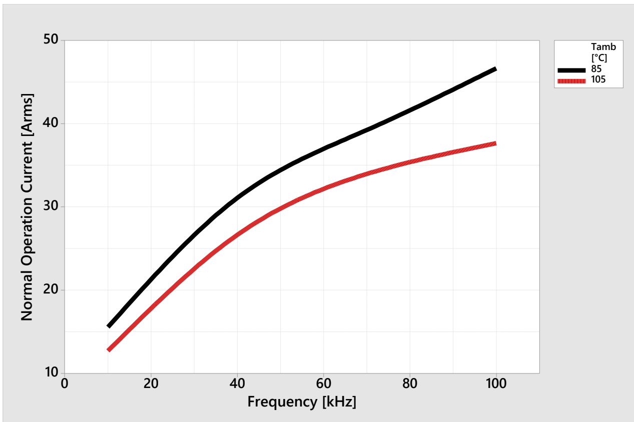
FA3





FA10



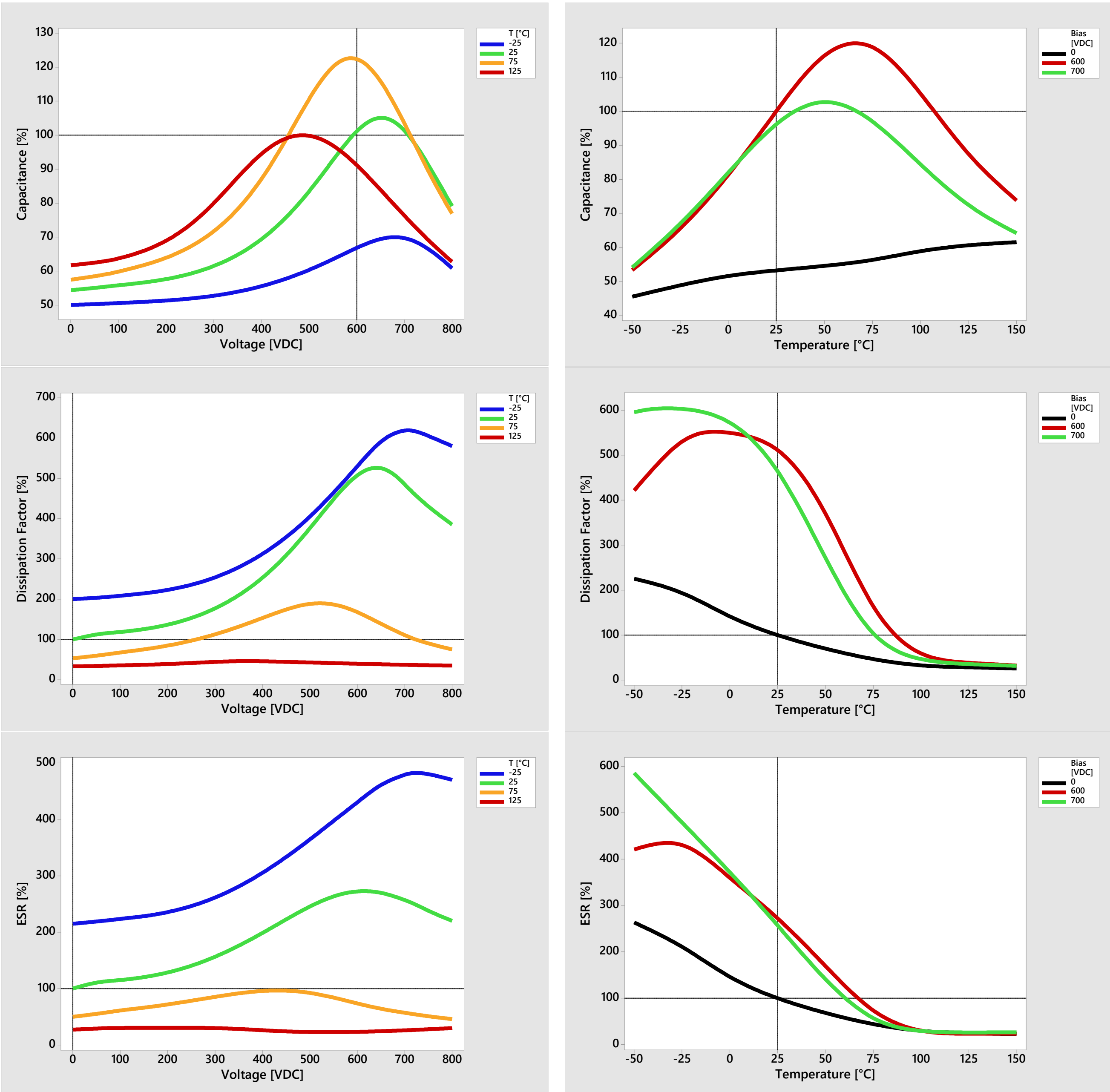


Typical characteristics as a function of temperature and voltage – $V_{R,Tmax}$ = 700 V

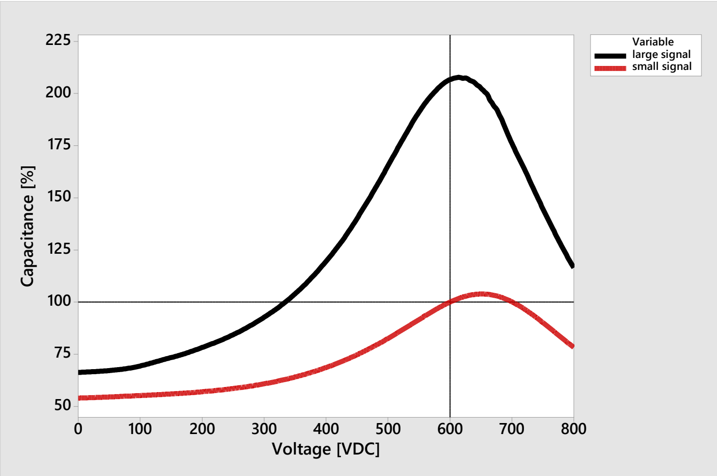
(0.5 V AC (RMS), frequency = 1 kHz)

All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100%-values correspond to tanδ, $C_{eff,typ}$ and ESR_{1kHz} which are given on page 2, 3 and 6 of this data sheet.



Typical capacitance values as a function of voltage – $V_{R,Tmax}$ = 700 V (valid for FA2, FA3 and FA10)



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at V_{op}.

See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

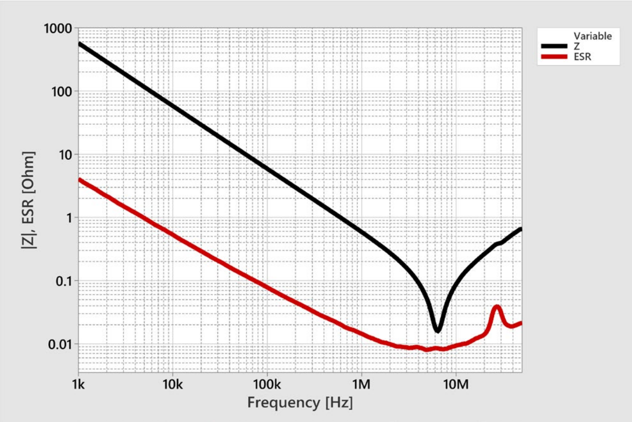
The effective capacitance is defined as the small signal capacitance at V_{op}.

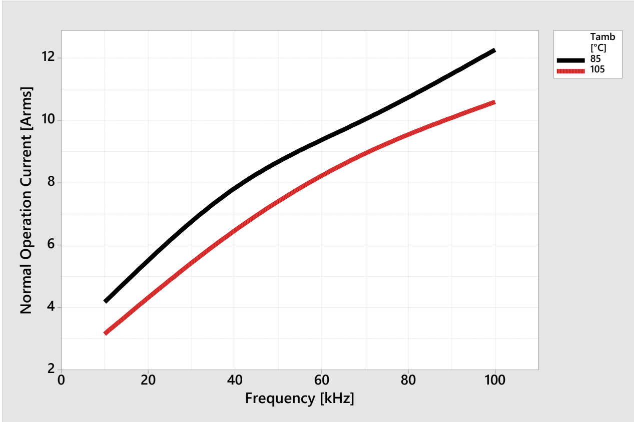
Typical impedance, ESR and permissible current as a function of frequency – $V_{R,Tmax}$ = 700 V

0 V DC, 0.5 V AC (RMS), T_{device} = +25 °C

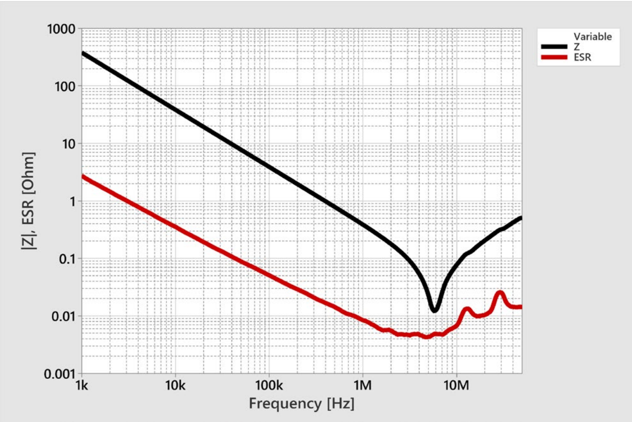
Measurements performed at V_{op}.
The values correspond to a device temperature of +150 °C. No forced cooling was used.

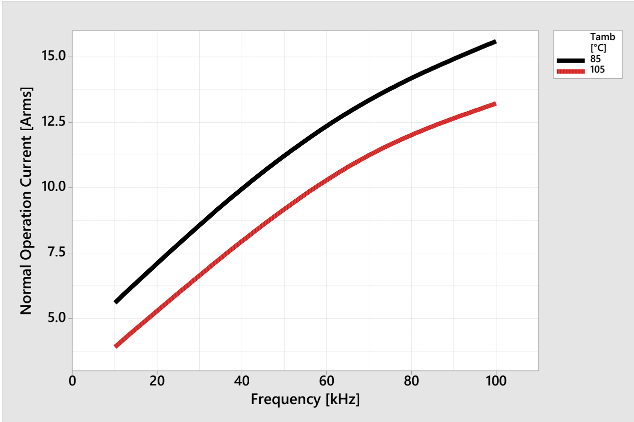
FA2



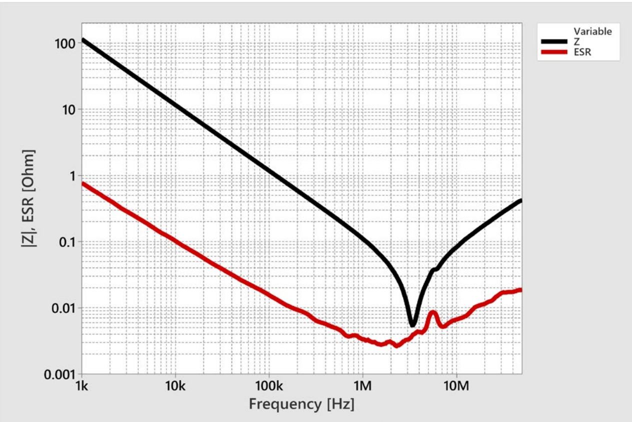


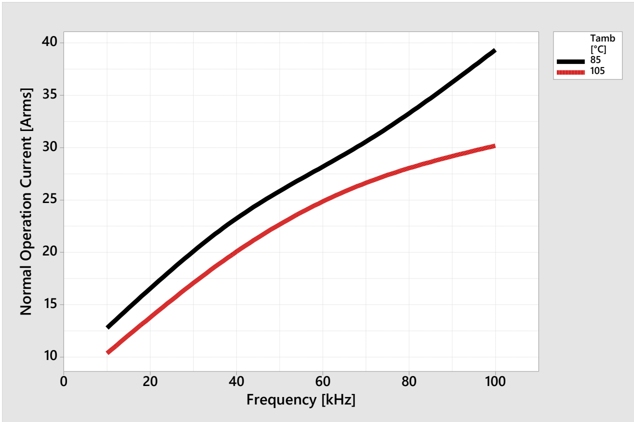
FA3





FA10



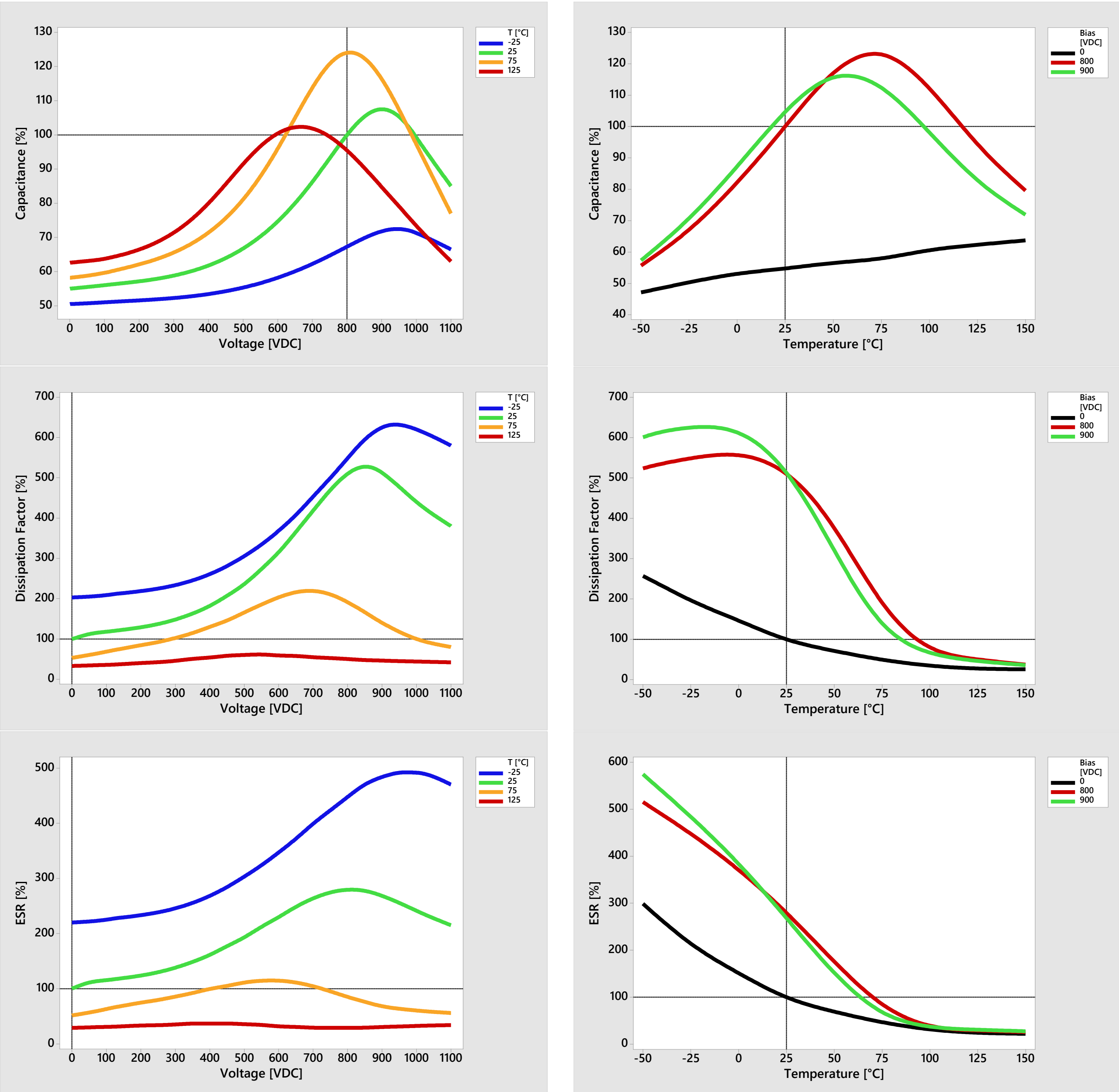


Typical characteristics as a function of temperature and voltage – $V_{R,Tmax}$ = 900 V

(0.5 V AC (RMS), frequency = 1 kHz)

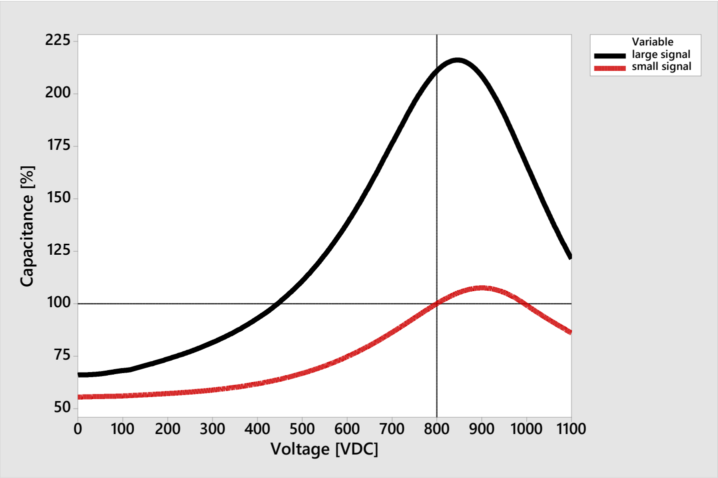
All given temperatures are device temperatures.

The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100%-values correspond to tanδ, $C_{eff,typ}$ and ESR_{1kHz} which are given on page 2, 3 and 6 of this data sheet.



Typical capacitance values as a function of voltage – $V_{R,Tmax}$ = 900 V

(valid for FA2, FA3 and FA10)



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C

The nominal capacitance is defined as the large signal capacitance at V_{op}.

See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

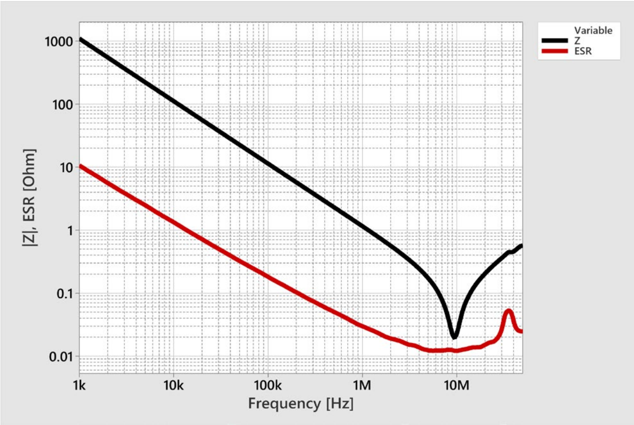
The effective capacitance is defined as the small signal capacitance at V_{op}.

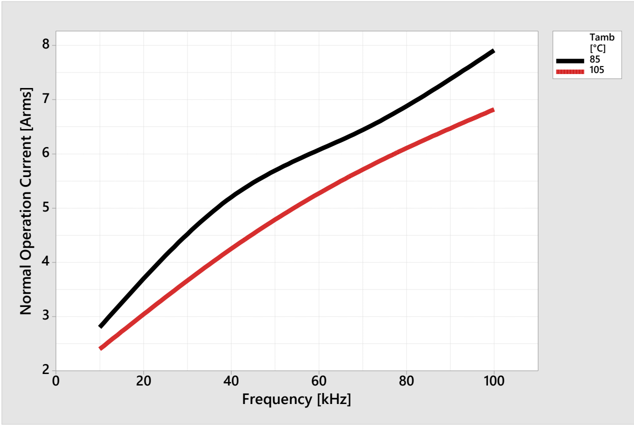
Typical impedance, ESR and permissible current as a function of frequency – $V_{R,Tmax}$ = 900 V

0 V DC, 0.5 V AC (RMS), T_{device} = +25 °C

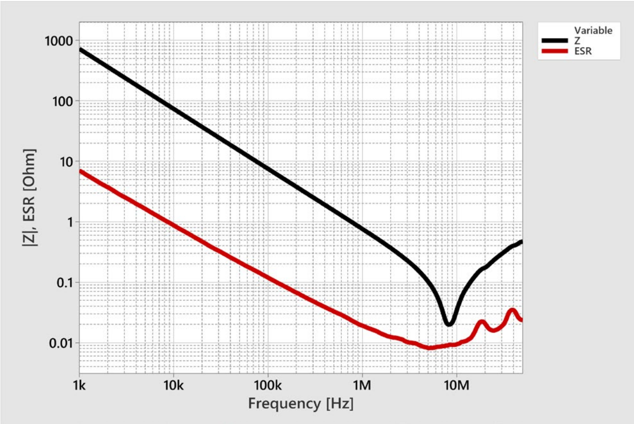
Measurements performed at V_{op}.
The values correspond to a device temperature of +150 °C. No forced cooling was used.

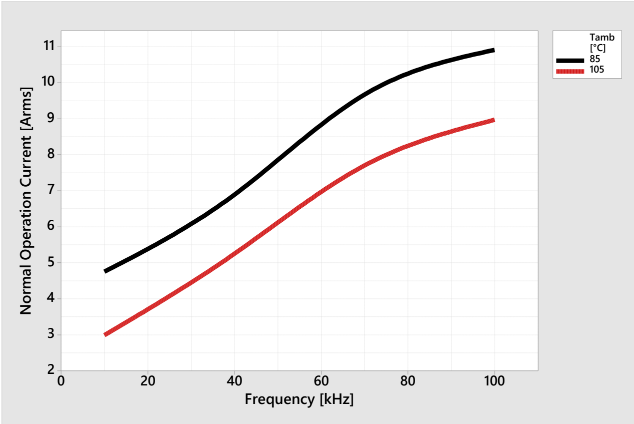
FA2



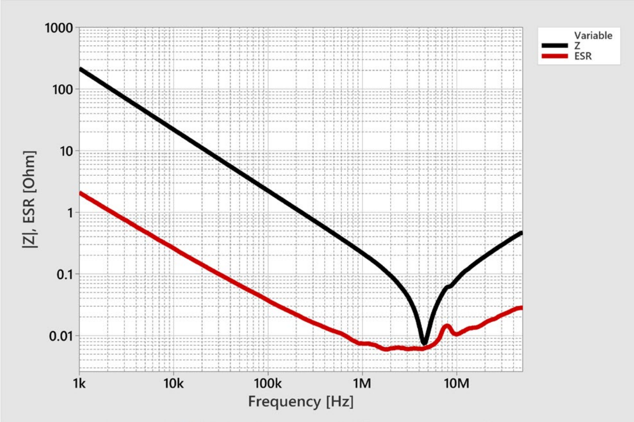


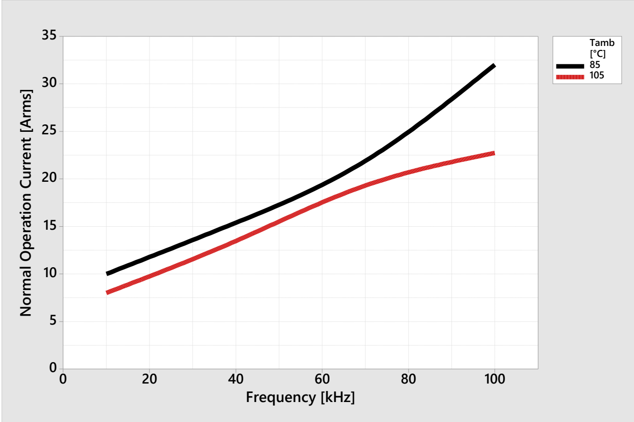
FA3





FA10





Reliability

A. Preconditioning

- Reflow solder the capacitor on a PCB using the recommended soldering profile
- Check of external appearance
- Measurement of isolation resistance R_{ins} *)
  - Apply $V_{pk,max}$ for 7 seconds and measure R_{ins} at room temperature:
    Isolation resistance (@ $V_{pk,max}$, 7 s, 25 °C) **R_{ins} > 100 MΩ**
- Measurement of electrical parameters C_0 and tanδ according to specification
  - Measure C_0 and tanδ within 10 minutes to 1 hour afterwards:
    Initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **C_0 acc. spec. on page 3**
    Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tanδ < 0.02**

B. Performance of a specific reliability test

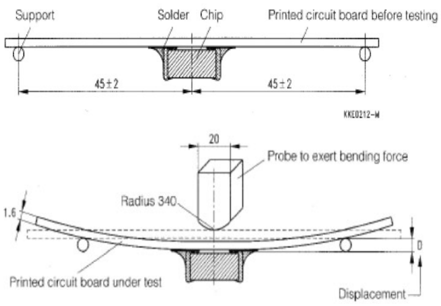
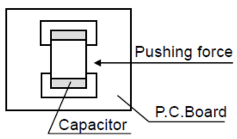
C. After performing a specific test

- Check the external appearance again
- Repeat the measurement of the electrical parameters
  - Apply $V_{pk,max}$ for 7 seconds and measure R_{ins} at room temperature:
    Isolation resistance (@ $V_{pk,max}$, 7 s, 25 °C) **R_{ins} > 100 MΩ**
  - Measure C and tanδ:
    Change of initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **$|\Delta C_0 / C_0|$ < 15%**
  - Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tanδ < 0.05**

*) Note that the measurement of the isolation resistance R_{ins} using the described measurement conditions is for pre- and post-measurement within the scope of the AEC-Q200 reliability tests only.

Qualification tests based on AEC-Q200 Rev. D (Table 2)

Test	AEC-Q200 No.	Standard	Test conditions	Criteria
Pre- and Post-Stress Electrical	1	-	As described above	$|\Delta C_0/C_0|$, tanδ and R_{ins} within defined limits.
High Temperature Exposure	3	MIL-STD-202 Method 108	+150 °C, unpowered, 1000 hours	No mechanical damage. $|\Delta C_0/C_0|$, tanδ and R_{ins} within defined limits.
Temperature Cycling	4	JESD22 Method JA-104	-55 °C to +150 °C, ≤ 20 seconds transfer time, 15 minutes dwell time, 1000 cycles	No mechanical damage $|\Delta C_0 / C_0|$, tanδ and R_{ins} within defined limits
Destructive Physical Analysis	5	EIA-469	-	No internal defects that might affect performance or reliability
Biased Humidity	7	MIL-STD-202, Method 103	+85 °C, 85% rel. hum., $V_{R,Tmax}$, 1000 hours	No mechanical damage $|\Delta C_0 / C_0|$, tanδ and R_{ins} within defined limits

Test	AEC-Q200 No.	Standard	Test conditions	Criteria
High Temperature Operating Life	8	MIL-STD-202, Method 108	+150 °C, $V_{R,Tmax}$, 1000 hours	No mechanical damage $\lvert \Delta C_0 / C_0 \rvert$, tanδ and R_{ins} within defined limits
External Visual	9	MIL-STD-883 Method 2009	Visual inspection with magnifying glass	No defects that might affect performance
Physical Dimension	10	JESD22 JB-100	Verify physical dimensions to the device specification using a caliper	Within specified tolerance in the chapter construction
Resistance to Solvent	12	MIL-STD-202 Method 215	Dipping and cleaning with isopropanol	Marking must be legible $\lvert \Delta C_0 / C_0 \rvert$, tanδ and R_{ins} within defined limits
Mechanical Shock	13	MIL-STD-202, method 213	Acceleration 400 m/s², half-sine pulse, duration 6 msec, 4000 bumps	No mechanical damage $\lvert \Delta C_0 / C_0 \rvert$, tanδ and R_{ins} within defined limits
Vibration	14	MIL-STD-202, method 204	5 g / 20 min, 12 cycles, 3 axes, 10 Hz to 2000 Hz	No mechanical damage $\lvert \Delta C_0 / C_0 \rvert$, tanδ and R_{ins} within defined limits
Solderability	18	See below		
Board Flex	21	AEC-Q200-005	Bending of 2 mm for 60 seconds  Dimensions in mm	No mechanical damage $\lvert \Delta C_0 / C_0 \rvert$, tanδ and R_{ins} within defined limits
Terminal Strength	22	AEC-Q200-006	Apply a force of 17.7 N for 60 s 	No detaching of termination. No rupture of ceramic $\lvert \Delta C_0 / C_0 \rvert$, tanδ and R_{ins} within defined limits

Solderability tests

Wettability (leadframe only)	J-STD-002, Method A @ 235 °C, cat. 3	Dip test of contact areas in solder bath (+235 °C for 5 ±0.5 seconds)	> 95% wettability of lead frame
Leaching test (leadframe only)	MIL-STD-202, Method 210, cond. B	Dip test of contact areas in solder bath (+260 °C for 10 seconds)	No damage of lead frame silver coating
Reflow test	-	3 times recommended reflow soldering profile	No mechanical damage Proper solder coating of contact areas $\lvert \Delta C_0 / C_0 \rvert$, tanδ and R_{ins} within defined limits

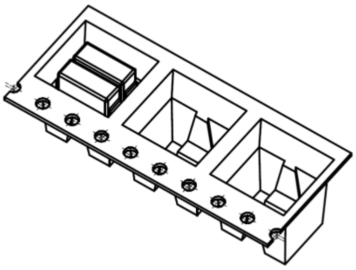
Packaging

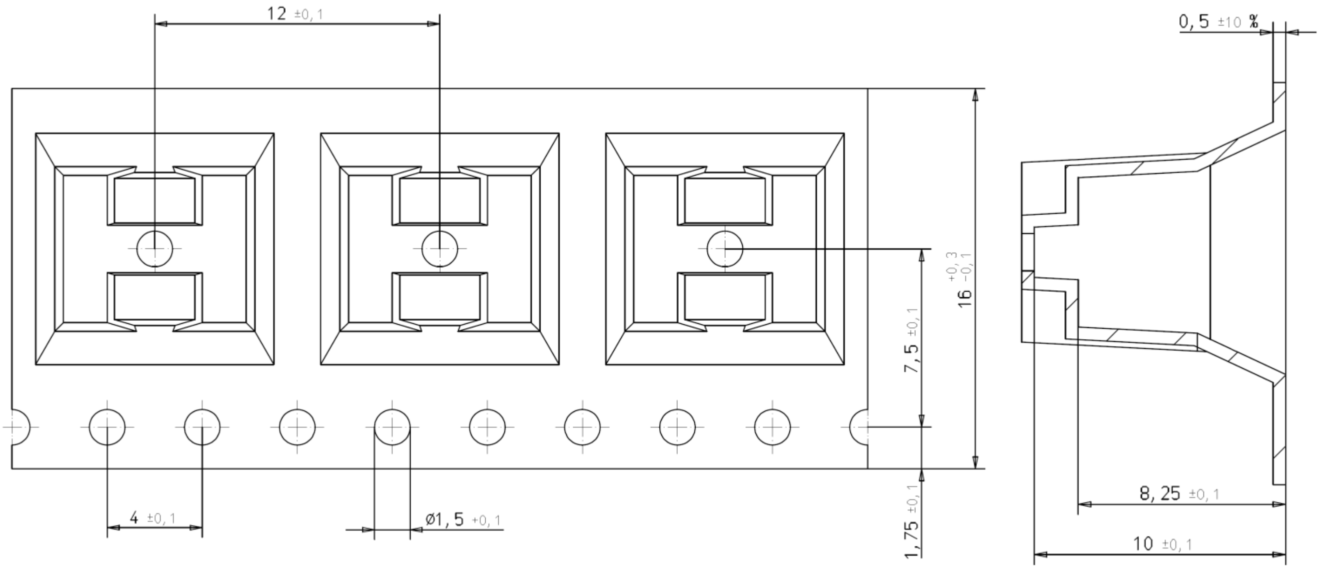
The CeraLink FA2 type is delivered in a blister tape (taping to IEC 60286-3, 180-mm / 330-mm reel available with 110 / 500 pieces per reel).

The CeraLink FA3 type is delivered in a blister tape (taping to IEC 60286-3, 180-mm / 330-mm reel available with 100 / 350 pieces per reel).

The CeraLink FA10 type is delivered in a cardboard box with 100 pieces per box.

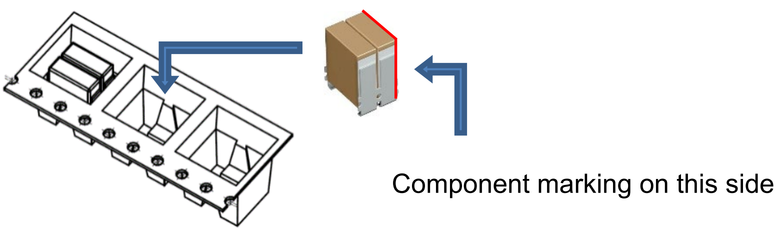
Blister tape for FA2



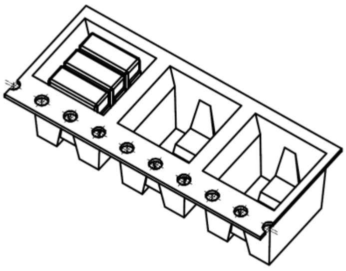


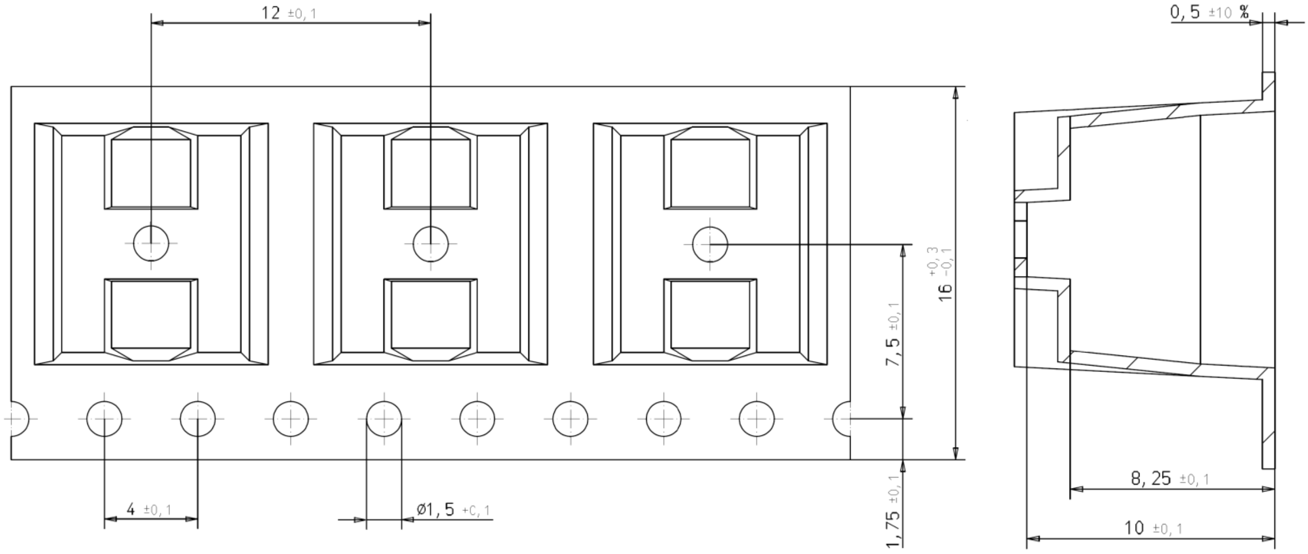
Part orientation

The part-orientation/polarity is the same for all CeraLink FA2 capacitors within the blister tape.



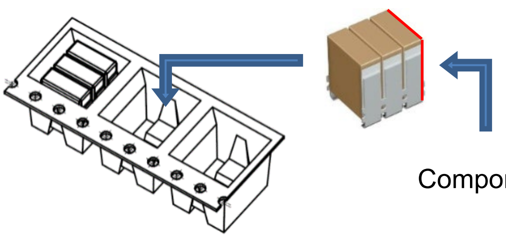
Blister tape for FA3





Part orientation

The part-orientation/polarity is the same for all CeraLink FA3 capacitors within the blister tape.

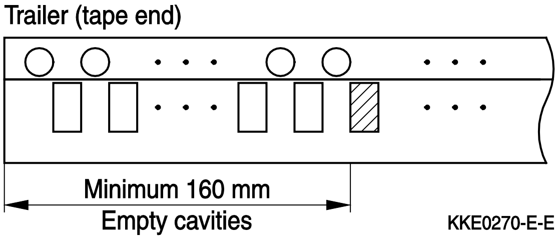


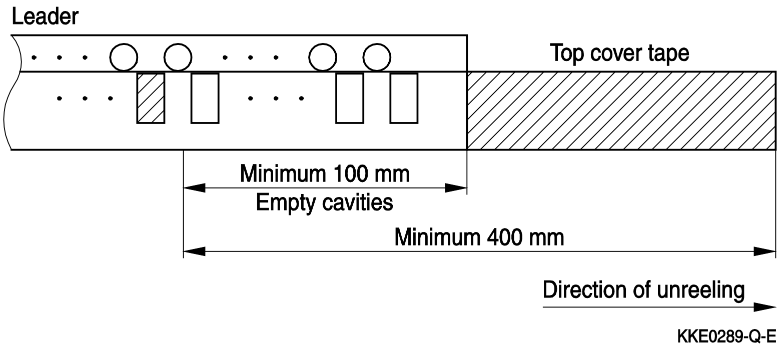
Component marking on this side

Taping information

Trailer: There is a minimum of 160 mm of carrier tape with empty compartments and sealed by the cover tape.

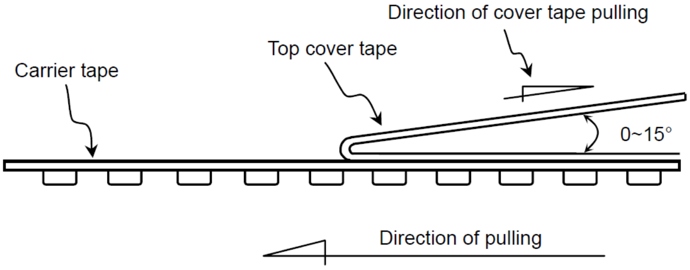
Leader: There is a minimum of 400 mm of cover tape, which includes at least 100 mm of carrier tape with empty compartments.



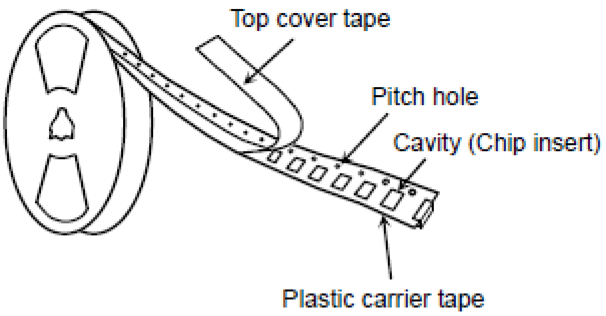


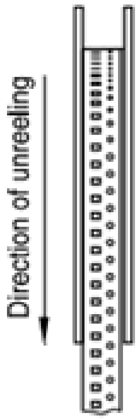
Fixing peeling strength (top tape)

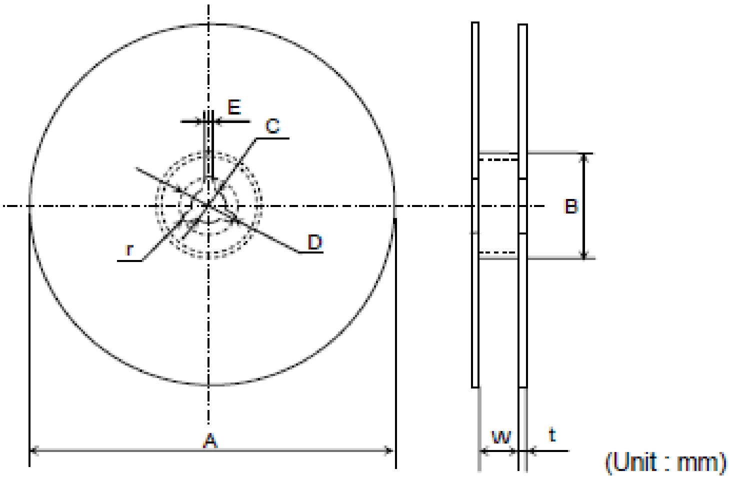
The peeling strength is 0.1 … 1.3 N.



Reel packing



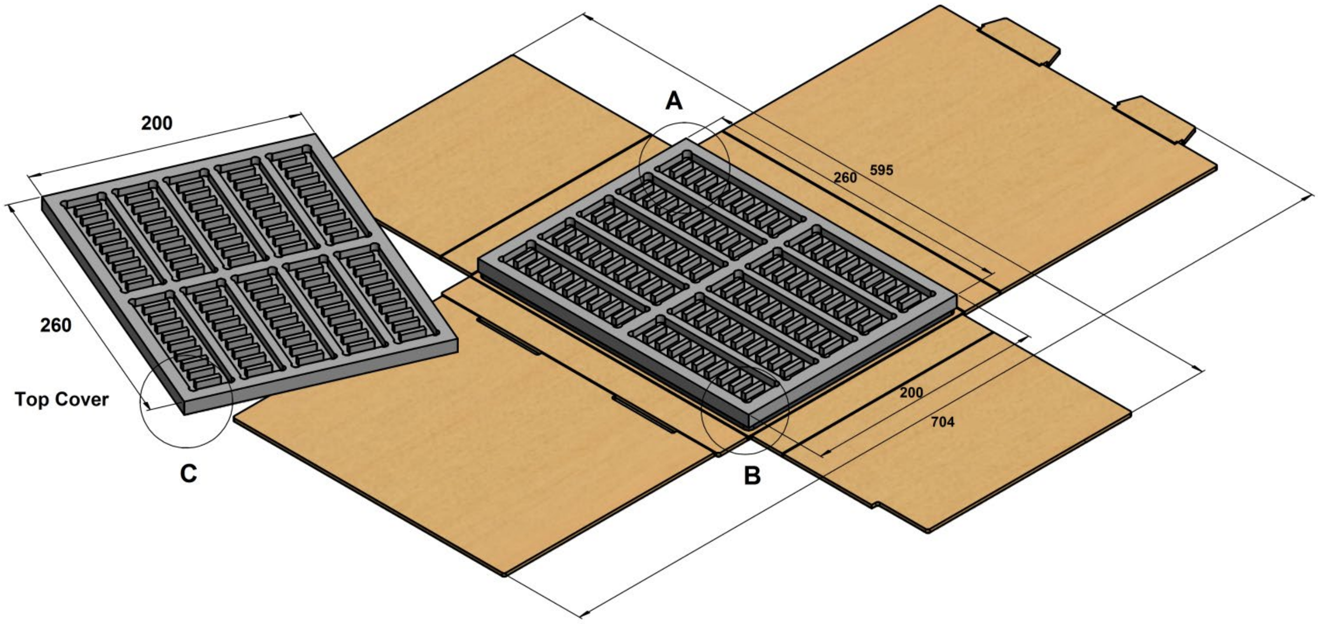


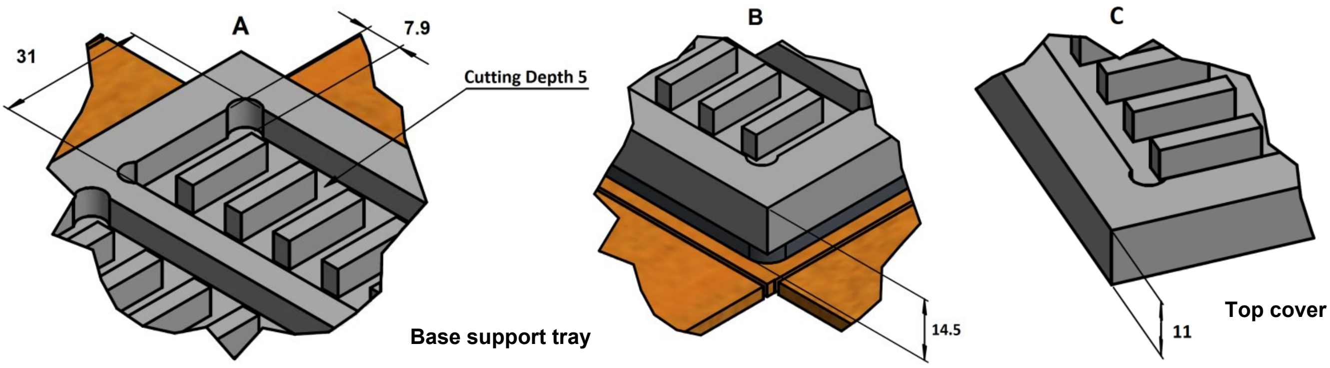


	FA2 & FA3 Type 330-mm reel	FA2 & FA3 Type 180-mm reel
A	330 ±2	180 ±3
B	62 ±1	62 ±1
C	12.8 +0.7	13.1 ±0.5
D	19.1 min.	19.1 min.
E	1.6 ±0.5	2.1 ±0.5
W	16.4 +2	17.0 -0.5 / +2

Dimensions in mm

Cardboard box for FA10

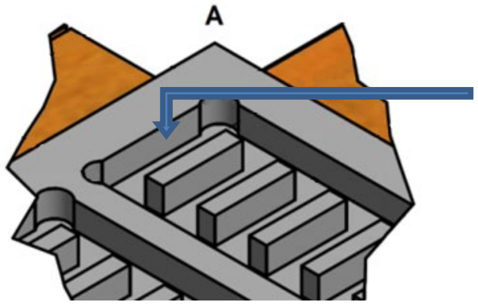


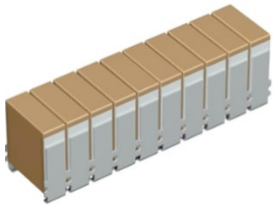


Dimensions in mm

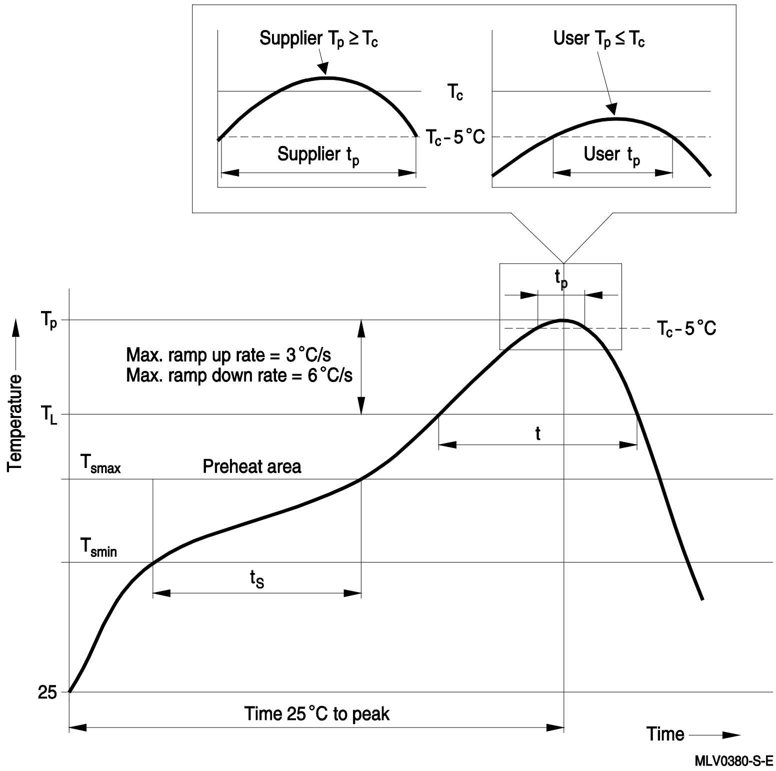
Part orientation

The part-orientation/polarity is the same for all CeraLink FA10 capacitors within the tray. Parts are placed with leadframes facing base support tray as shown.





Recommended reflow-soldering profile



Profile feature		SAC, Sn95.5Ag3.8Cu0.7 @ N_2 atmosphere
Preheat and soak - Temperature min - Temperature max - Time	 T_{smin} T_{smax} t_{smin} to t_{smax}	 +150 °C +200 °C 60 … 120 seconds
Average ramp-up rate	T_L to T_p	3 °C/ second max.
Liquidus temperature Time at liquidus temperature	T_L t_L	+217 °C 60 … 150 seconds
Peak package body temperature	T_p 1)	245 °C … 260 °C max. 2)
Time (t_p) 3) within +5 °C of specified classification temperature (T_c)		30 seconds 3)
Average ramp-down rate	T_p to T_L	+6 °C/ second max.
Time +25 °C to peak temperature		maximum 8 minutes

1) Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
2) Depending on package thickness (cf. JEDEC J-STD-020D).
3) Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Notes:
All temperatures refer to topside of the package, measured on the package body surface.
Max. number of reflow cycles: 3
After the soldering process, the capacitance is lowered. Applying V_R to the device will re-establish the capacitance.
The proposed soldering profile is based on IEC 60068-2-58 (respectively JEDEC J-STD-020D) recommendations.

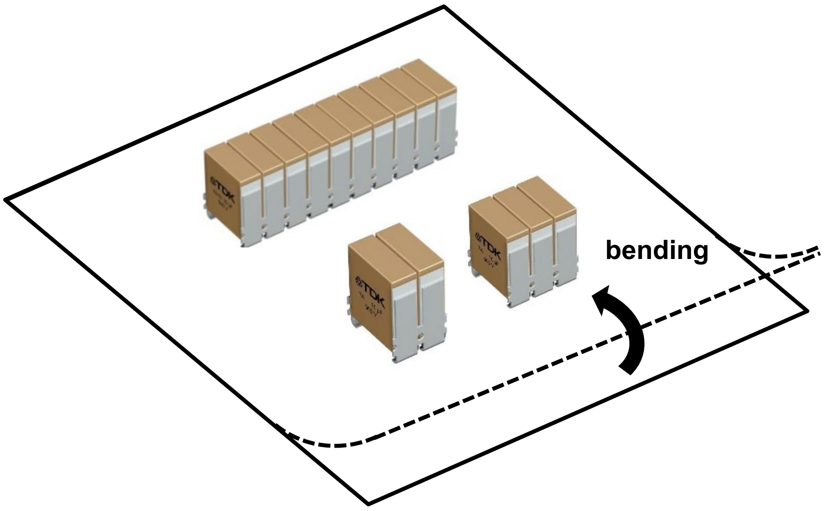
General technical information

Storage

- Only store CeraLink capacitors in their original packaging. Do not open the package prior to processing.
- Storage conditions in original packaging: temperature −25 °C to +45 °C, relative humidity ≤ 75% annual average, maximum 95%, dew precipitation is inadmissible.
- Do not store CeraLink capacitors where they are exposed to heat or direct sunlight. Otherwise the packaging material may be deformed or CeraLink may stick together, causing problems during mounting.
- Avoid contamination of the CeraLink surface during storage, handling, and processing.
- Avoid storing CeraLink devices in harmful environments where they are exposed to corrosive gases (e.g. SOx, Cl).
- Use CeraLink as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- Solder CeraLink components within 12 months after shipment.

Handling

- Do not drop CeraLink components or allow them to be chipped.
- Do not clamp CeraLink components on the face sides (e.g. during pick-and-place). A vacuum-based pick-and-place process picking the component on the top side is recommended.
- Do not touch CeraLink with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink surface during handling.
- The CeraLink FA series was tested to withstand the board flex test defined in the AEC-Q200 rev D, method 005.
- The CeraLink FA series uses copper-invar lead frames to prevent mechanical stress to the ceramic. Too much bending causes open mode. Avoid high mechanical stress like twisting after soldering on a PCB.

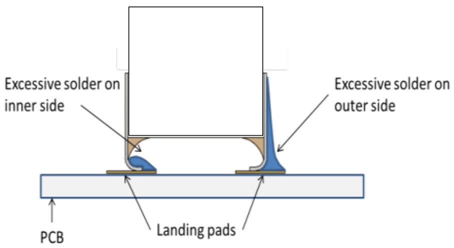


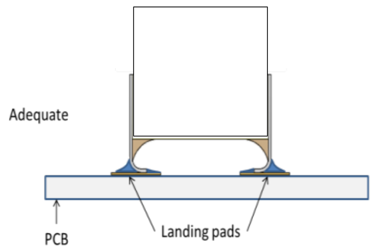
Mounting

- Do not subject CeraLink devices to mechanical stress when encapsulating them with sealing material or overmolding with plastic material. Encapsulation may lead to worse heat dissipation too. Please ask for further information.
- Do not scratch the electrodes before, during or after the mounting process.
- Make sure contacts and housings used for assembly with CeraLink components are clean before mounting.
- The surface temperature of an operating CeraLink can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink to allow proper cooling.
- Avoid contamination of the CeraLink surface during processing.

Soldering guidelines

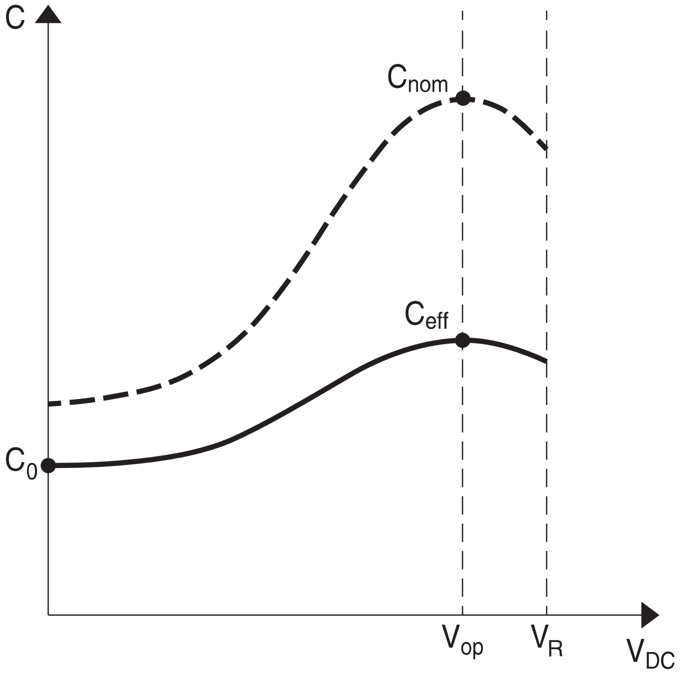
- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB.
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- Excessive usage of solder paste can reduce the mechanical robustness of the device, whereas insufficient solder may cause the CeraLink to detach from the PCB. Use an adequate amount of solder paste, but on the landing pads only.





- If an unsuitable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink may cause damage to the component.
- Excessive washing like ultrasonic cleaning, can affect the connection between the ceramic chip and the outer electrode. To avoid this, we give the following recommendation:
  - Power: 20 W/l max.
  - Frequency: 40 kHz max.
  - Washing time: 5 minutes max.

Glossary



Initial capacitance C_0:	Is the value at the origin of the hysteresis without any applied direct voltage.
Effective capacitance C_{eff}:	Occurs at V_{op} and is measured with an applied ripple voltage of 0.5 V AC (RMS) and 1 kHz. The CeraLink is designed to have its highest capacitance value at the operating voltage V_{op}.
Nominal capacitance C_{nom}:	Is the value derived by the tangent of the mean hysteresis as the derivative of the mean hysteresis is dQ/dV ~ C.

See our *CeraLink Technical Guide* for further details.

Symbols and terms

AC	Alternating current
C_0	Initial capacitance @ 0 V_{DC}, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{eff,typ}$	Typical effective capacitance @ V_{op}, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{nom,typ}$	Typical nominal capacitance @ V_{op}, quasistatic, +25 °C. See glossary for definition of the nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I_{op}	Operating ripple current, root mean square value of sinusoidal AC current
LP	Low profile
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R_{ins}	Insulation resistance @ $V_{pk,max}$, measurement time t = 7 s, +25 °C
$R_{ins,typ}$	Insulation resistance @ V_{op}, measurement time t > 240 s, +25 °C
SAC	Tin silver copper alloy; lead-free solder paste
T_{amb}	Ambient temperature
tanδ	Dissipation factor @ 0 V DC, 0.5 V AC (RMS),1 kHz, +25 °C
T_{device}	Device temperature. $T_{device} = T_{amb} + \Delta T$ (ΔT defines the self-heating of the device due to applied current).
T_{max}	Max. device temperature, T_{max} = +150 °C. Reference temperature for reliability tests
V_{op}	Operating voltage at maximum attenuation capability
V_R	Rated voltage for $T_{device} \leq T_{max}$. Depends on the temperature derating conditions defined on page 4 and can be higher than $V_{R,Tmax}$
$V_{R,Tmax}$	Rated voltage for T_{max}. Reference DC voltage for reliability tests
$V_{AC,RMS}$	Root mean square value of sinusoidal AC voltage
$V_{pk,max}$	Maximum peak operating voltage (e.g. voltage overshoots or surge pulses which occur < 5% of total component lifecycle). Not for continuous operation.
ΔT	Increase of temperature during operation

Cautions and warnings

General

- Not for use in resonant circuits, where a voltage of alternating polarity occurs.
- Not for AC applications. Consult our local representative for further details.
- If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.
- Do not use CeraLink components for purposes not identified in our specifications.
- Ensure the suitability of a CeraLink in particular by testing it for reliability during design-in. Always evaluate a CeraLink component under worst-case conditions.
- Pay special attention to the reliability of CeraLink devices intended for use in safety-critical applications (e.g. medical equipment, automotive, spacecraft, nuclear power plant).
- Depending on the individual application, CeraLink components are electrically connected to voltages and currents, which are potentially dangerous for life and health of the operator. Installation and operation of CeraLink must be done only by authorized personnel. Ensure proper and safe connections, couplers, and drivers.
- Caution: CeraLink components are highly efficient charge storing devices. Even when disconnected from a supply, the electrical energy content of a loaded component can be high and is held for a long time. Always ensure a complete discharging of the component (e.g. via a 10 kΩ resistor) before handling. Do not discharge by simple short-circuiting, because of the risk of damaging the ceramic.
- Electrical charges can be generated on disconnected components by varying load or temperature. Caution: Discharge a CeraLink before connecting it to a measuring component/electronics, when this component is not sufficiently voltage proved.

See *Important notes* section for further details.

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the lifetime of CeraLink devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases, the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

Operation

- Use CeraLink only within the specified operating temperature range.
- Use CeraLink only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink can produce audible noise due to its piezoelectric characteristic.
- CeraLink components are mainly designed for encased applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of the manufacturer.

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2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
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