# BLA9H0912L-1200P; BLA9H0912LS-1200P LDMOS avionics power transistor Rev. 1 — 1 November 2018

**AMPLEON** 

Product data sheet

#### **Product profile** 1.

## 1.1 General description

1200 W LDMOS power transistor for avionics applications in the frequency range of 960 MHz to 1215 MHz.

#### **Typical performance** Table 1.

Typical RF performance at  $T_{case} = 25 \,^{\circ}\text{C}$ ;  $t_p = 50 \, \mu\text{s}$ ;  $\delta = 2 \, \%$ ;  $I_{Dq} = 75 \, \text{mA}$ ; in a class-AB demo circuit.

Test signal	f	V <sub>DS</sub>	PL	<b>G</b> p	η <sub>D</sub>
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	1030	50	1200	19	60
pulsed RF at 1 dB compression	960 to 1215	50	>1050	19	57

#### 1.2 Features and benefits

- High efficiency
- Excellent ruggedness
- Designed for avionics band operation
- Excellent thermal stability
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- High flexibility with respect to pulse formats
- Internally matched for ease of use
- For RoHS compliance see the product details on the Ampleon website

## 1.3 Applications

Avionics applications in the frequency range of 960 MHz to 1215 MHz

## 2. Pinning information

Table 2. Pinning

Pin	Description	S	Simplified outline	Graphic symbol
BLA9H09	912L-1200P (SOT539A)			
1	drain1			
2	drain2		1 2	1
3	gate1		5	
4	gate2		3 4	5
5	source	[1]		4 7
				<u>'</u>
				2 sym117
BLA9H09	912LS-1200P (SOT539B)			
1	drain1			
2	drain2		1 2	1
3	gate1		5	
4	gate2		3 4	5
5	source	[1]		4 —
				<b>'</b> ⊢_
				2 sym117

<sup>[1]</sup> Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BLA9H0912L-1200P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A		
BLA9H0912LS-1200P	-	earless flanged balanced ceramic package; 4 leads	SOT539B		

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Min	Max	Unit
$V_{DS}$	drain-source voltage	-	106	V
$V_{GS}$	gate-source voltage	-6	+11	V
T <sub>stg</sub>	storage temperature	-65	+150	°C
Tj	junction temperature [1]	-	225	°C

Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

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## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
$Z_{\text{th(j-mb)}}$	transient thermal impedance from junction	T <sub>case</sub> = 85 °C; P <sub>L</sub> = 600 W		
to mounting base	$t_p = 32 \ \mu s; \ \delta = 2 \ \%$	0.027	K/W	
		$t_p$ = 10 $\mu$ s; $\delta$ = 10 %	0.036	K/W
		$t_p$ = 64 $\mu$ s; $\delta$ = 1 %	0.032	K/W
		$t_p$ = 2.4 ms; $\delta$ = 6.4 %	0.126	K/W

## 6. Characteristics

#### Table 6. DC characteristics

 $T_i = 25 \,^{\circ}$ C, per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_{D} = 4 \text{ mA}$	106	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 400 mA	1.5	2.0	2.5	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	2.8	μΑ
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	60	-	Α
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 11 V; V <sub>DS</sub> = 0 V	-	-	280	nA
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 400 mA	-	3.7	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 14 \text{ A}$	-	0.060	-	Ω

#### Table 7. RF characteristics

Test signal: pulsed RF; f = 1030 MHz;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %; RF performance at  $V_{DS}$  = 50 V;  $I_{Dq}$  = 75 mA;  $T_{case}$  = 25  $^{\circ}$ C; unless otherwise specified, in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
G <sub>p</sub>	power gain	P <sub>L</sub> = 1200 W	17.8	19	-	dB
$\eta_{D}$	drain efficiency	P <sub>L</sub> = 1200 W	57	60	-	%
RLin	input return loss	P <sub>L</sub> = 1200 W	-	-15	-	dB
P <sub>droop(pulse)</sub>	pulse droop power	P <sub>L</sub> = 1200 W	-	0.2	0.5	dB
t <sub>r</sub>	rise time	P <sub>L</sub> = 1200 W	-	6	50	ns
t <sub>f</sub>	fall time	P <sub>L</sub> = 1200 W	-	6	50	ns
P <sub>L(2dB)</sub>	output power at 2 dB gain compression		-	1400	-	W

## 7. Test information

## 7.1 Ruggedness in class-AB operation

The BLA9H0912L-1200P and BLA9H0912LS-1200P are capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions:  $V_{DS}$  = 50 V;  $I_{Dq}$  = 75 mA;  $P_{L}$  = 1200 W;  $t_{p}$  = 50  $\mu$ s;  $\delta$  = 2 %.

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## 7.2 Impedance information

Typical impedance (per section) Table 8.

f	Z <sub>S</sub> [1]	Z <sub>L</sub> [1]
(MHz)	(Ω)	(Ω)
950	0.717 – j1.793	0.965 - j1.305
1000	0.953 – j1.886	1.049 – j1.561
1050	1.091 – j1.910	1.032 – j1.780
1100	1.353 – j0.443	1.291 – j1.952
1150	1.962 – j1.061	1.474 – j2.081
1200	0.837 – j0.936	1.514 – j2.413

[1]  $Z_S$  and  $Z_L$  defined in Figure 1.

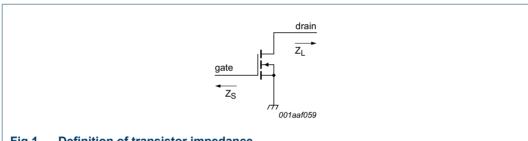


Fig 1. **Definition of transistor impedance** 

## 7.3 Test circuit

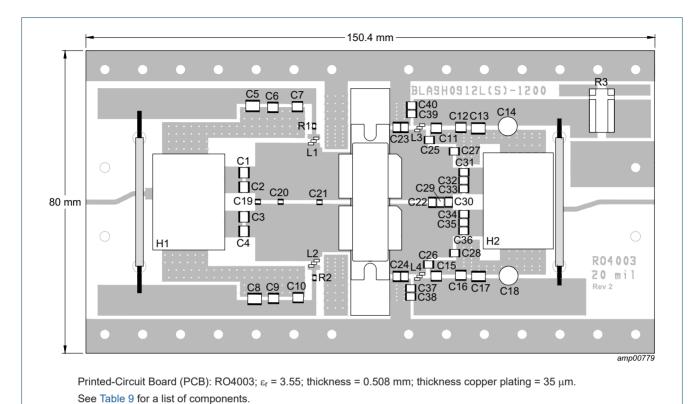


Fig 2. Component layout for application circuit

Table 9. List of components

See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C3, C4	multilayer ceramic chip capacitor	39 pF	ATC 100B
C5, C8, C13, C17	multilayer ceramic chip capacitor	10 μF	Murata: GRM55DR61H106KA88L
C6, C9, C12, C16	multilayer ceramic chip capacitor	1 nF	ATC 100B
C7, C10, C11, C15	multilayer ceramic chip capacitor	51 pF	ATC 100B
C14, C18	electrolytic capacitor	100 μF, 63 V	
C19, C20	multilayer ceramic chip capacitor	0.5 pF	ATC 100A
C21	multilayer ceramic chip capacitor	5.6 pF	ATC 100A
C22	multilayer ceramic chip capacitor	3.0 pF	ATC 100B
C23a, C23b, C24a, C24b	multilayer ceramic chip capacitor	5.1 pF	ATC 800B
C25, C26, C27, C28	multilayer ceramic chip capacitor	2.4 pF	ATC 100B
C29	multilayer ceramic chip capacitor	0.8 pF	ATC 100B
C30	multilayer ceramic chip capacitor	1.6 pF	ATC 100B
C31, C32, C33, C34, C35, C36	multilayer ceramic chip capacitor	43 pF	ATC 100B
C37, C39	multilayer ceramic chip capacitor	20 nF	ATC 200B
C38, C40	multilayer ceramic chip capacitor	1 nF	ATC 200B
H1, H2	balun transformer		Anaren: 3A412S

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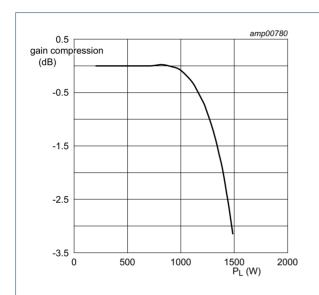
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Table 9. List of components ... continued

See Figure 2 for component layout.

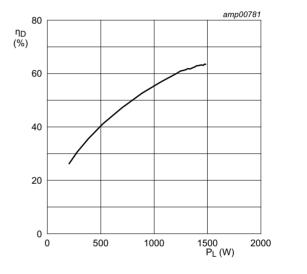
Component	Description	Value	Remarks
L1, L2	inductor	27 nH	Coilcraft: 1111SQ-27NJEB
L3, L4	inductor	1/2 turns, D = 1.5 mm, 8.9 nH	8 mm copper wire
R1, R2	resistor	5 Ω	SMD 0603
R3	resistor	5 mΩ	FC4L110R005FER

## 7.4 Graphical data



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 75 mA;  $t_p$  = 50  $\mu s; \, \delta$  = 2 %.

Fig 3. Gain compression as a function of output power; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 75 mA;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %.

Fig 4. Drain efficiency as a function of output power; typical values

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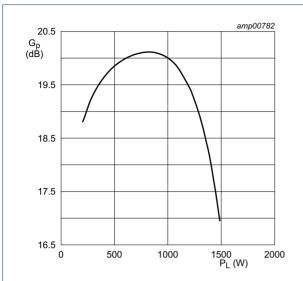
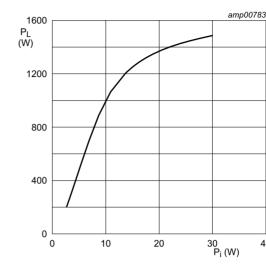


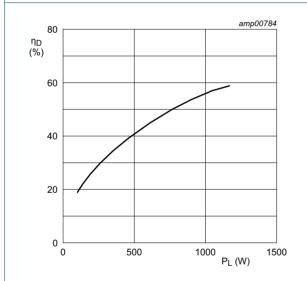
Fig 5. Power gain as a function of output power; typical values

 $V_{DS}$  = 50 V;  $I_{Dq}$  = 75 mA;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %.



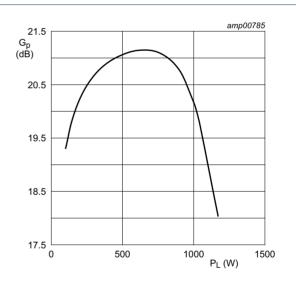
 $V_{DS}$  = 50 V;  $I_{Dq}$  = 75 mA;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %.

Fig 6. Output power as a function of input power; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA;  $t_p$  = 2.4 ms;  $\delta$  = 6.4 %. Fig 7. Drain efficiency as a function of output power;

typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA;  $t_p$  = 2.4 ms;  $\delta$  = 6.4 %.

Fig 8. Power gain as a function of output power; typical values

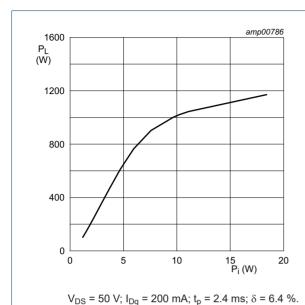
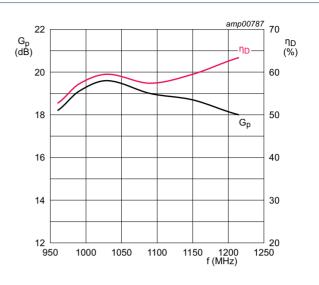


Fig 9. Output power as a function of input power; typical values



 $V_{DS}$  = 51.6 V;  $I_{Dq}$  = 100 mA;  $P_L$  =  $P_{L(1dB)}$  (>1050 W);  $t_p$  = 50  $\mu$ s;  $\delta$  = 5 %. Performance measured in a dedicated broadband

Fig 10. Power gain and drain efficiency as function of frequency; typical values

fixture.

## 8. Package outline

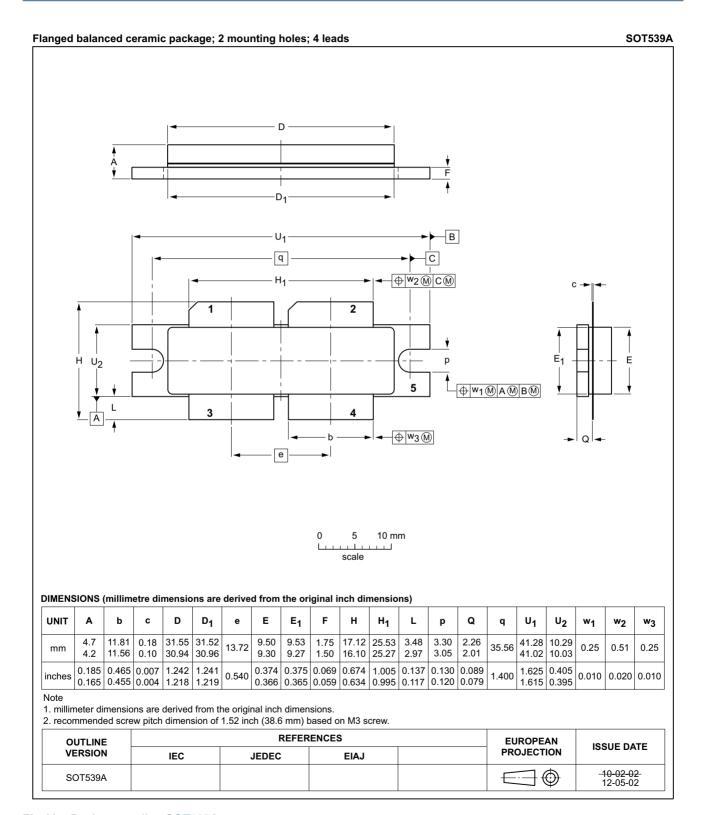


Fig 11. Package outline SOT539A

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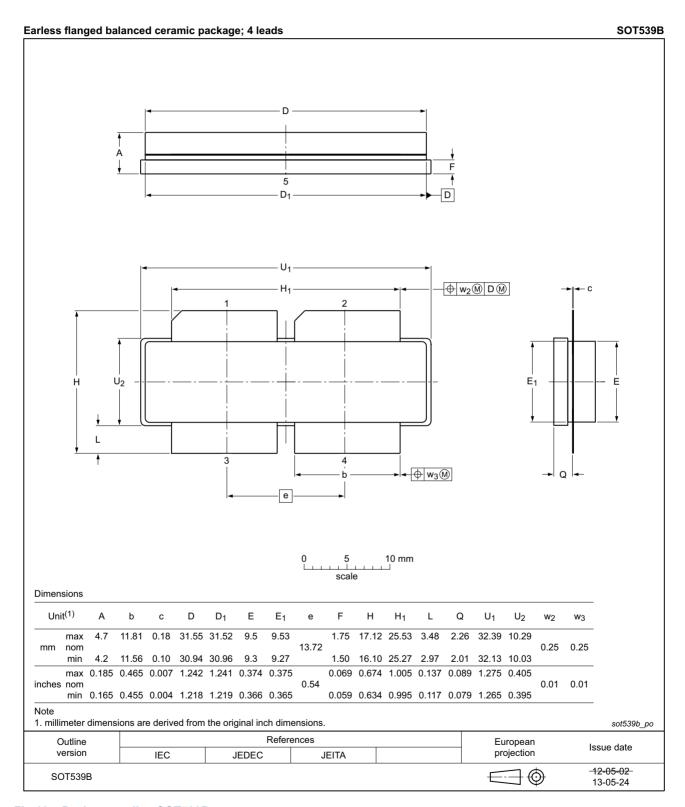


Fig 12. Package outline SOT539B

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## 9. Handling information

#### **CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

- [1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.
- [2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

## 10. Abbreviations

Table 11. Abbreviations

Acronym	Description	
ESD	ElectroStatic Discharge	
LDMOS	aterally Diffused Metal-Oxide Semiconductor	
MTF	Median Time to Failure	
RoHS	Restriction of Hazardous Substances	
SMD	Surface Mounted Device	
VSWR	Voltage Standing Wave Ratio	

## 11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA9H0912L-1200P_LS-1200P v.1	20181101	Product data sheet	-	-

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# **AMPLEON**

# BLA9H0912L(S)-1200P

## **LDMOS** avionics power transistor

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