

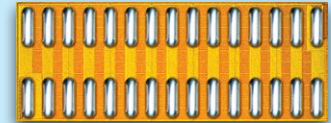
EPC2022 – Enhancement Mode Power Transistor

 V_{DS} , 100 V $R_{DS(on)}$, 3.2 mΩ I_D , 90 A

Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 2.5^\circ\text{C/W}$)	90	A
	Pulsed (25°C, $T_{PULSE} = 300 \mu\text{s}$)	390	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	



Die Size: 6.05 x 2.3 mm

EPC2022 eGaN® FETs are supplied only in passivated die form with solder bumps.

- High Speed DC-DC Conversion
- Motor Drive
- Industrial Automation
- Synchronous Rectification
- Inrush Protection
- Class-D Audio

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.4	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	1.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	42	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 0.9 \text{ mA}$	100			V
I_{DSS}	Drain-Source Leakage	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$		0.1	0.7	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		1	9	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.1	0.7	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 13 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 25 \text{ A}$		2.4	3.2	mΩ
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.8		V

All measurements were done with substrate connected to source.

Dynamic Characteristics[#] ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		1400	1690	pF
C_{OSS}	Output Capacitance			840	1260	
C_{RSS}	Reverse Transfer Capacitance			7		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		1090		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1410		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 25\text{ A}$		13	16	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 50\text{ V}, I_D = 25\text{ A}$		3.4		
Q_{GD}	Gate-to-Drain Charge			2.4		
$Q_{G(TH)}$	Gate Charge at Threshold			2.1		
Q_{OSS}	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		71	107	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.

[#] Defined by design. Not subject to production test.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

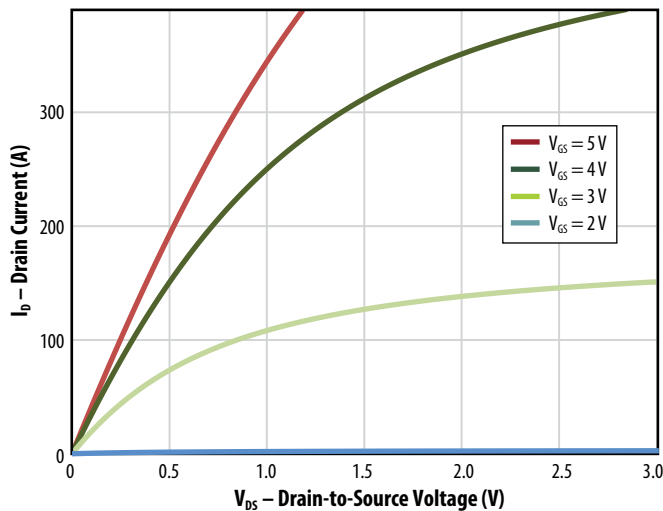
Figure 1: Typical Output Characteristics at 25°C 

Figure 2: Typical Transfer Characteristics

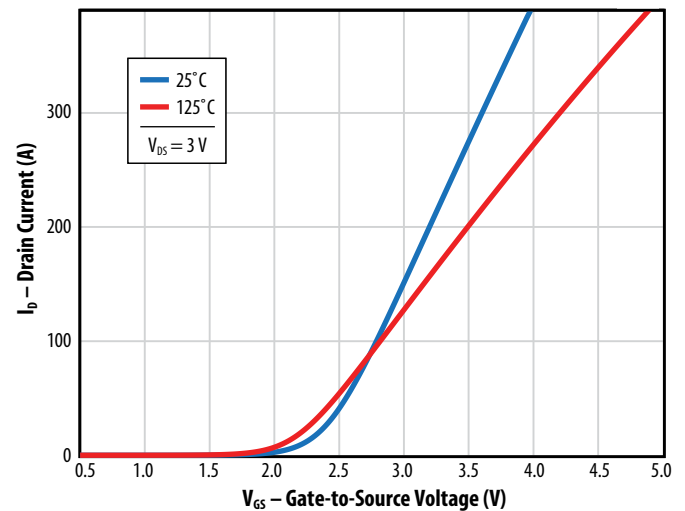
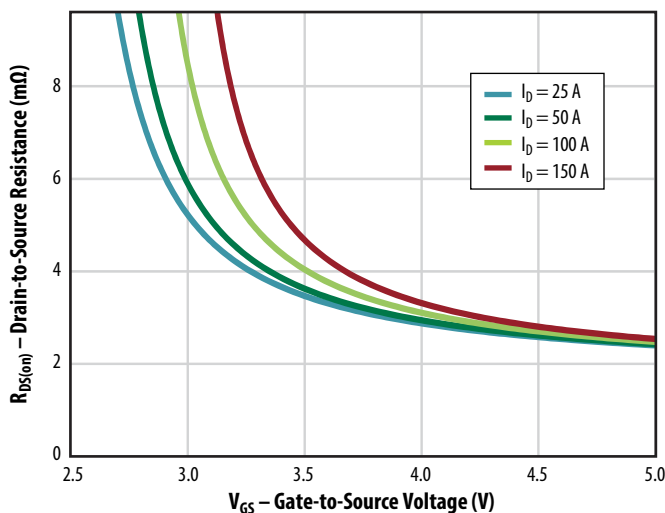
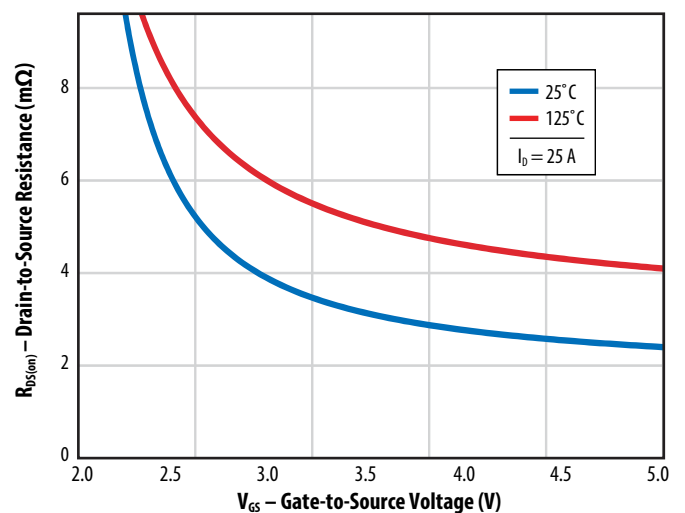
Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

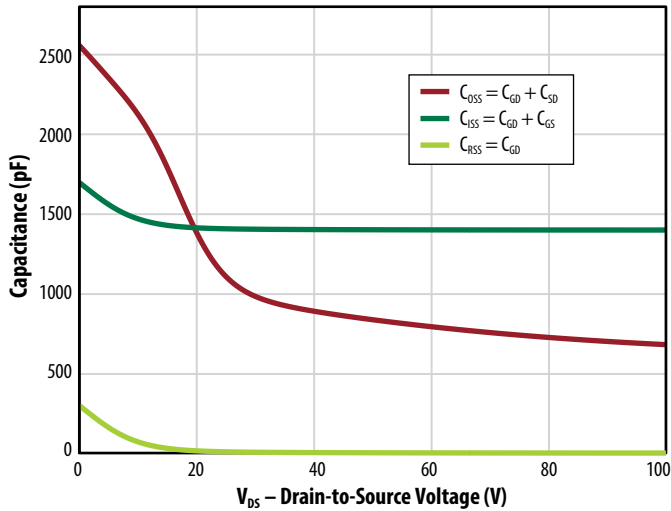


Figure 5b: Typical Capacitance (Log Scale)

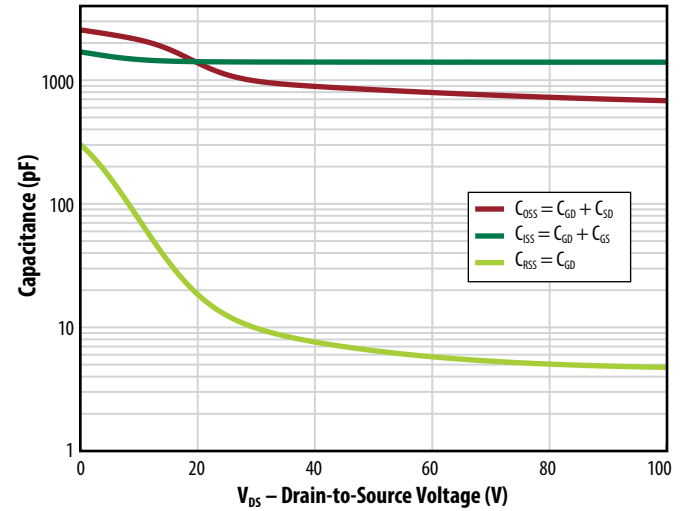


Figure 6: Typical Gate Charge

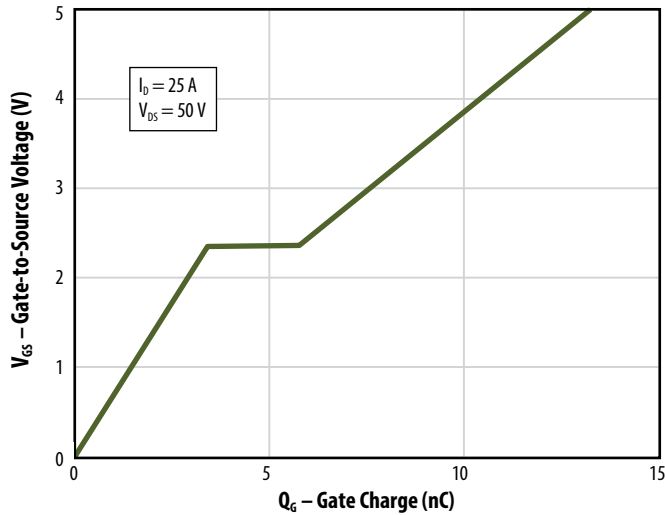


Figure 7: Typical Reverse Drain-Source Characteristics

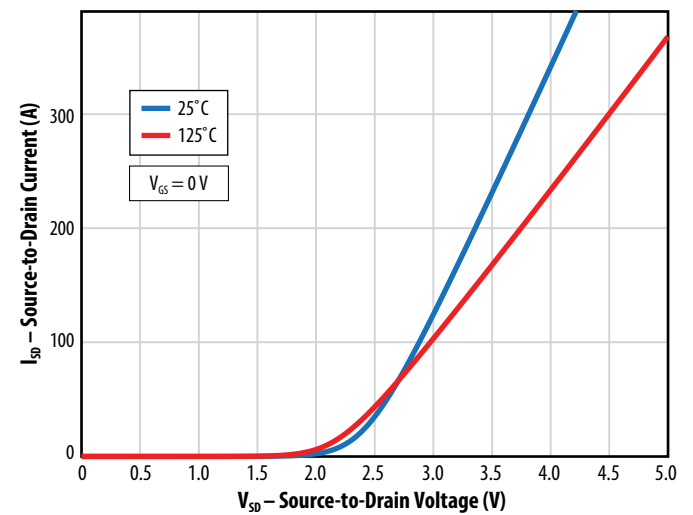


Figure 8: Normalized On-State Resistance vs. Temperature

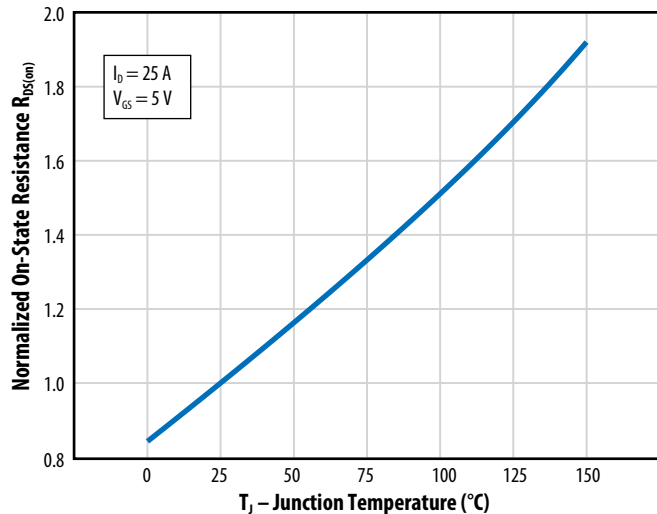
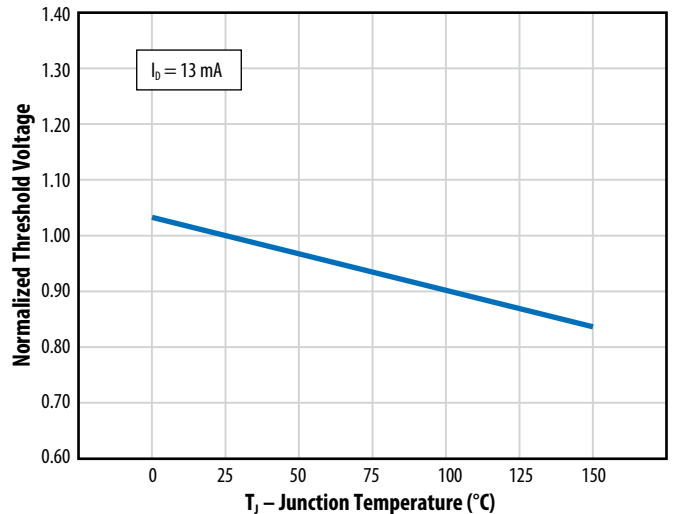


Figure 9: Normalized Threshold Voltage vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 10: Gate Leakage Current

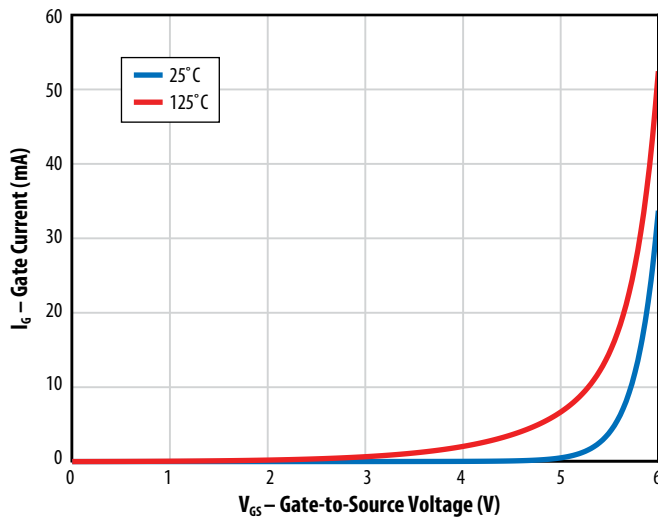


Figure 11: Safe Operating Area

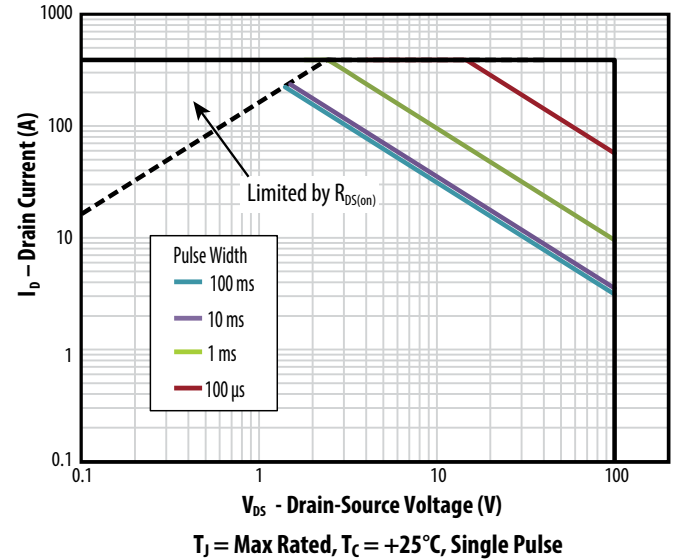
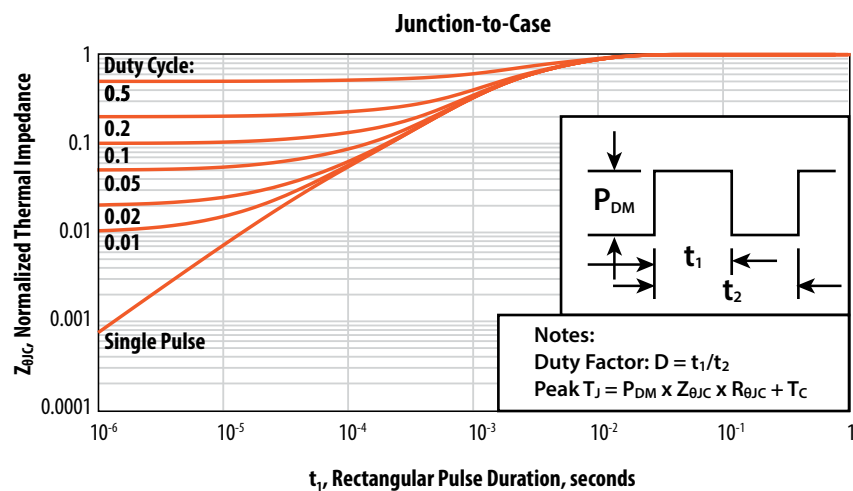
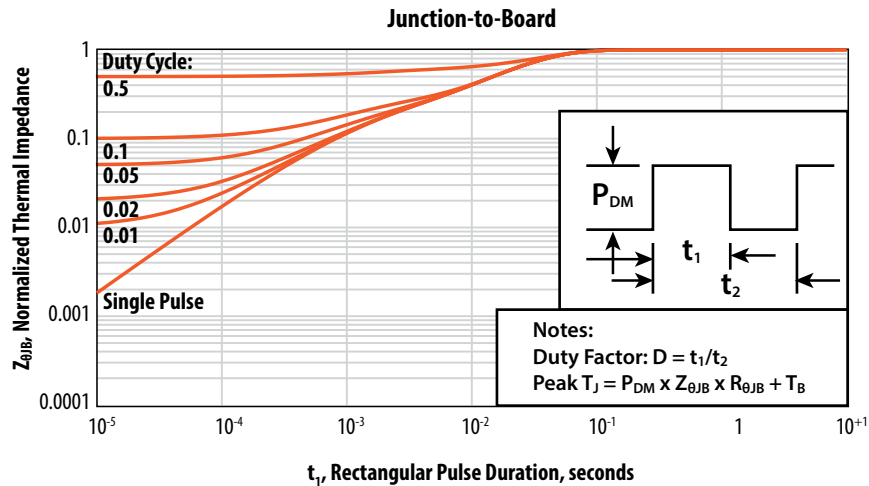


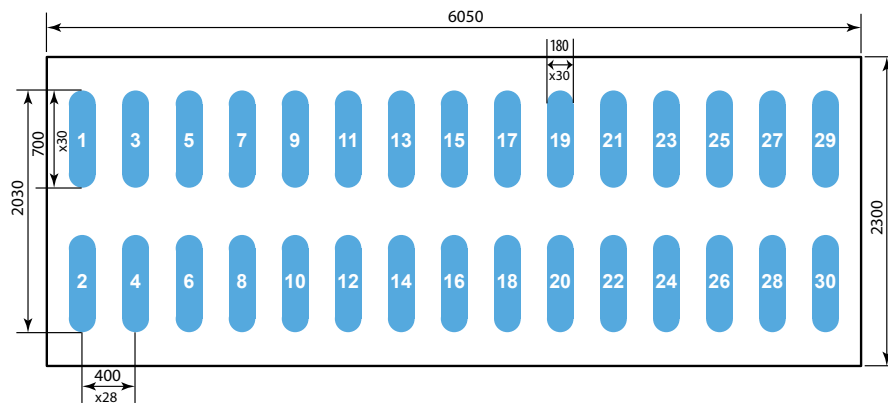
Figure 12: Transient Thermal Response Curves



8 mm pitch, 12 mm wide tape on 7" reel

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

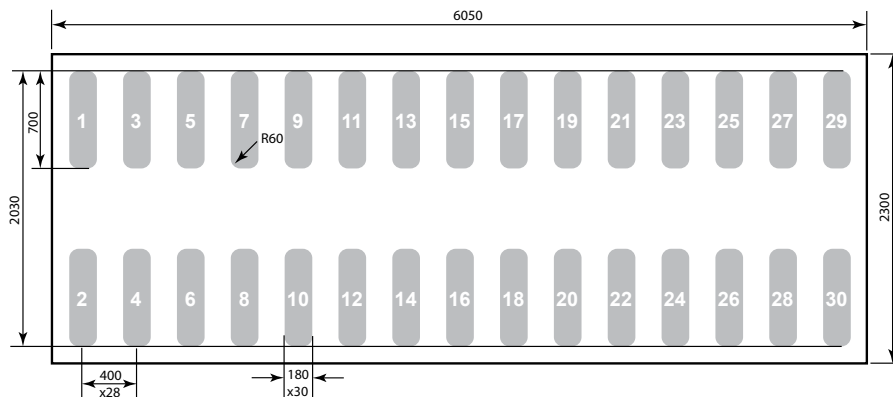
(units in μm)



Pads 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22,
25, 26, 29 are Source;
Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23,
24, 27, 28 are Drain;
Pad 30 is Substrate.*

*Substrate pin should be connected to Source

(units in μm)



Additional assembly resources available at
<https://epc-co.com/epc/design-support/assemblybasics>

Information subject to
change without notice.
Revised June 2023