

DDR4 SDRAM SODIMM

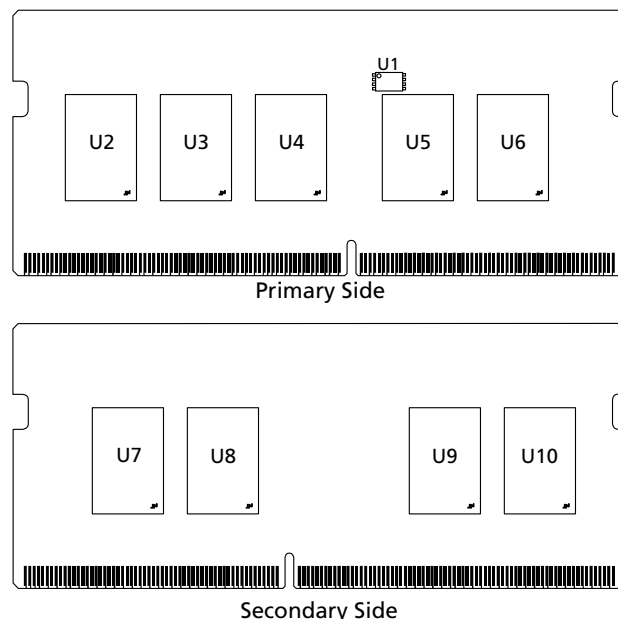
Addendum

MTA9ASF2G72HZ – 16GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 260-pin, small-outline dual in-line memory module (SODIMM)
- Fast data transfer rate: PC4-3200
- 16GB (2 Gig x 72)
- $V_{DD} = 1.20V$ (NOM)
- $V_{PP} = 2.5V$ (NOM)
- $V_{DDSPD} = 2.5V$ (NOM)
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- Single-rank
- On-board I²C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 260-Pin SODIMM (R/C D2)



Options

- Operating temperature
 - Commercial (0°C ≤ T_{OPER} ≤ 95°C)
- Package
 - 260-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)

Marking

None

Z

-3G2

Table 1: Addressing

Parameter	16GB
Row address	128K A[16:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (2 Gig x 8), 16 banks
Module rank address	CS0_n



16GB (x72, ECC, SR) 260-Pin DDR4 SODIMM Features

Table 2: Part Numbers and Timing Parameters – 16GB Modules

Base device: MT40A2G8,¹ 16Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL- ⁿ RCD- ⁿ RP)
MTA9ASF2G72HZ-3G2__	16GB	2 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22

Notes: 1. The data sheet for the base device can be found at micron.com.

2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA9ASF2G72HZ-3G2F1.



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DQ Map

Table 3: Component-to-Module DQ Map (PCB 2450, 2974, 3219, 3239)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	3	21	U3	0	19	63
	1	0	8		1	17	49
	2	2	20		2	18	62
	3	1	7		3	16	50
	4	6	16		4	22	58
	5	4	4		5	21	45
	6	7	17		6	23	59
	7	5	3		7	20	46
U4	0	CB7	104	U5	0	38	183
	1	CB4	88		1	36	170
	2	CB6	100		2	39	182
	3	CB5	87		3	37	169
	4	CB3	105		4	35	186
	5	CB1	91		5	32	174
	6	CB2	104		6	34	187
	7	CB0	92		7	33	173
U6	0	55	225	U7	0	56	237
	1	52	211		1	58	249
	2	54	224		2	57	236
	3	53	212		3	59	250
	4	50	228		4	61	233
	5	49	215		5	62	245
	6	51	229		6	60	232
	7	48	216		7	63	246
U8	0	40	195	U9	0	29	67
	1	42	207		1	30	79
	2	41	194		2	28	66
	3	43	208		3	31	80
	4	44	191		4	24	70
	5	47	204		5	26	83
	6	45	190		6	25	71
	7	46	203		7	27	84



16GB (x72, ECC, SR) 260-Pin DDR4 SODIMM DQ Map

Table 3: Component-to-Module DQ Map (PCB 2450, 2974, 3219, 3239) (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U10	0	12	24				
	1	15	37				
	2	13	25				
	3	14	38				
	4	9	29				
	5	10	41				
	6	8	28				
	7	11	42				

I_{DD} Specifications

Table 4: DDR4 I_{DD} Specifications and Conditions – 16GB (Die Revision B)

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	567	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I _{pp} current	I _{PP0}	36	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	666	mA
Precharge standby current	I _{DD2N}	468	mA
Precharge standby ODT current	I _{DD2NT}	504	mA
Precharge power-down current	I _{DD2P}	387	mA
Precharge quiet standby current	I _{DD2Q}	423	mA
Active standby current	I _{DD3N}	720	mA
Active standby I _{pp} current	I _{PP3N}	27	mA
Active power-down current	I _{DD3P}	621	mA
Burst read current	I _{DD4R}	1818	mA
Burst write current	I _{DD4W}	1647	mA
Distributed refresh current (1x REF)	I _{DD5R}	729	mA
Distributed refresh I _{pp} current (1x REF)	I _{PP5R}	45	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N}	666	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E}	1161	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R}	234	mA
Auto self refresh current (25°C)	I _{DD6A}	135	mA
Auto self refresh current (45°C)	I _{DD6A}	234	mA
Auto self refresh current (75°C)	I _{DD6A}	657	mA
Auto self refresh current (95°C)	I _{DD6A}	1161	mA
Auto self refresh I _{pp} current	I _{PP6X}	81	mA
Bank interleave read current	I _{DD7}	1764	mA
Bank interleave read I _{pp} current	I _{PP7}	90	mA
Maximum power-down current	I _{DD8}	360	mA



16GB (x72, ECC, SR) 260-Pin DDR4 SODIMM I_{DD} Specifications

Table 5: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 8GB (Die Revision F)

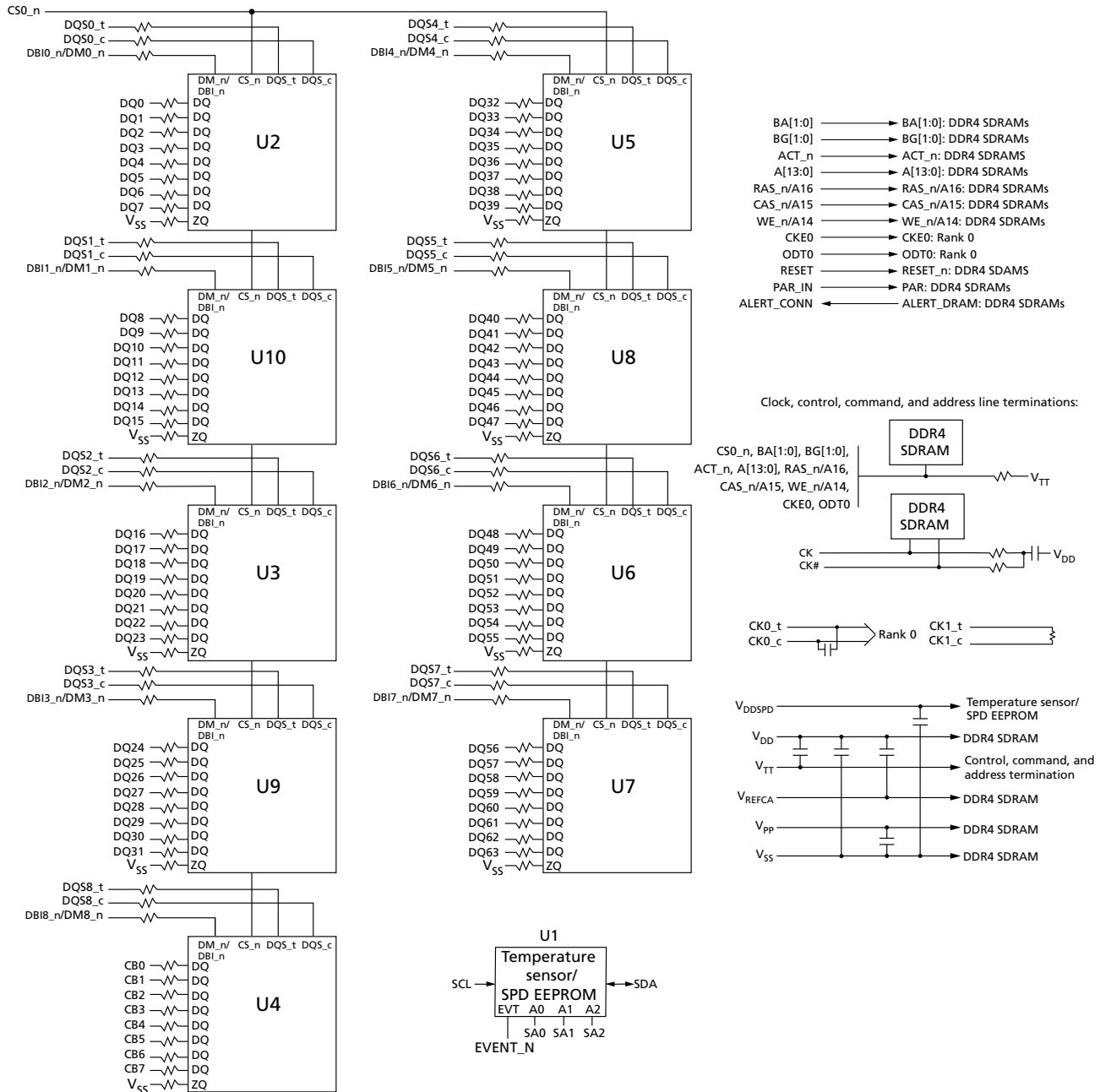
Values are for the MT40A1G16 DDR4 SDRAM only and are computed from values specified in the 16Gb (1 Gig x 16) component data sheet

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0}	540	mA
One bank ACTIVATE-PRECHARGE, Word Line Boost, I _{pp} current	I _{PP0}	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1}	639	mA
Precharge standby current	I _{DD2N}	405	mA
Precharge standby ODT current	I _{DD2NT}	459	mA
Precharge power-down current	I _{DD2P}	342	mA
Precharge quiet standby current	I _{DD2Q}	378	mA
Active standby current	I _{DD3N}	549	mA
Active standby I _{pp} current	I _{PP3N}	18	mA
Active power-down current	I _{DD3P}	450	mA
Burst read current	I _{DD4R}	1260	mA
Burst write current	I _{DD4W}	1008	mA
Burst refresh current (1x REF)	I _{DD5R}	612	mA
Burst refresh I _{pp} current (1x REF)	I _{PP5R}	36	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N}	477	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E}	810	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R}	180	mA
Auto self refresh current (25°C)	I _{DD6A}	99	mA
Auto self refresh current (45°C)	I _{DD6A}	180	mA
Auto self refresh current (75°C)	I _{DD6A}	459	mA
Auto self refresh current (95°C)	I _{DD6A}	810	mA
Auto self refresh I _{pp} current	I _{PP6X}	54	mA
Bank interleave read current	I _{DD7}	1503	mA
Bank interleave read I _{pp} current	I _{PP7}	72	mA
Maximum power-down current	I _{DD8}	324	mA

Notes: 1. When T_C > 85°C, the I_{DD} and I_{pp} values must be derated. Refer to the base device data sheet I_{DD} and I_{pp} specification tables for derating values for the applicable die-revision.

Functional Block Diagram

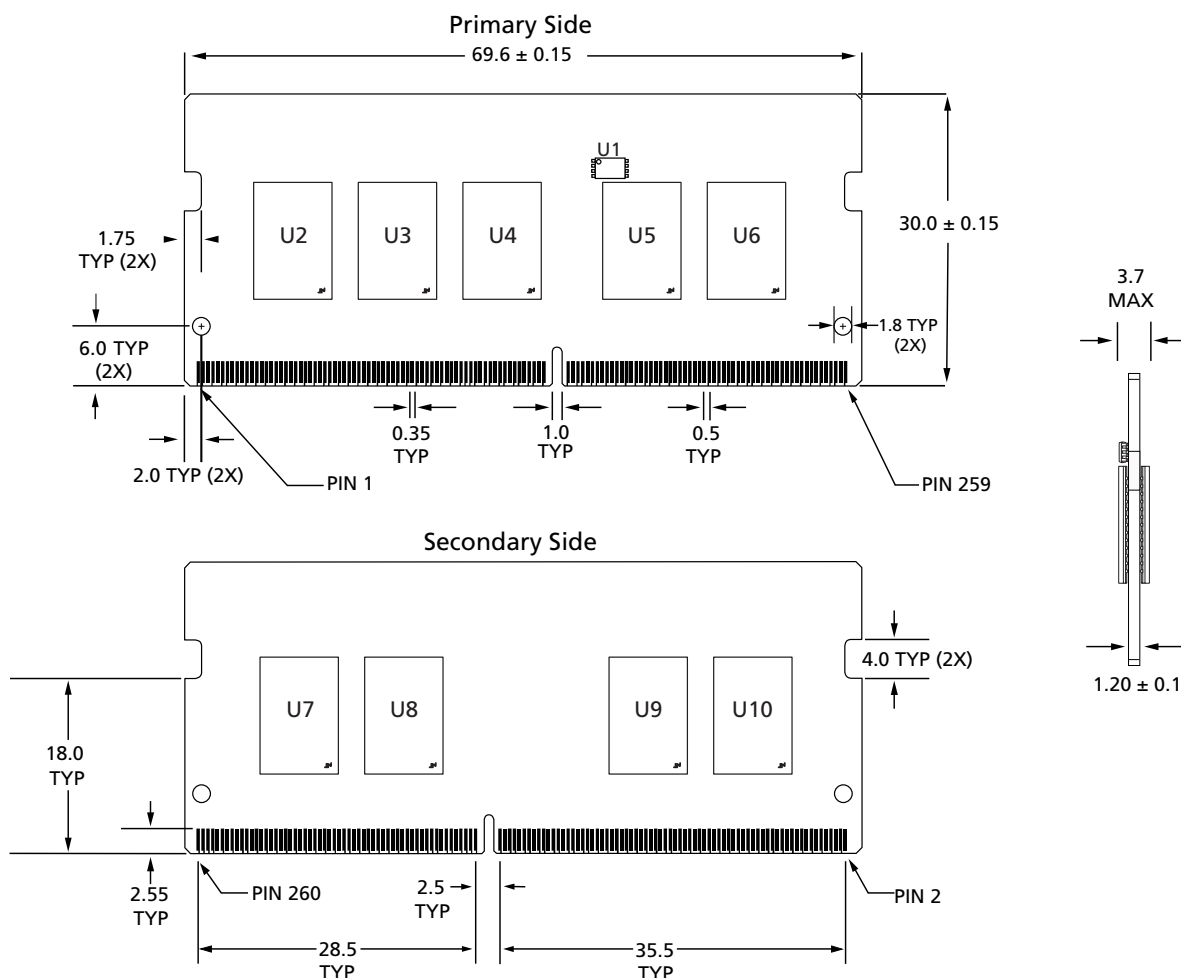
Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Module Dimensions

Figure 3: 260 Pin DDR4 SODIMM - PCB 3233 (R/C D2)



- Notes: 1. All dimensions are in millimeters; MAX/MIN or typical (TYP) where noted.
 2. Tolerances for all dimensions ± 0.15 mm unless otherwise specified.
 3. The dimensional diagram is for reference only.

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