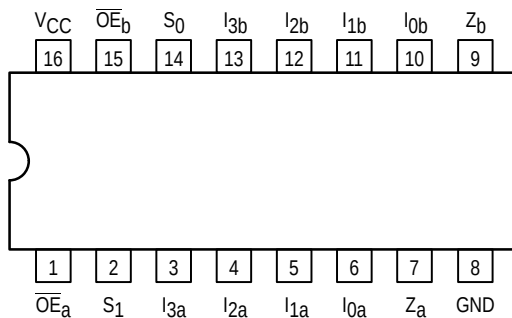




DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC54/74F253 is a Dual 4-Input Multiplexer with 3-State Outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high-impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus-oriented systems.

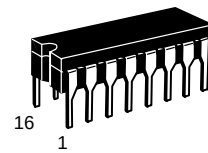
CONNECTION DIAGRAM DIP (TOP VIEW)



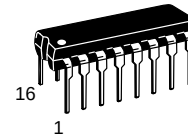
MC54/74F253

**DUAL 4-INPUT MULTIPLEXER
WITH 3-STATE OUTPUTS**

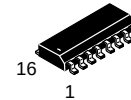
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08



D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

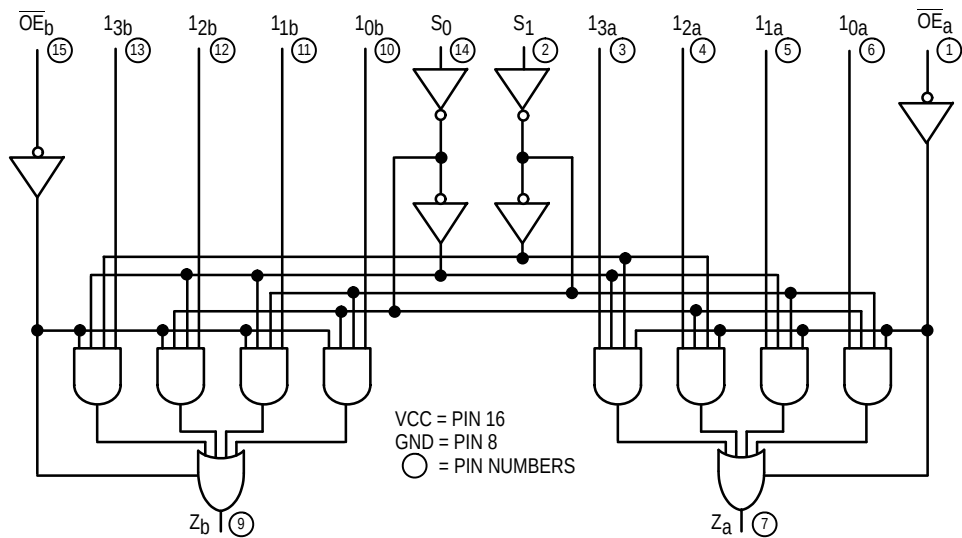
MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

MC54/74F253

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The F253 contains two identical 4-input Multiplexers with 3-State Outputs. They select two bits from four sources selected by common Select Inputs (S_0 , S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (high Z) state.

The F253 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

FUNCTION TABLE

Select Inputs		Data Inputs				Output Enable	Output
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance (off)
Address inputs S_0 and S_1 are common to both sections.

MC54/74F253

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4			V	I _{OH} = -3.0 mA	V _{CC} = 4.50 V
		74	2.7			V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage				0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output Off Current — HIGH				50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output Off Current — LOW				-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current				20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
					100	μA	V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CC}	Power Supply Current					mA	OE _n = GND	
	Total, Output HIGH				16		I _O = 4.5 V; S _n , I ₁ - I ₃ = GND	
	Total, Output LOW				23		I _n , S _n , OE _n = GND V _{CC} = MAX	
	Total at HIGH-Z				23		OE _n = 4.5 V, V _{CC} = MAX I _n , S _n = GND	

AC CHARACTERISTICS

Symbol	Parameter	54/74F		54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = -55°C to +125°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t _{PLH}	Propagation Delay	4.5	11.5	3.5	15	4.5	13.5	ns
t _{PHL}	S _n to Z _n	3.0	9.0	2.5	11	3.0	10	
t _{PLH}	Propagation Delay	3.0	7.0	2.5	9.0	3.0	8.0	ns
t _{PHL}	I _n to Z _n	2.5	6.0	2.5	8.0	2.5	7.0	
t _{PZH}	Output Enable Time	3.0	8.0	2.5	10	3.0	9.0	ns
t _{PZL}		3.0	8.0	2.5	10	3.0	9.0	
t _{PHZ}	Output Disable Time	2.0	5.0	2.0	6.5	2.0	6.0	ns
t _{PLZ}		2.0	6.0	2.0	8.0	2.0	7.0	