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April 1st, 2010
Renesas Electronics Corporation

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

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April 1, 2003

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MITSUBISHI MICROCOMPUTERS

3851 Group
(Built-in 16 KB ROM)

✻This data sheet explains the products which have 16 KB ROM.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3851 group is the 8-bit microcomputer based on the 740 family core technology.

The 3851 group is designed for the household products and office automation equipment and includes serial I/O functions, 8-bit timer, A-D converter, and I²C-bus interface.

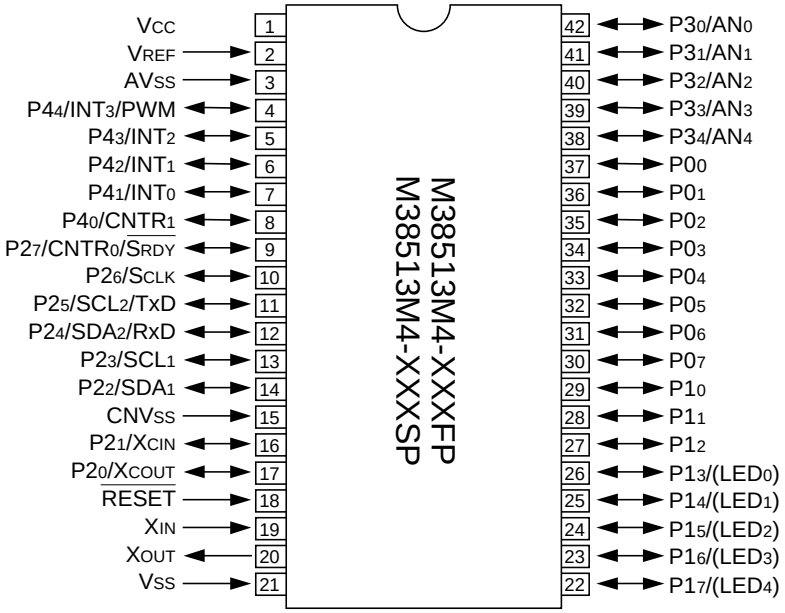
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.5 µs (at 8 MHz oscillation frequency)
- Memory size
  - ROM ..... 16 Kbytes
  - RAM ..... 512 bytes
- Programmable input/output ports 34
- Interrupts ..... 16 sources, 16 vectors
- Timers ..... 8-bit × 4
- Serial I/O ..... 8-bit × 1(UART or Clock-synchronized)
- Multi-master I²C-bus interface (option) ..... 1 channel
- PWM ..... 8-bit × 1
- A-D converter ..... 10-bit × 5 channels
- Watchdog timer ..... 16-bit × 1
- Clock generating circuit ..... Built-in 2 circuits (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  - In high-speed mode ..... 4.0 to 5.5 V (at 8 MHz oscillation frequency)
  - In high-speed mode ..... 2.7 to 5.5 V (at 4 MHz oscillation frequency)
  - In middle-speed mode ..... 2.7 to 5.5 V (at 8 MHz oscillation frequency)
  - In low-speed mode ..... 2.7 to 5.5 V (at 32 kHz oscillation frequency)
- Power dissipation
  - In high-speed mode ..... 34 mW (at 8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 60 µW (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... –20 to 85°C

APPLICATION

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : FP ..... 42P2R-A/E (42-pin plastic-molded SSOP)
Package type : SP ..... 42P4B (42-pin shrink plastic-molded DIP)

Fig. 1 M38513M4-XXXFP/SP pin configuration

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FUNCTIONAL BLOCK

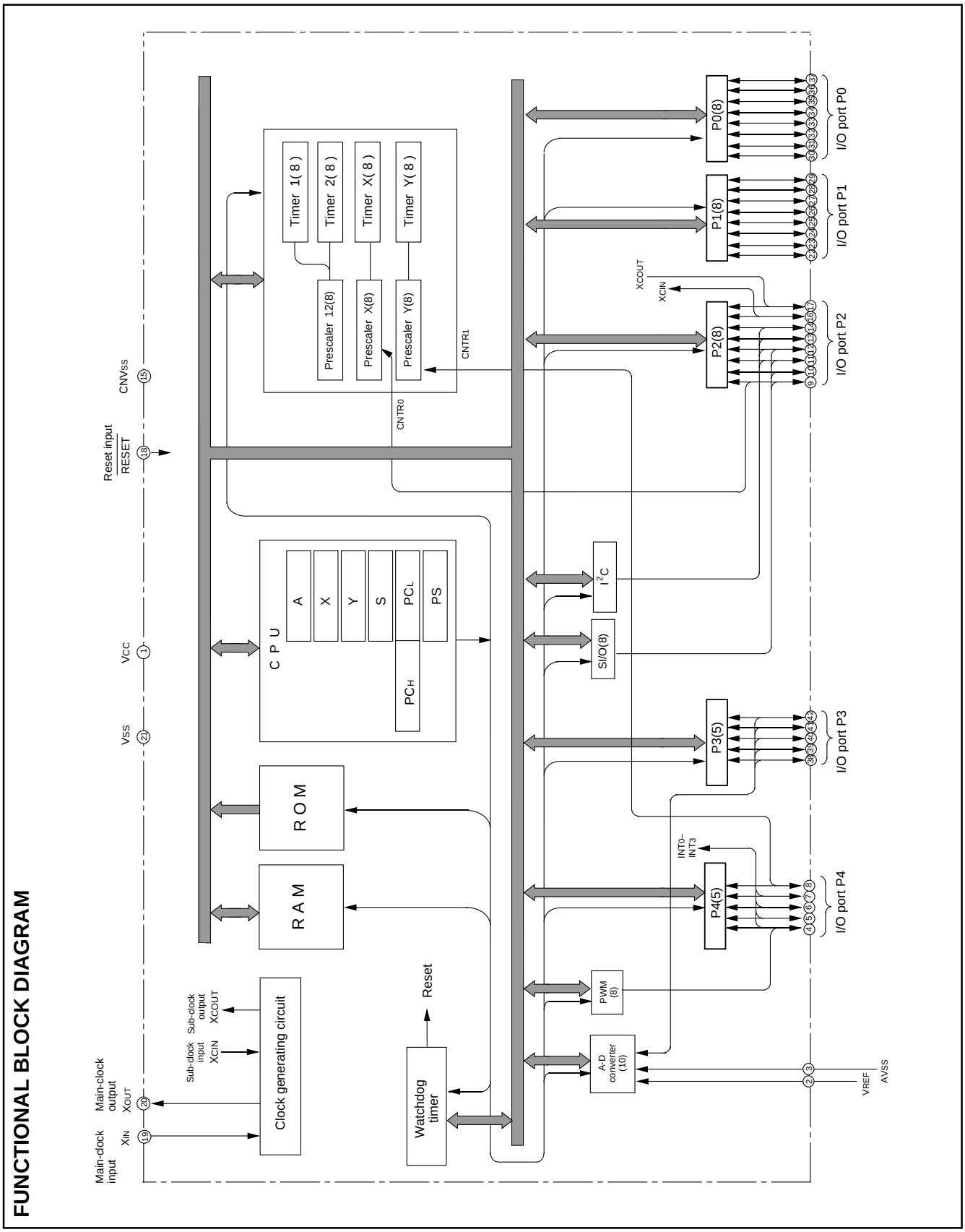


Fig. 2 Functional block diagram

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PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Functions	Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip. •Normally connected to VSS.	
VREF	Reference voltage input	•Reference voltage input pin for A-D converter.	
AVSS	Analog power source input	•Analog power source input pin for A-D converter. •Connect to Vss.	
RESET	Reset input	•Reset input pin for active "L."	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00–P07	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •P13 to P17 (5 bits) are enabled to output large current for LED drive.	
P10–P17	I/O port P1		
P20/XCOUT P21/XCIN	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •P22 to P25 can be switched between CMOS compatible input level or SMBUS input level in the I2C-BUS interface function. •P20, P21, P24 to P27: CMOS3-state output structure. •P24, P25: N-channel open-drain structure in the I2C-BUS interface function. •P22, P23: N-channel open-drain structure.	• Sub-clock generating circuit I/O pins (connect a resonator)
P22/SDA1 P23/SCL1			• I2C-BUS interface function pins
P24/SDA2/RxD P25/SCL2/TxD			• I2C-BUS interface function pin/ Serial I/O function pins
P26/SCLK			• Serial I/O function pin
P27/CNTR0/ SRDY			• Serial I/O function pin/ Timer X function pin
P30/AN0– P34/AN4	I/O port P3	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A-D converter input pin
P40/CNTR1	I/O port P4	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• Timer Y function pin
P41/INT0– P43/INT2			• Interrupt input pins
P44/INT3/PWM			• Interrupt input pin • PWM output pin

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GROUP EXPANSION

Mitsubishi plans to expand the 3851 group as follows:

Memory Type

Support for mask ROM and One Time PROM versions.

Memory Size

ROM/PROM size ..... 16 K bytes
RAM size ..... 512 bytes

Packages

42P2R-A ..... 42-pin plastic molded SSOP
42P4B ..... 42-pin shrink plastic-molded DIP

Memory Expansion Plan

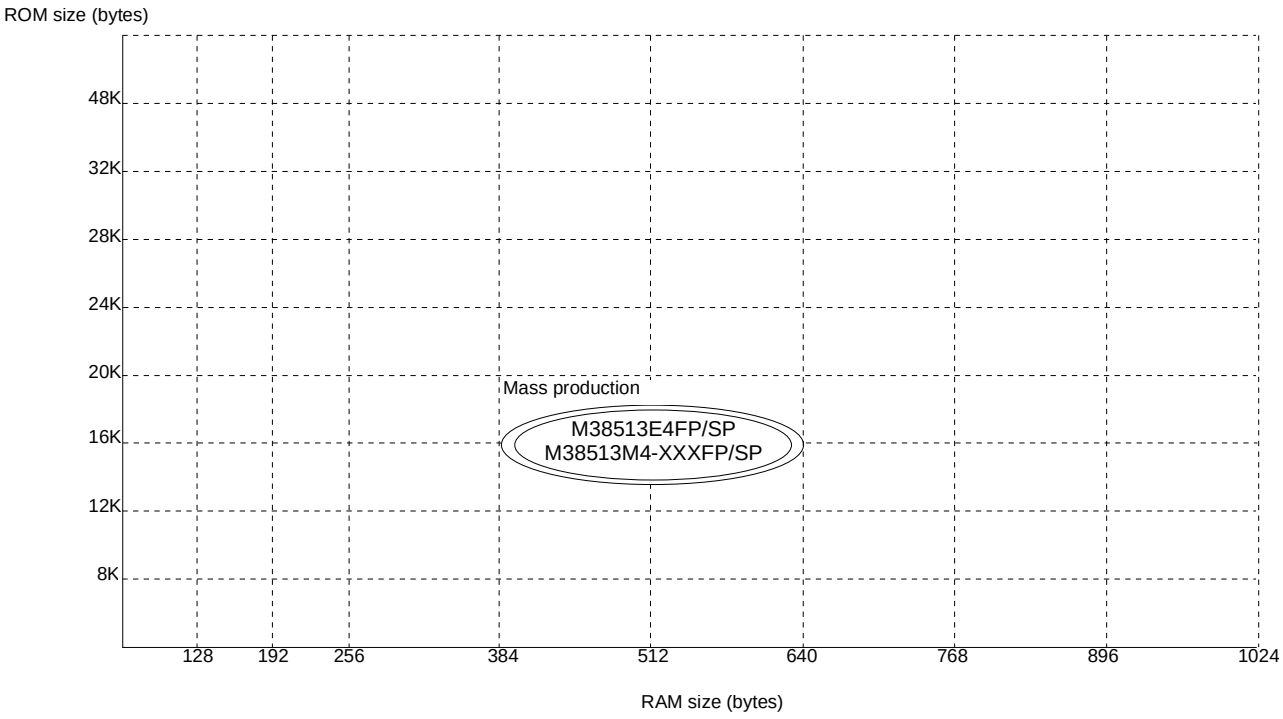


Fig. 3 Memory expansion plan

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FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3851 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc. The CPU mode register is allocated at address 003B16.

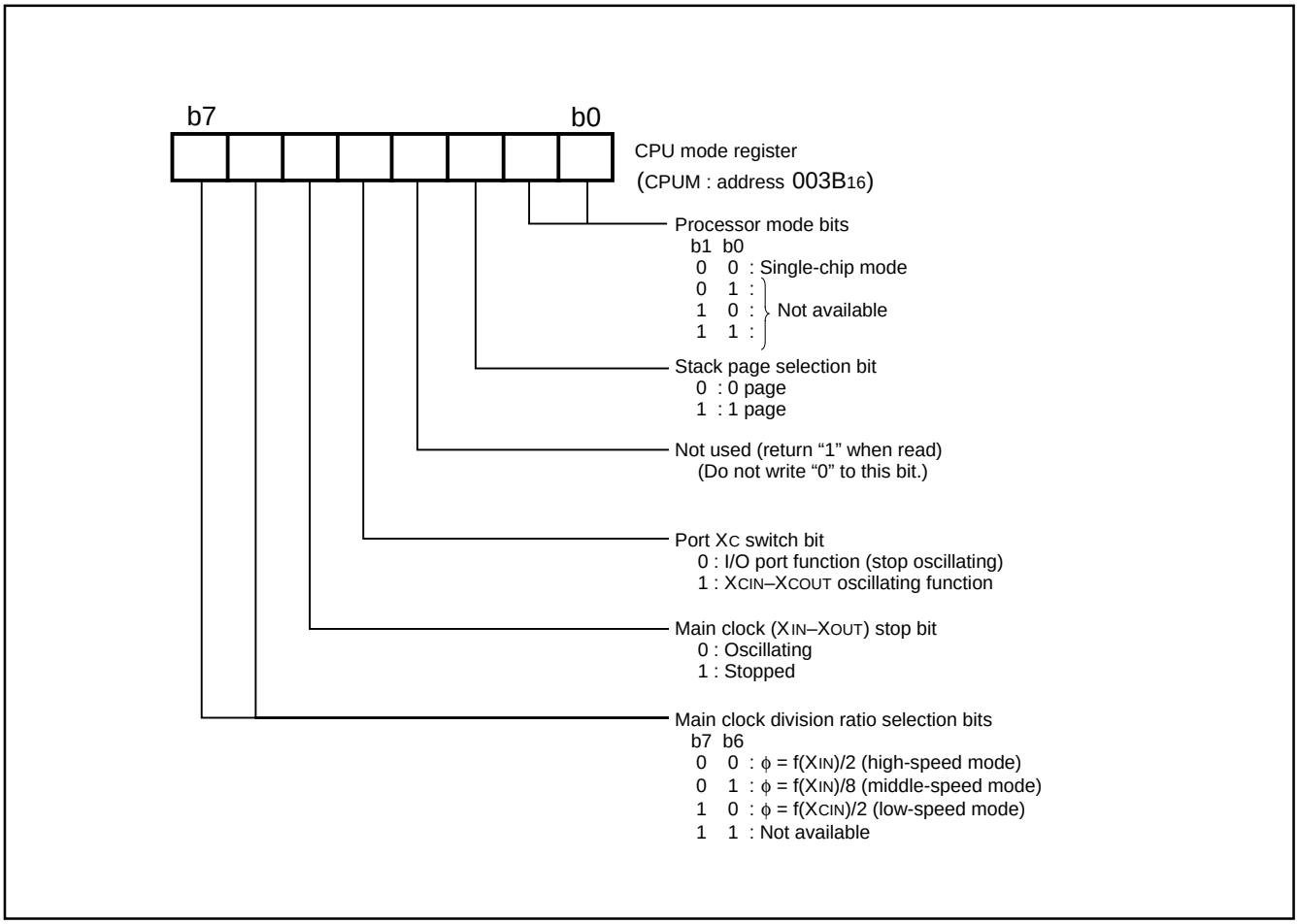


Fig. 4 Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address XXXX16
192	00FF16
256	013F16
384	01BF16
512	023F16
640	02BF16
768	033F16
896	03BF16
1024	043F16
1536	063F16
2048	083F16
3072	0C3F16
4032	0FFF16

ROM area

ROM size (bytes)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016

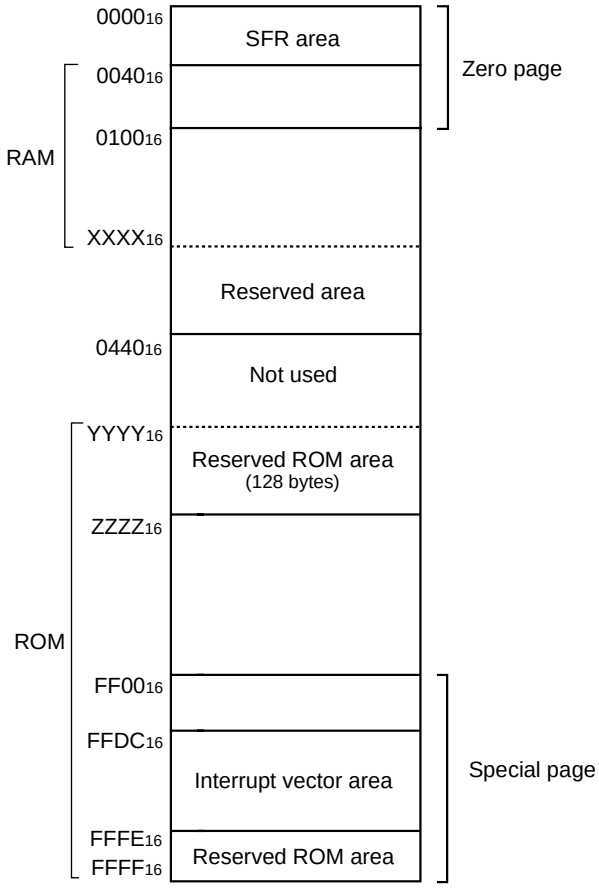


Fig. 5 Memory map diagram

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0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	
$000B_{16}$	
$000C_{16}$	
$000D_{16}$	
$000E_{16}$	
$000F_{16}$	
0010_{16}	
0011_{16}	
0012_{16}	
0013_{16}	
0014_{16}	
0015_{16}	Reserved ✻
0016_{16}	Reserved ✻
0017_{16}	Reserved ✻
0018_{16}	Transmit/Receive buffer register (TB/RB)
0019_{16}	Serial I/O status register (SIOSTS)
$001A_{16}$	Serial I/O control register (SIOCON)
$001B_{16}$	UART control register (UARTCON)
$001C_{16}$	Baud rate generator (BRG)
$001D_{16}$	PWM control register (PWMCON)
$001E_{16}$	PWM prescaler (PREPWM)
$001F_{16}$	PWM register (PWM)

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	Timer count source selection register (TCSS)
0029_{16}	
$002A_{16}$	
$002B_{16}$	I^2C data shift register (S0)
$002C_{16}$	I^2C address register (S0D)
$002D_{16}$	I^2C status register (S1)
$002E_{16}$	I^2C control register (S1D)
$002F_{16}$	I^2C clock control register (S2)
0030_{16}	I^2C start/stop condition control register (S2D)
0031_{16}	Reserved ✻
0032_{16}	
0033_{16}	
0034_{16}	A-D control register (ADCON)
0035_{16}	A-D conversion low-order register (ADL)
0036_{16}	A-D conversion high-order register (ADH)
0037_{16}	
0038_{16}	MISRG
0039_{16}	Watchdog timer control register (WDTCON)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

✻ Reserved : Do not write “1” to this address.

Fig. 6 Memory map of special function register (SFR)

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I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 2 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P00–P07	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output			(1)
P10–P17	Port P1					
P20/XCOUT P21/XCIN	Port P2			Sub-clock generating circuit	CPU mode register	(2) (3)
P22/SDA1 P23/SCL1			CMOS compatible input level CMOS/SMBUS input level (when selecting I2C-BUS interface function) N-channel open-drain output	I2C-BUS interface function I/O	I2C control register	(4) (5)
P24/SDA2/RxD P25/SCL2/TxD			CMOS compatible input level CMOS/SMBUS input level (when selecting I2C-BUS interface function) CMOS 3-state output N-channel open-drain output (when selecting I2C-BUS interface function)	I2C-BUS interface function I/O Serial I/O function I/O	I2C control register Serial I/O control register	(6) (7)
P26/SCLK			CMOS compatible input level CMOS 3-state output	Serial I/O function I/O	Serial I/O control register	(8)
P27/CNTR0/$\overline{\text{SRDY}}$				Serial I/O function I/O Timer X function I/O	Serial I/O control register Timer XY mode register	(9)
P30/AN0— P34/AN4	Port P3			A-D conversion input	A-D control register	(10)
P40/CNTR1	Port P4			Timer Y function I/O	Timer XY mode register	(11)
P41/INT0— P43/INT2				External interrupt input	Interrupt edge selection register	(12)
P44/INT3/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(13)

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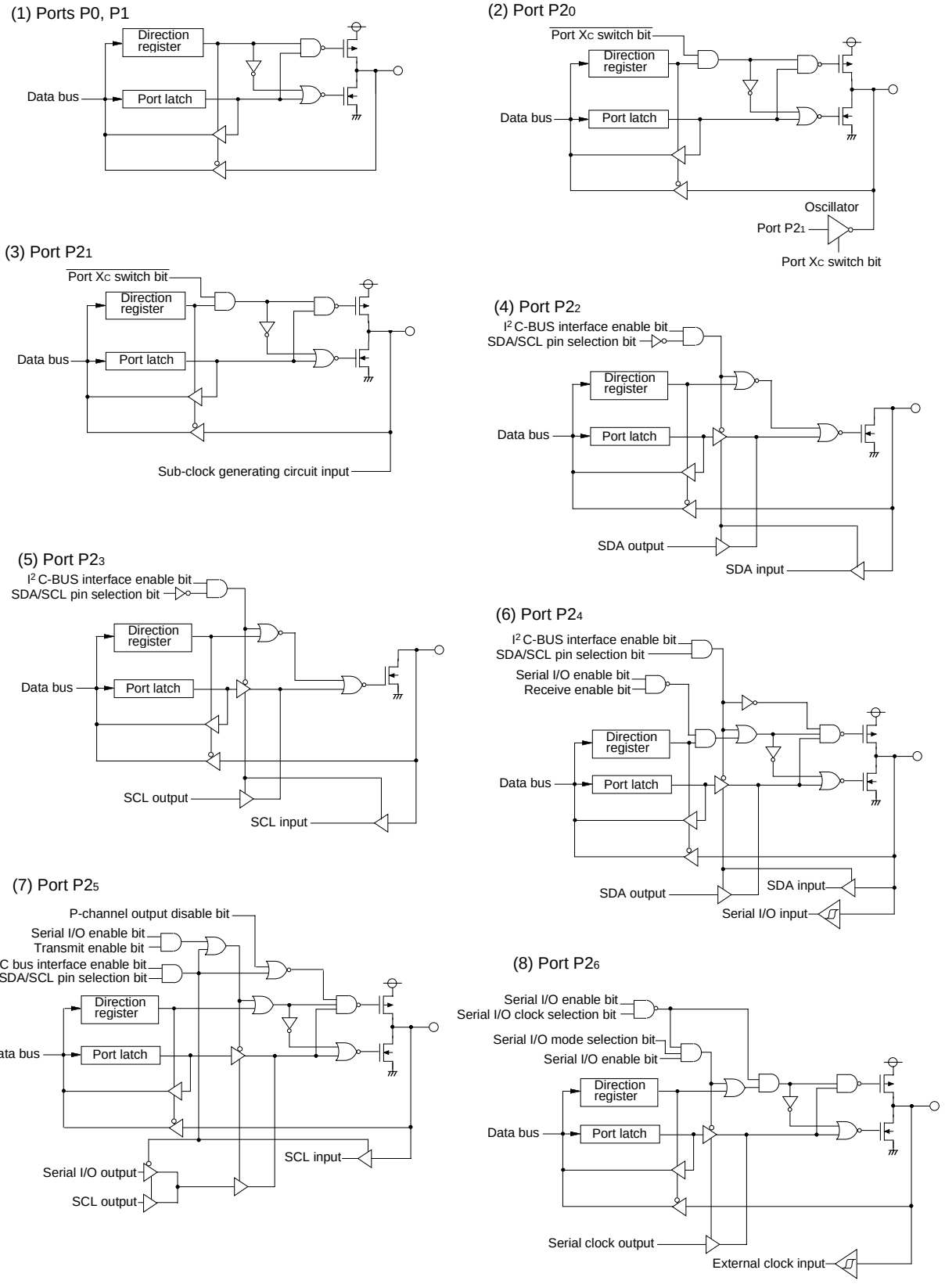
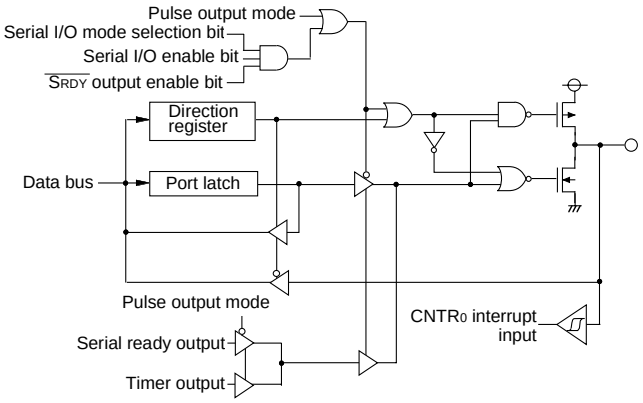


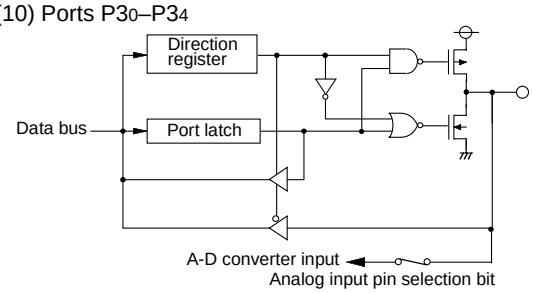
Fig. 7 Port block diagram (1)

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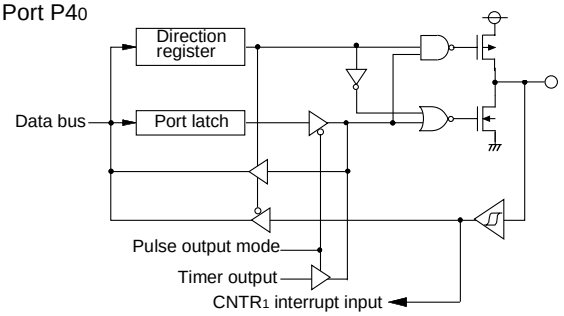
(9) Port P2$_7$



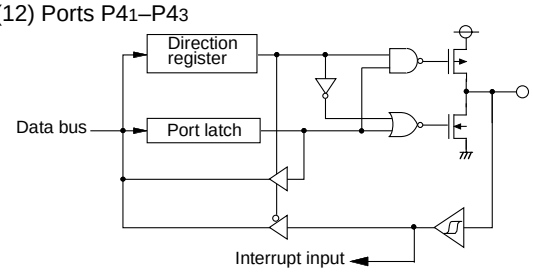
(10) Ports P3$_0$–P3$_4$



(11) Port P4$_0$



(12) Ports P4$_1$–P4$_3$



(13) Port P4$_4$

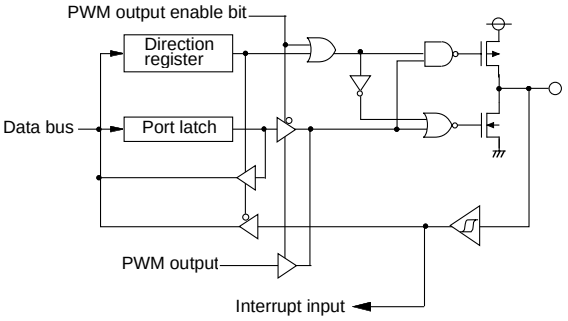


Fig. 8 Port block diagram (2)

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INTERRUPTS

Interrupts occur by 16 sources among 16 sources: seven external, eight internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes

When setting the followings, the interrupt request bit may be set to “1”.

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $3A_{16}$)
Timer XY mode register (address 23_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt edge selection register (address $3A_{16}$)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to “0” (disabled).
②Set the interrupt edge select bit or the interrupt source select bit.
③Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to “1” (enabled).

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Table 3 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
SCL, SDA	3	FFF916	FFF816	At detection of either rising or falling edge of SCL or SDA input	External interrupt (active edge selectable)
INT1	4	FFF716	FFF616	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
INT2	5	FFF516	FFF416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	6	FFF316	FFF216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
I^2C	7	FFF116	FFF016	At completion of data transfer	
Timer X	8	FFEF16	FFEE16	At timer X underflow	
Timer Y	9	FFED16	FFEC16	At timer Y underflow	
Timer 1	10	FFEB16	FFEA16	At timer 1 underflow	STP release timer underflow
Timer 2	11	FFE916	FFE816	At timer 2 underflow	
Serial I/O reception	12	FFE716	FFE616	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O Transmission	13	FFE516	FFE416	At completion of serial I/O transfer shift or when transmission buffer is empty	Valid when serial I/O is selected
CNTR0	14	FFE316	FFE216	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	15	FFE116	FFE016	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
A-D converter	16	FFDF16	FFDE16	At completion of A-D conversion	
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

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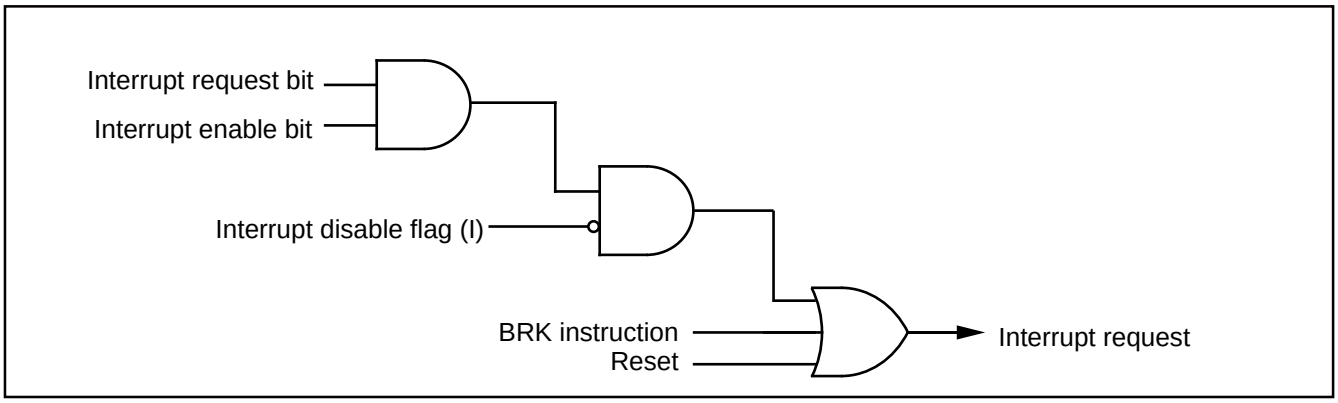


Fig. 9 Interrupt control

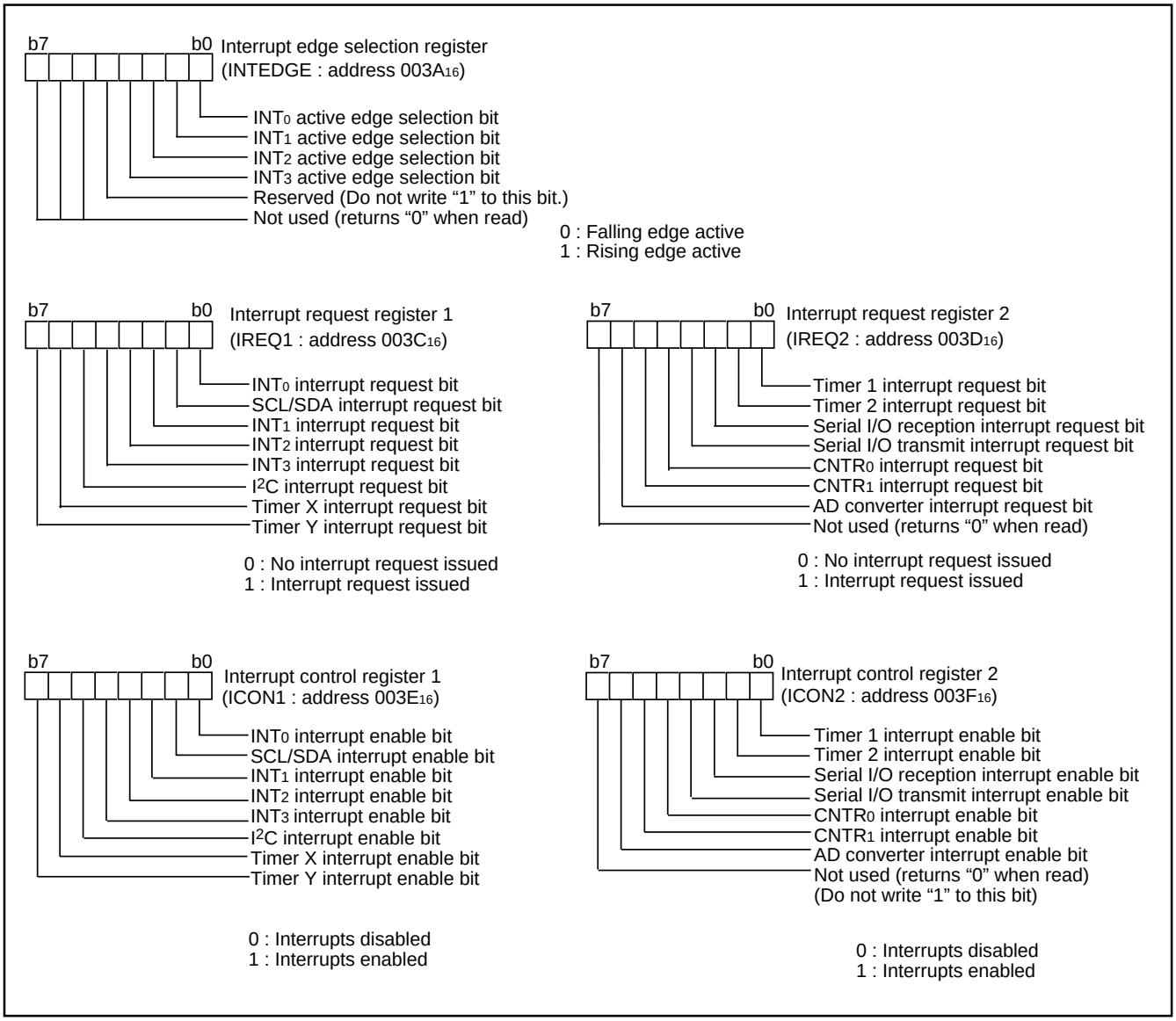


Fig. 10 Structure of interrupt-related registers (1)

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TIMERS

The 3851 group has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are count down. When the timer reaches "00$_{16}$", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

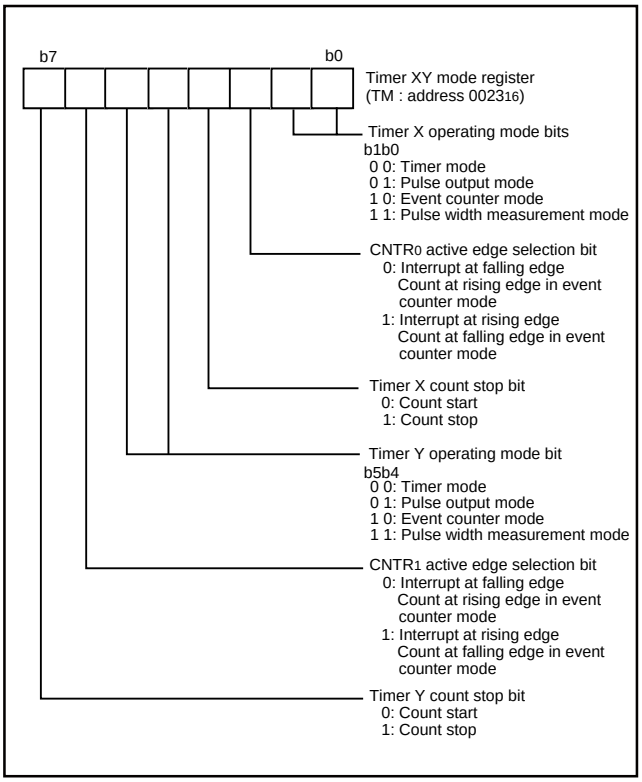


Fig. 11 Structure of timer XY mode register

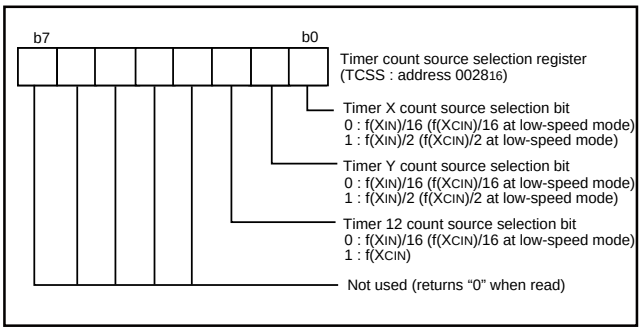


Fig. 12 Structure of timer count source selection register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts the count source selected by Timer count source selection bit.

(2) Pulse Output Mode

The timer counts the count source selected by Timer count source selection bit. Whenever the contents of the timer reach "00$_{16}$", the signal output from the CNTR$_0$ (or CNTR$_1$) pin is inverted. If the CNTR$_0$ (or CNTR$_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port P2$_7$ (or port P4$_0$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the CNTR$_0$ or CNTR$_1$ pin.

When the CNTR$_0$ (or CNTR$_1$) active edge selection bit is "0", the rising edge of the CNTR$_0$ (or CNTR$_1$) pin is counted.

When the CNTR$_0$ (or CNTR$_1$) active edge selection bit is "1", the falling edge of the CNTR$_0$ (or CNTR$_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the CNTR$_0$ (or CNTR$_1$) active edge selection bit is "0", the timer counts the selected signals by the count source selection bit while the CNTR$_0$ (or CNTR$_1$) pin is at "H". If the CNTR$_0$ (or CNTR$_1$) active edge selection bit is "1", the timer counts it while the CNTR$_0$ (or CNTR$_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer overflows.

■Note

When switching the count source by the timer 12, X and Y count source bit, the value of timer count is altered in unconsiderable amount owing to generating of a thin pulses in the count input signals.

Therefore, select the timer count source before set the value to the prescaler and the timer.

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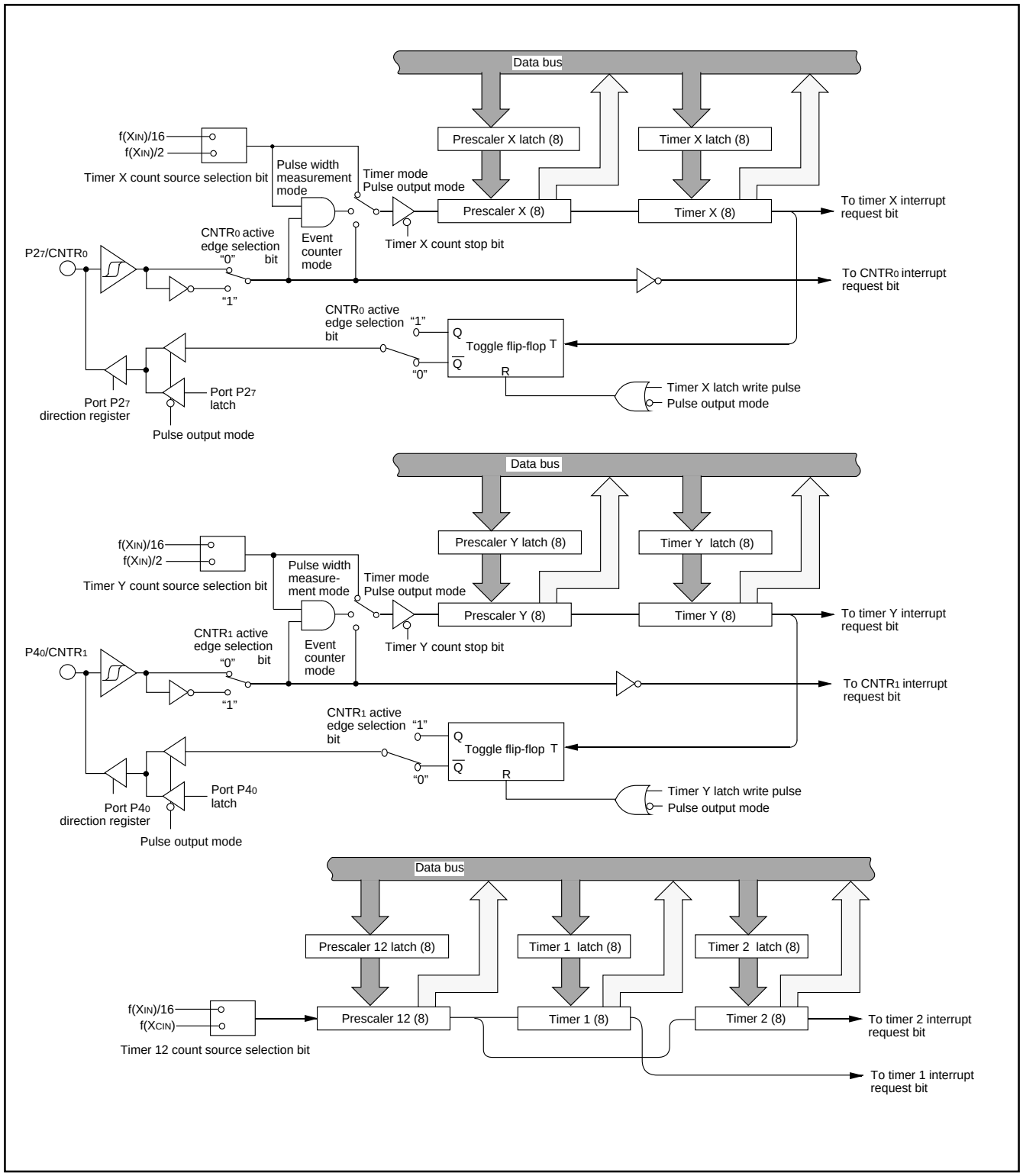


Fig. 13 Block diagram of timer X, timer Y, timer 1, and timer 2

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SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O mode selection bit of the serial I/O control register (bit 6 of address 001A16) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

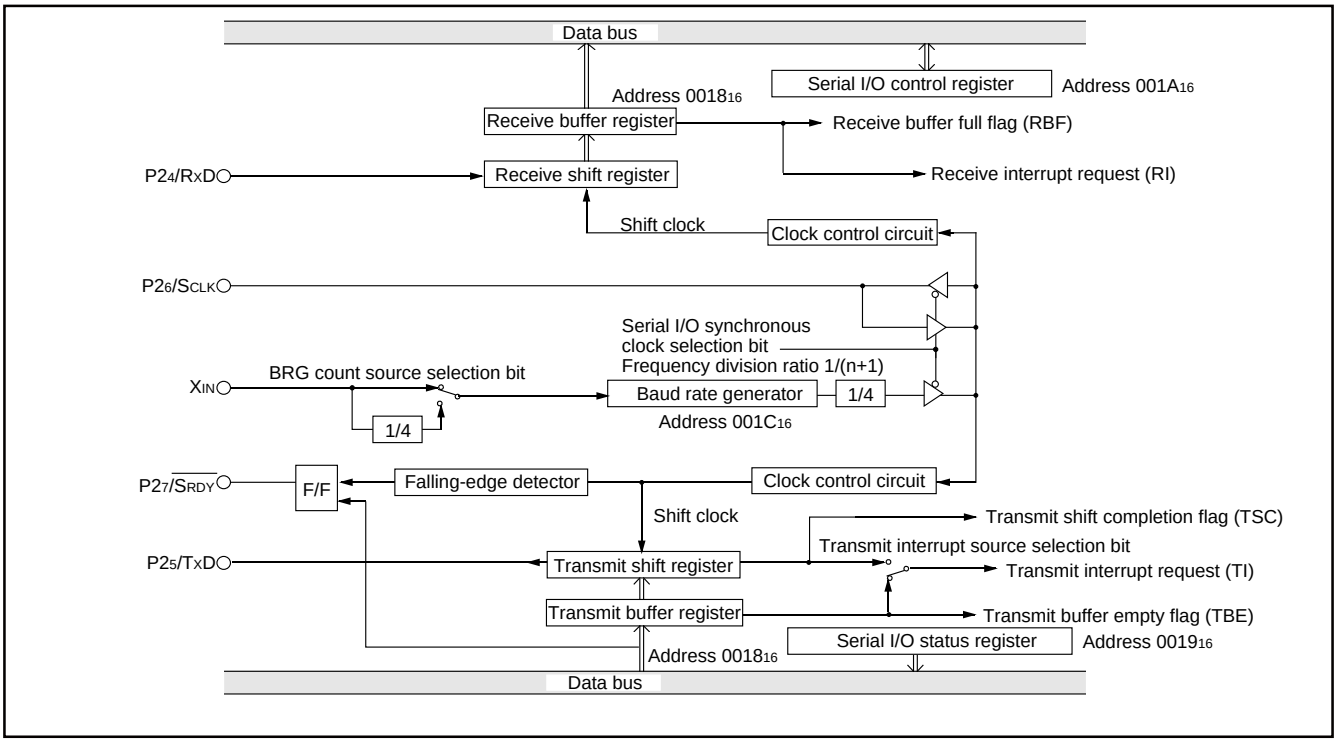
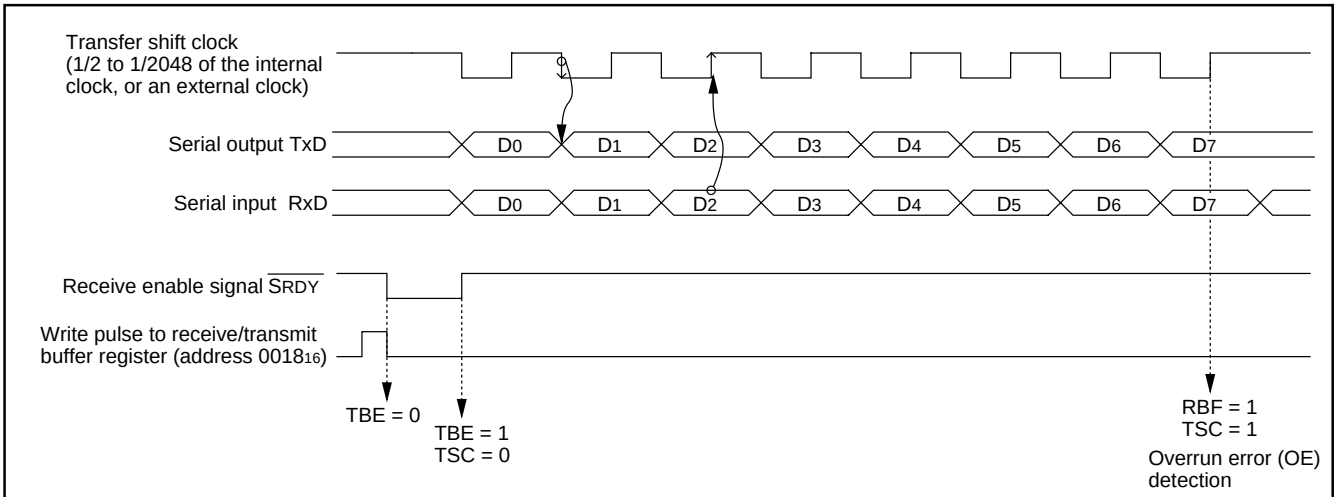


Fig. 14 Block diagram of clock synchronous serial I/O



Notes 1: As the transmit interrupt (TI), either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1" .

Fig. 15 Operation of clock synchronous serial I/O function

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(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit (b6) of the serial I/O control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

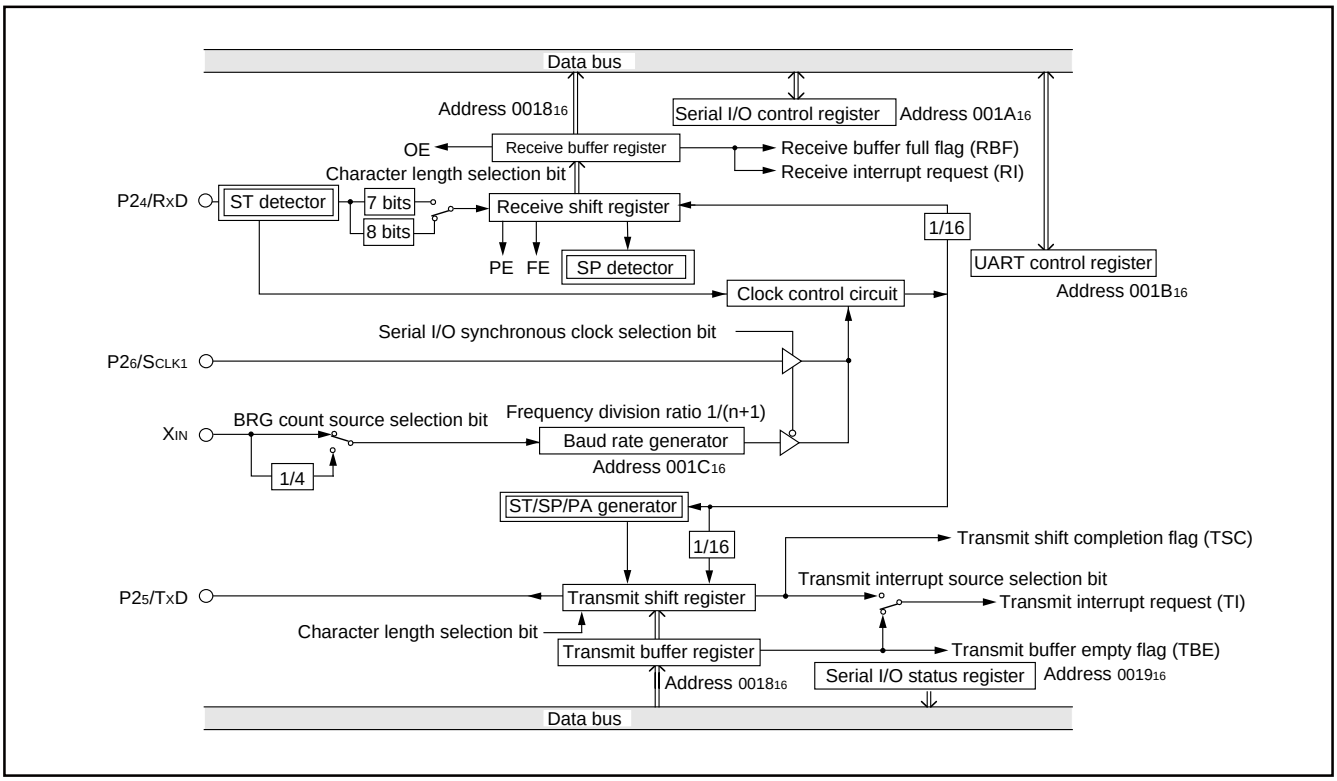
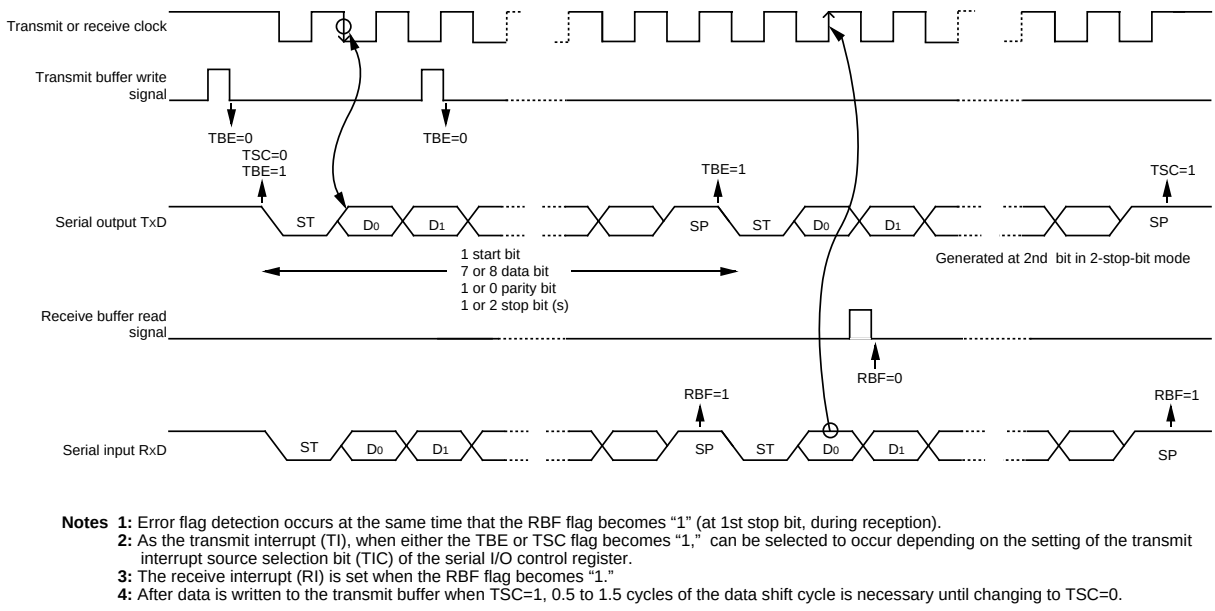


Fig.16 Block diagram of UART serial I/O

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Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes "1," can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1."
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 17 Operation of UART serial I/O function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the serial I/O control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register consists of eight control bits for the serial I/O function.

[UART Control Register (UARTCON)] 001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the P25/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on Serial I/O

1. When using the serial I/O, clear the I^2C-BUS interface enable bit to "0" or the SCL/SDA interrupt pin selection bit to "0".
2. When setting the transmit enable bit of serial I/O to "1", the serial I/O transmit interrupt request bit is automatically set to "1". When not requiring the interrupt occurrence synchronized with the transmission enalbed, take the following sequence.
   ①Set the serial I/O transmit interrupt enable bit to "0" (disabled).
   ②Set the transmit enable bit to "1".
   ③Set the serial I/O transmit interrupt request bit to "0" after 1 or more instructions have been executed.
   ④Set the serial I/O transmit interrupt enable bit to "1" (enabled).

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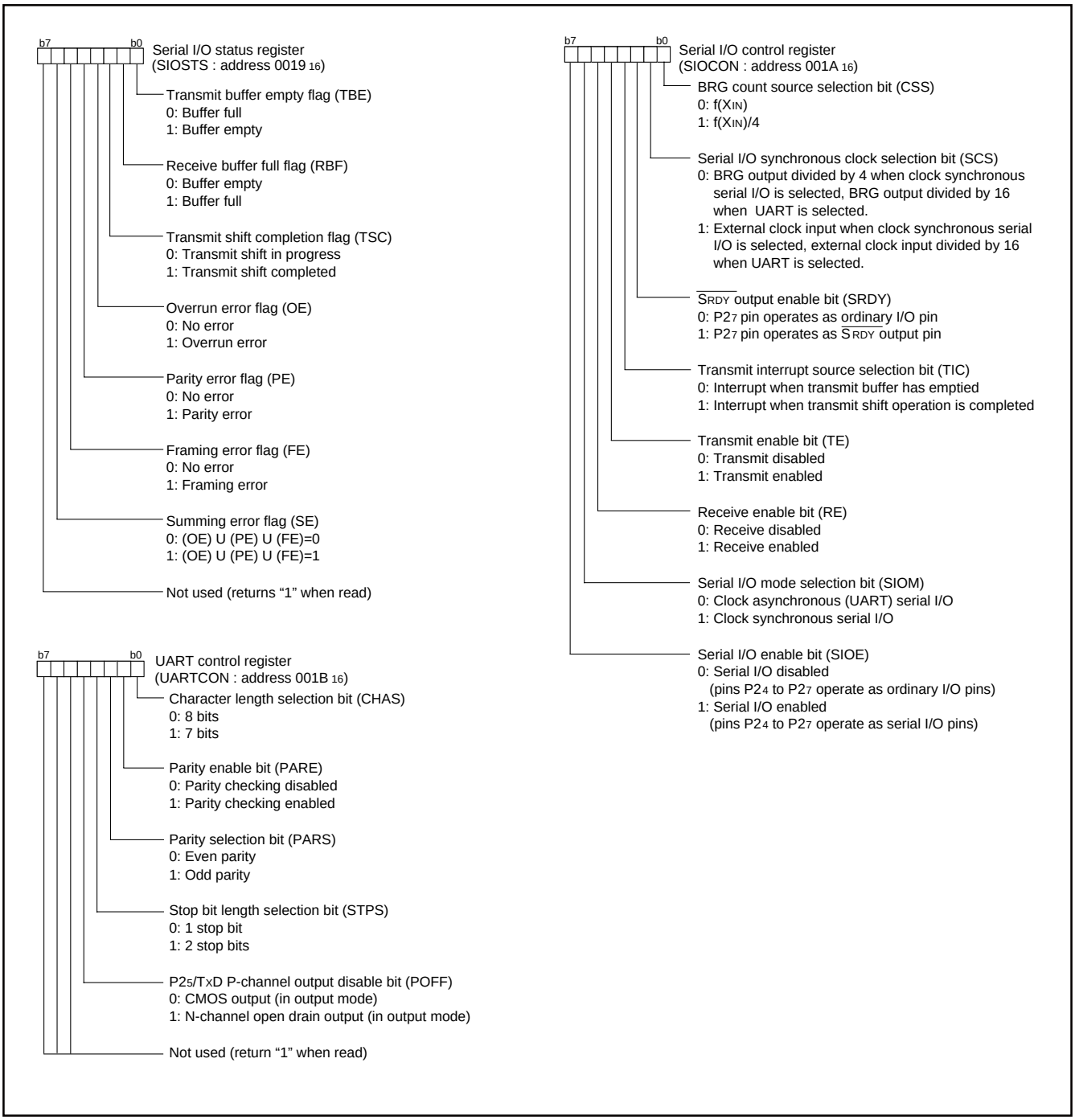


Fig. 18 Structure of serial I/O control registers

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MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 19 shows a block diagram of the multi-master I²C-BUS interface and Table 4 lists the multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register, the I²C start/stop condition control register and other control circuits.

When using the multi-master I²C-BUS interface, set 1 MHz or more to ϕ.

Note: Mitsubishi Electric Corporation assumes no responsibility for infringement of any third-party's rights or originating in the use of the connection control function between the I²C-BUS interface and the ports SCL1, SCL2, SDA1 and SDA2 with the bit 6 of I²C control register (002E16).

Table 4 Multi-master I²C-BUS interface functions

Item	Function
Format	In conformity with Philips I²C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I²C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ= 4 MHz)

System clock ϕ = f(XIN)/2 (high-speed mode)
ϕ = f(XIN)/8 (middle-speed mode)

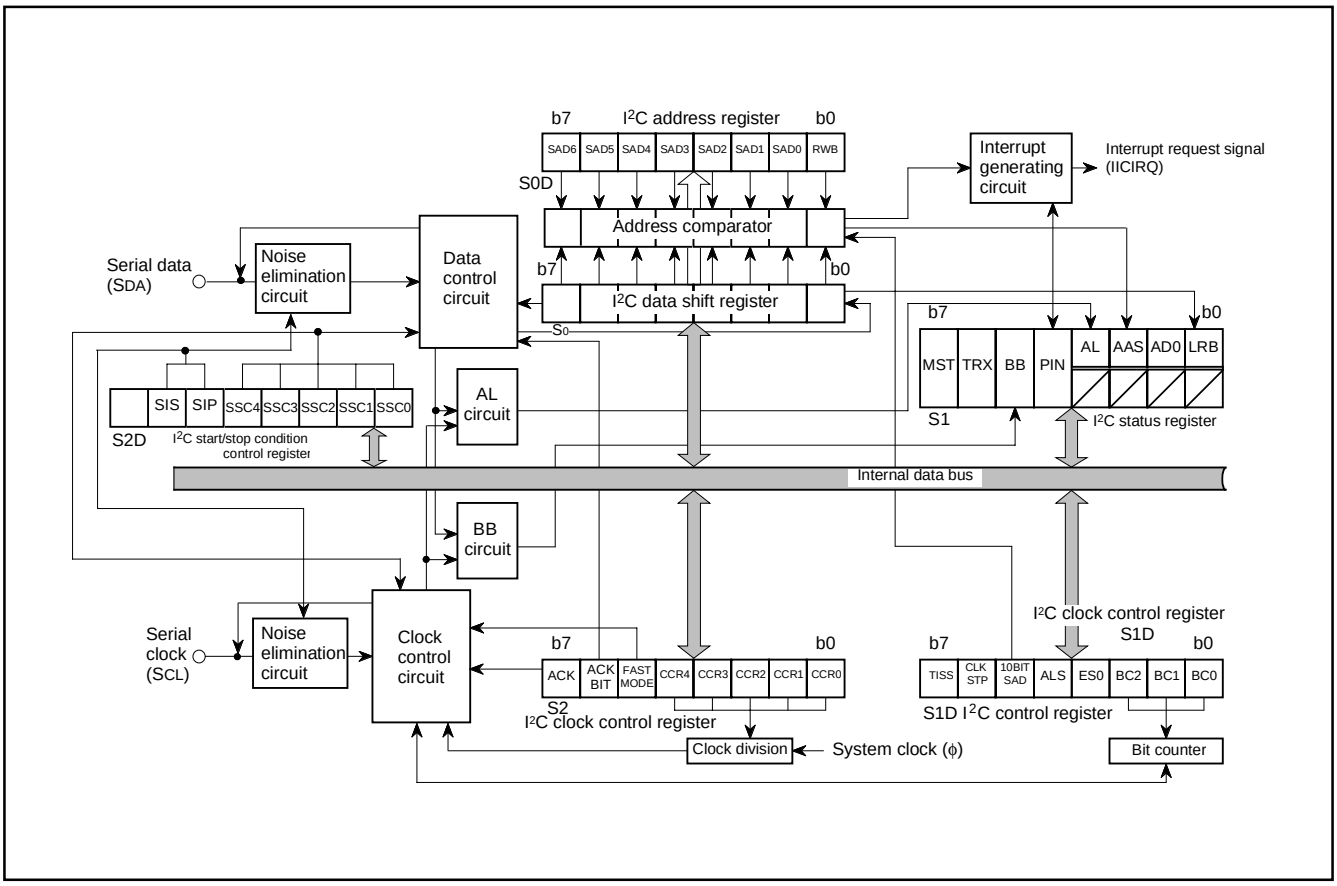


Fig. 19 Block diagram of multi-master I²C-BUS interface

∗ : Purchase of MITSUBISHI ELECTRIC CORPORATIONS I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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[I²C Data Shift Register (S0)] 002B16

The I²C data shift register (S0 : address 002B16) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted by one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted by one bit to the left. The minimum 2 machine cycles are required from the rising of the SCL clock until input to this register.

The I²C data shift register is in a write enable status only when the I²C-BUS interface enable bit (ES0 bit : bit 3 of address 002E16) of the I²C control register is "1". The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (address 002D16) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

[I²C Address Register (S0D)] 002C16

The I²C address register (address 002C16) consists of a 7-bit slave address and a read/$\overline{\text{write}}$ bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition is detected.

•Bit 0: Read/$\overline{\text{write}}$ bit (RWB)

This is not used in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RWB) of the I²C address register.

The RWB bit is cleared to "0" automatically when the stop condition is detected.

•Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

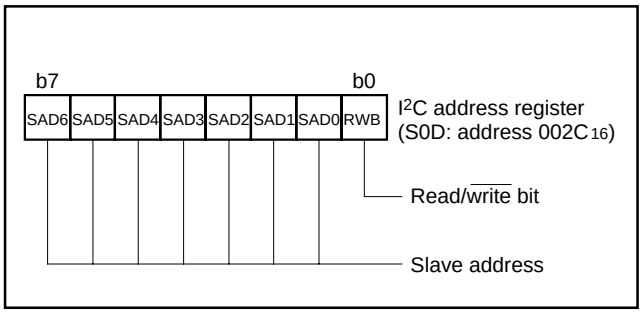


Fig. 20 Structure of I²C address register

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[I²C Clock Control Register (S2)] 002F16

The I²C clock control register (address 002F16) is used to set ACK control, SCL mode and SCL frequency.

•Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 5.

•Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is selected. When the bit is set to "1," the high-speed clock mode is selected.

When connecting the bus of the high-speed mode I²C bus standard (maximum 400 kbits/s), use 8 MHz or more oscillation frequency f(XIN) and 2 division clock.

•Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is selected and SDA goes to "L" at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is selected. The SDA is held in the "H" status at the occurrence of an ACK clock.

However, when the slave address agree with the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made "L" (ACK is returned). If there is a disagreement between the slave address and the address data, the SDA is automatically made "H" (ACK is not returned).

*ACK clock: Clock for acknowledgment

•Bit 7: ACK clock bit (ACK)

This bit specifies the mode of acknowledgment which is an acknowledgment response of data transfer. When this bit is set to "0," the no ACK clock mode is selected. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is selected and the master generates an ACK clock each completion of each 1-byte data transfer. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (makes SDA "H") and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transfer. If data is written during transfer, the I²C clock generator is reset, so that data cannot be transferred normally.

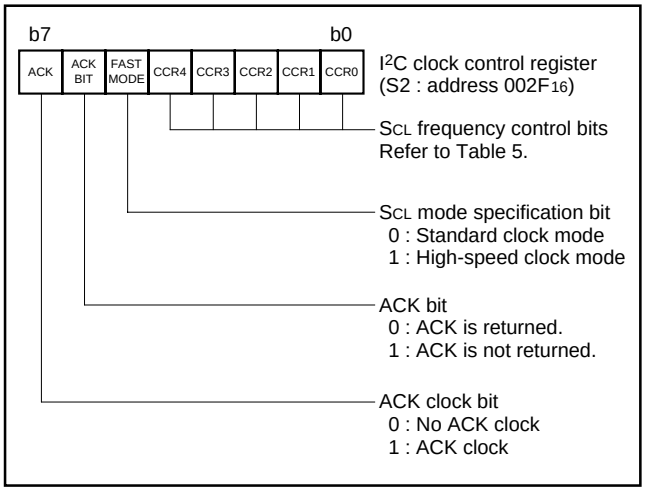


Fig. 21 Structure of I²C clock control register

Table 5 Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency (at ϕ = 4 MHz, unit : kHz)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	– **(Note 2)**	333
0	0	1	0	0	– **(Note 2)**	250
0	0	1	0	1	100	400 **(Note 3)**
0	0	1	1	0	83.3	166
⋮	⋮	⋮	⋮	⋮	500/CCR value **(Note 3)**	1000/CCR value **(Note 3)**
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes 1: Duty of SCL clock output is 50 %. The duty becomes 35 to 45 % only when the high-speed clock mode is selected and CCR value = 5 (400 kHz, at ϕ = 4 MHz). "H" duration of the clock fluctuates from –4 to +2 machine cycles in the standard clock mode, and fluctuates from –2 to +2 machine cycles in the high-speed clock mode. In the case of negative fluctuation, the frequency does not increase because "L" duration is extended instead of "H" duration reduction.
These are value when SCL clock synchronization by the synchronous function is not performed. CCR value is the decimal notation value of the SCL frequency control bits CCR4 to CCR0.

2: Each value of SCL frequency exceeds the limit at ϕ = 4 MHz or more. When using these setting value, use ϕ of 4 MHz or less.

3: The data formula of SCL frequency is described below:
ϕ/(8 × CCR value) Standard clock mode
ϕ/(4 × CCR value) High-speed clock mode (CCR value ≠ 5)
ϕ/(2 × CCR value) High-speed clock mode (CCR value = 5)
Do not set 0 to 2 as CCR value regardless of ϕ frequency.
Set 100 kHz (max.) in the standard clock mode and 400 kHz (max.) in the high-speed clock mode to the SCL frequency by setting the SCL frequency control bits CCR4 to CCR0.

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[I²C Control Register (S1D)] 002E16

The I²C control register (address 002E16) controls data communication format.

•Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. The I²C interrupt request signal occurs immediately after the number of count specified with these bits (ACK clock is added to the number of count when ACK clock is selected by ACK clock bit (bit 7 of address 002F16)) have been transferred, and BC0 to BC2 are returned to "0002".

Also when a START condition is received, these bits become "0002" and the address data is always transmitted and received in 8 bits.

•Bit 3: I²C interface enable bit (ES0)

This bit enables to use the multi-master I²C-BUS interface. When this bit is set to "0," the use disable status is provided, so that the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.

When ES0 = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (which are bits of the I²C status register at address 002D16).
- Writing data to the I²C data shift register (address 002B16) is disabled.

•Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "I²C Status Register," bit 1) is received, transfer processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

•Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 002C16) are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected, and all the bits of the I²C address register are compared with address data.

•Bit 6: SDA/SCL pin selection bit

This bit selects the input/output pins of SCL and SDA of the multi-master I²C-BUS interface.

•Bit 7: I²C-BUS interface pin input level selection bit

This bit selects the input level of the SCL and SDA pins of the multi-master I²C-BUS interface.

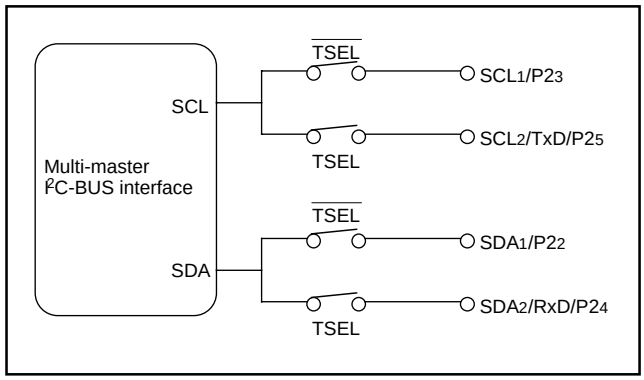


Fig. 22 SDA/SCL pin selection bit

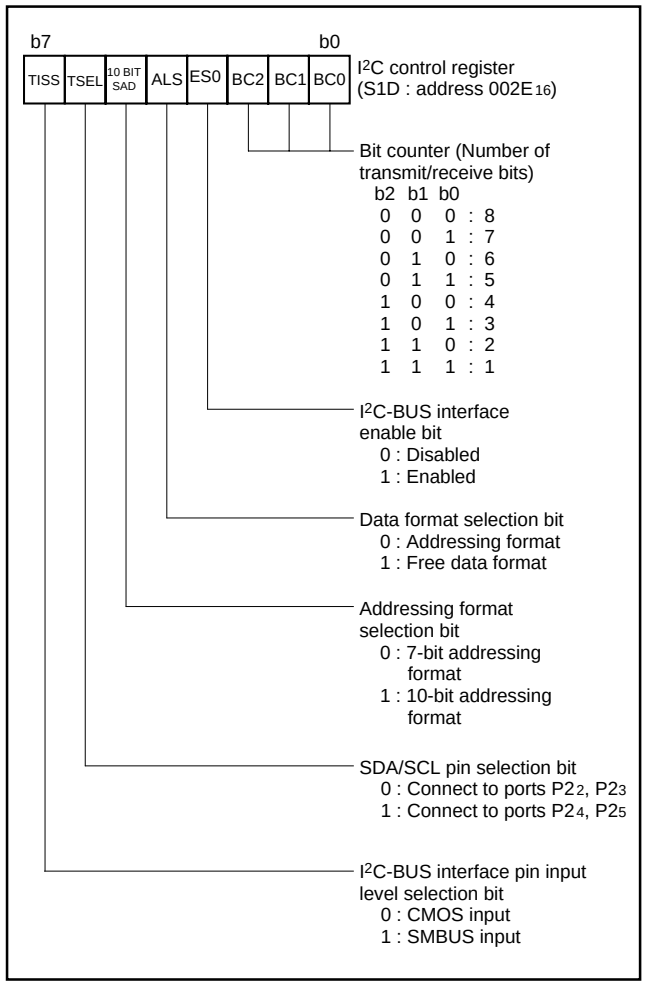


Fig. 23 Structure of I²C control register

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[I²C Status Register (S1)] 002D16

The I²C status register (address 002D16) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

Set "0000₂" to the low-order 4 bits, because these bits become the reserved bits at writing.

•Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 002B16).

•Bit 1: General call detecting flag (AD0)

When the ALS bit is "0", this bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition, or reset.

*General call: The master transmits the general call address "00₁₆" to all slaves.

•Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data when the ALS bit is "0".

① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions:
- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C address register (address 002C16).
- A general call is received.

② In the slave receive mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition:
- When the address data is compared with the I²C address register (8 bits consisting of slave address and RWB bit), the first bytes agree.

③ This bit is set to "0" by executing a write instruction to the I²C data shift register (address 002B16) when ES0 is set to "1" or reset.

•Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." The arbitration lost can be detected only in the master transmission mode. When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to detect the agreement of its own slave address and address data transmitted by another master device.

*Arbitration lost : The status in which communication as a master is disabled.

•Bit 4: SCL pin low hold bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the PIN bit changes from "1" to "0." At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 25 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions:
- Executing a write instruction to the I²C data shift register (address 002B16). (This is the only condition which the prohibition of the internal clock is released and data can be communicated except for the start condition detection.)
- When the ES0 bit is "0"
- At reset
- When writing "1" to the PIN bit by software

The conditions in which the PIN bit is set to "0" are shown below:
- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address agreement or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

•Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. The BB flag is set/reset by the SCL, SDA pins input signal regardless of master/slave. This flag is set to "1" by detecting the start condition, and is set to "0" by detecting the stop condition. The condition of these detecting is set by the start/stop condition setting bits (SSC4–SSC0) of the I²C start/stop condition control register (address 003016). When the ES0 bit of the I²C control register (address 002E16) is "0" or reset, the BB flag is set to "0."

For the writing function to the BB flag, refer to the sections "START Condition Generating Method" and "STOP Condition Generating Method" described later.

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•Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is “0,” the reception mode is selected and the data of a transmitting device is received. When the bit is “1,” the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

This bit is set/reset by software and hardware. About set/reset by hardware is described below. This bit is set to “1” by hardware when all the following conditions are satisfied:

- When ALS is “0”
- In the slave reception mode or the slave transmission mode
- When the R/$\overline{W}$ bit reception is “1”

This bit is set to “0” in one of the following conditions:

- When arbitration lost is detected.
- When a STOP condition is detected.
- When writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- With MST = “0” and when a START condition is detected.
- With MST = “0” and when ACK non-return is detected.
- At reset

•Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is “0,” the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is “1,” the master is specified and a START condition and a STOP condition are generated. Additionally, the clocks required for data communication are generated on the SCL.

This bit is set to “0” in one of the following conditions.

- Immediately after completion of 1-byte data transfer when arbitration lost is detected
- When a STOP condition is detected.
- Writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
- At reset

Note: START condition duplication preventing function
The MST, TRX, and BB bits is set to “1” at the same time after confirming that the BB flag is “0” in the procedure of a START condition occurrence. However, when a START condition by another master device occurs and the BB flag is set to “1” immediately after the contents of the BB flag is confirmed, the START condition duplication preventing function makes the writing to the MST and TRX bits invalid. The duplication preventing function becomes valid from the rising of the BB flag to reception completion of slave address.

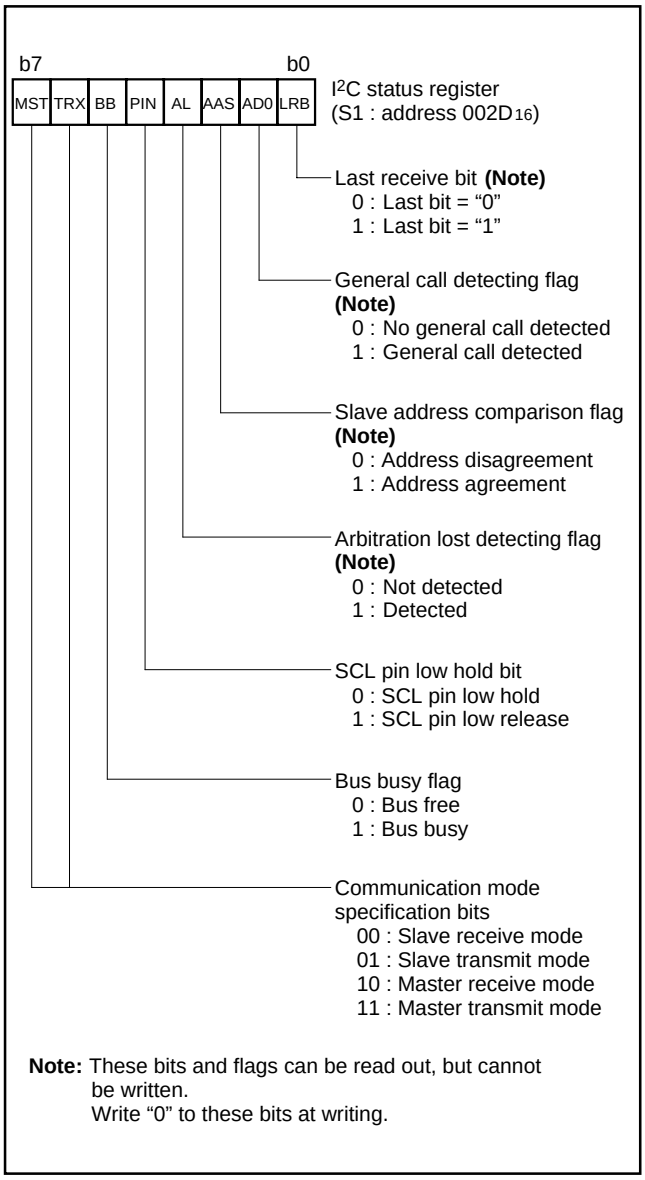


Fig. 24 Structure of I²C status register

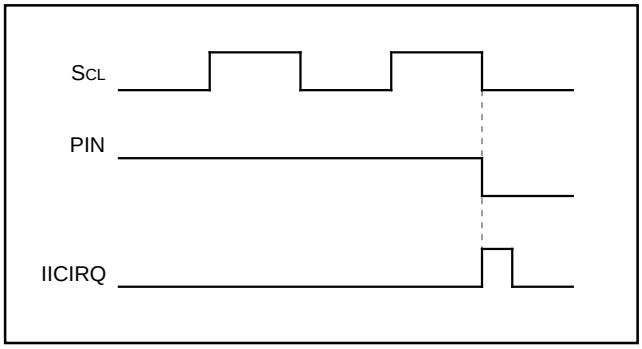


Fig. 25 Interrupt request signal generating timing

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START Condition Generating Method

When writing "1" to the MST, TRX, and BB bits of the I²C status register (address 002D16) at the same time after writing the slave address to the I²C data shift register (address 002B16) with the condition in which the ES0 bit of the I²C control register (address 002E16) and the BB flag are "0", a START condition occurs. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 26, the START condition generating timing diagram, and Table 6, the START condition generating timing table.

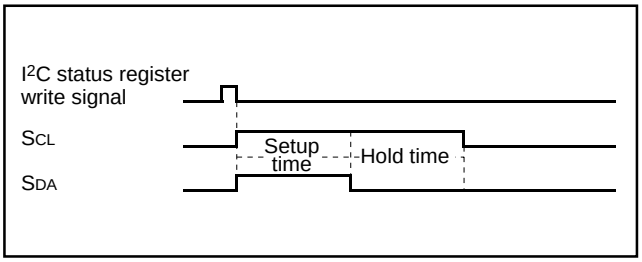


Fig. 26 START condition generating timing diagram

Table 6 START condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Hold time	5.0 µs (20 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

STOP Condition Generating Method

When the ES0 bit of the I²C control register (address 002E16) is "1," write "1" to the MST and TRX bits, and write "0" to the BB bit of the I²C status register (address 002D16) simultaneously. Then a STOP condition occurs. The STOP condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 27, the STOP condition generating timing diagram, and Table 7, the STOP condition generating timing table.

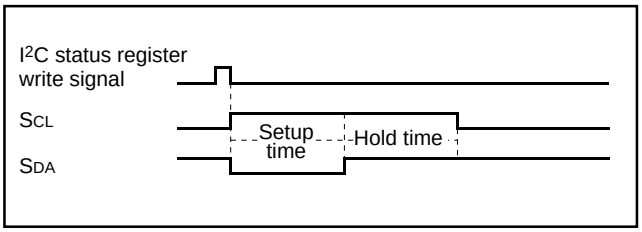


Fig. 27 STOP condition generating timing diagram

Table 7 STOP condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	3.0 µs (12 cycles)
Hold time	4.5 µs (18 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

START/STOP Condition Detecting Operation

The START/STOP condition detection operations are shown in Figures 28, 29, and Table 8. The START/STOP condition is set by the START/STOP condition set bit.

The START/STOP condition can be detected only when the input signal of the SCL and SDA pins satisfy three conditions: SCL release time, setup time, and hold time (see Table 8).

The BB flag is set to "1" by detecting the START condition and is reset to "0" by detecting the STOP condition.

The BB flag set/reset timing is different in the standard clock mode and the high-speed clock mode. Refer to Table 8, the BB flag set/reset time.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" occurs to the CPU.

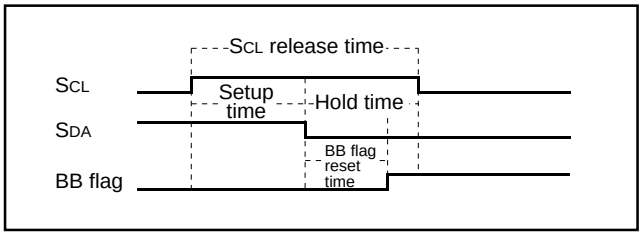


Fig. 28 START condition detecting timing diagram

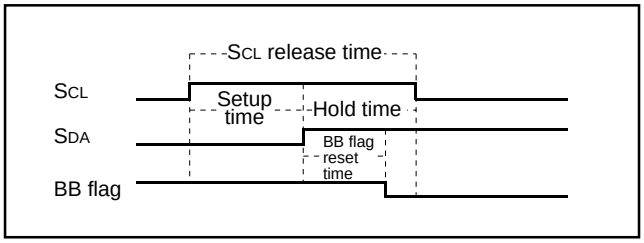


Fig. 29 STOP condition detecting timing diagram

Table 8 START condition/STOP condition detecting conditions

	Standard clock mode	High-speed clock mode
SCL release time	SSC value + 1 cycle (6.25 µs)	4 cycles (1.0 µs)
Setup time	$\frac{\text{SSC value + 1}}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (1.0 µs)
Hold time	$\frac{\text{SSC value + 1}}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (0.5 µs)
BB flag set/ reset time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles (3.375 µs)	3.5 cycles (0.875 µs)

Note: Unit : Cycle number of system clock ϕ
SSC value is the decimal notation value of the START/STOP condition set bits SSC4 to SSC0. Do not set "0" or an odd number to SSC value. The value in parentheses is an example when the I²C START/STOP condition control register is set to "1816" at ϕ = 4 MHz.

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[I²C START/STOP Condition Control Register (S2D)] 003016

The I²C START/STOP condition control register (address 003016) controls START/STOP condition detection.

•Bits 0 to 4: START/STOP condition set bit (SSC4–SSC0)

SCL release time, setup time, and hold time change the detection condition by value of the main clock divide ratio selection bit and the oscillation frequency f(XIN) because these time are measured by the internal system clock. Accordingly, set the proper value to the START/STOP condition set bits (SSC4 to SSC0) in considered of the system clock frequency. Refer to Table 8.

Do not set "000002" or an odd number to the START/STOP condition set bit (SSC4 to SSC0).

Refer to Table 9, the recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency.

•Bit 5: SCL/SDA interrupt pin polarity selection bit (SIP)

An interrupt can occur when detecting the falling or rising edge of the SCL or SDA pin. This bit selects the polarity of the SCL or SDA pin interrupt pin.

•Bit 6: SCL/SDA interrupt pin selection bit (SIS)

This bit selects the pin of which interrupt becomes valid between the SCL pin and the SDA pin.

Note: When changing the setting of the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0, the SCL/SDA interrupt request bit may be set. When selecting the SCL/SDA interrupt source, disable the interrupt before the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0 is set. Reset the request bit to "0" after setting these bits, and enable the interrupt.

Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

① 7-bit addressing format

To adapt the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 002E16) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (address 002C16). At the time of this comparison, address comparison of the RWB bit of the I²C address register (address 002C16) is not performed. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 31, (1) and (2).

② 10-bit addressing format

To adapt the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 002E16) to "1." An address comparison is performed between the first-byte address data transmitted from the master and the 8-bit slave address stored in the I²C address register (address 002C16). At the time of this comparison, an address comparison between the RWB bit of the I²C address register (address 002C16) and the R/$\overline{W}$ bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the RWB bit which is the last bit of the address data not only specifies the direction of communication for control data, but also is processed as an address data bit.

When the first-byte address data agree with the slave address, the AAS bit of the I²C status register (address 002D16) is set to "1." After the second-byte address data is stored into the I²C data shift register (address 002B16), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes agree with the slave address, set the RBW bit of the I²C address register (address 002C16) to "1" by software. This processing can make the 7-bit slave address and R/$\overline{W}$ data agree, which are received after a RESTART condition is detected, with the value of the I²C address register (address 002C16). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 31, (3) and (4).

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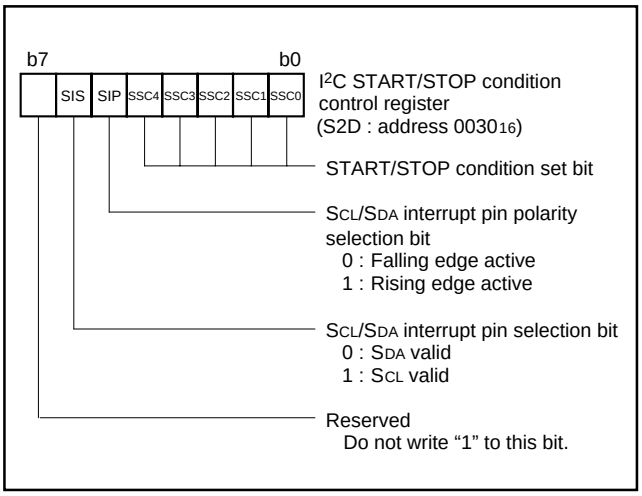


Fig. 30 Structure of I²C START/STOP condition control register

Table 9 Recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency

Oscillation frequency f(XIN) (MHz)	Main clock divide ratio	System clock ϕ (MHz)	START/STOP condition control register	SCL release time (µs)	Setup time (µs)	Hold time (µs)
8	2	4	XXX11010	6.75 µs (27 cycles)	3.375 µs (13.5 cycles)	3.375 µs (13.5 cycles)
			XXX11000	6.25 µs (25 cycles)	3.125 µs (12.5 cycles)	3.125 µs (12.5 cycles)
8	8	1	XXX00100	5.0 µs (5 cycles)	2.5 µs (2.5 cycles)	2.5 µs (2.5 cycles)
4	2	2	XXX01100	6.5 µs (13 cycles)	3.25 µs (6.5 cycles)	3.25 µs (6.5 cycles)
			XXX01010	5.5 µs (11 cycles)	2.75 µs (5.5 cycles)	2.75 µs (5.5 cycles)
2	2	1	XXX00100	5.0 µs (5 cycles)	2.5 µs (2.5 cycles)	2.5 µs (2.5 cycles)

Note: Do not set an odd number to the START/STOP condition set bit (SSC4 to SSC0).

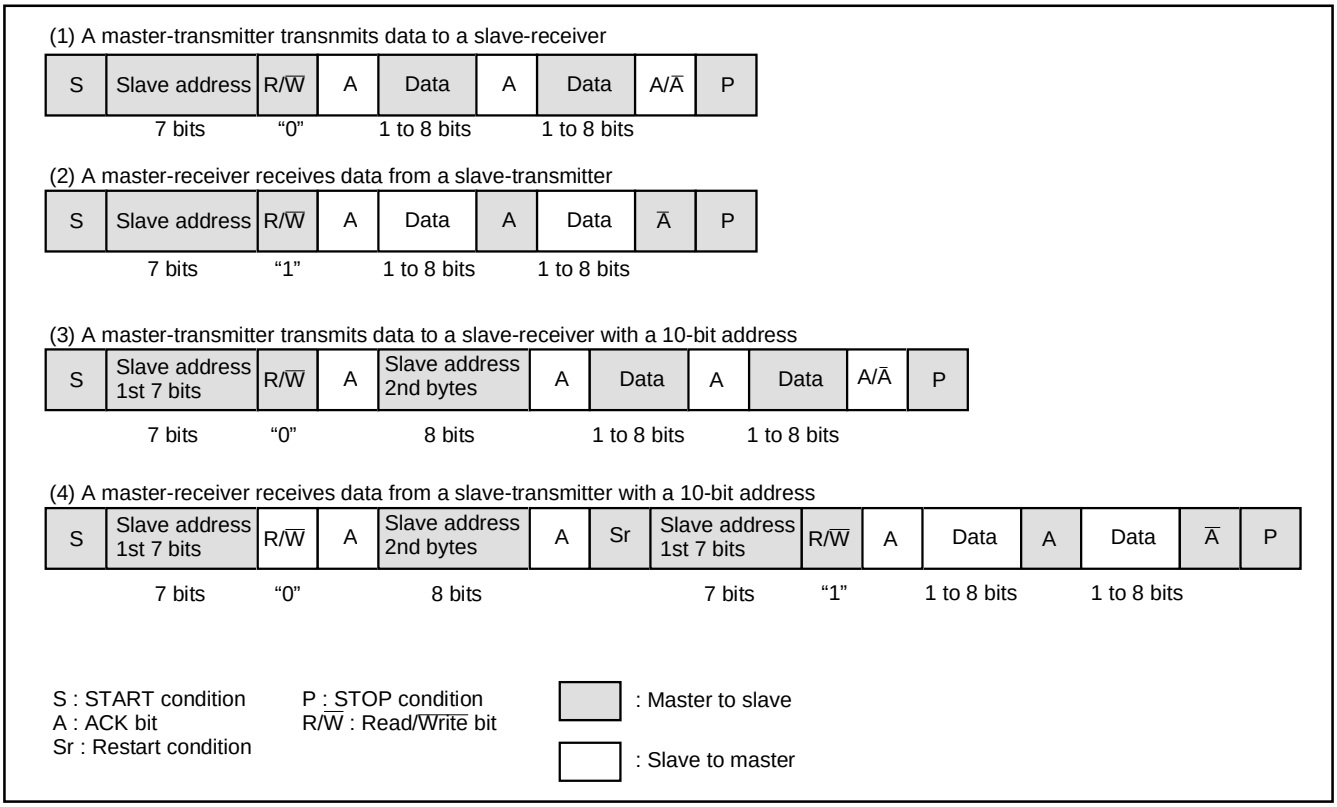


Fig. 31 Address data communication format

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Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $002C_{16}$) and "0" into the RWB bit.
② Set the ACK return mode and SCL = 100 kHz by setting "85_{16}" in the I^2C clock control register (address $002F_{16}$).
③ Set "00_{16}" in the I^2C status register (address $002D_{16}$) so that transmission/reception mode can become initializing condition.
④ Set a communication enable status by setting "08_{16}" in the I^2C control register (address $002E_{16}$).
⑤ Confirm the bus free condition by the BB flag of the I^2C status register (address $002D_{16}$).
⑥ Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (address $002B_{16}$) and set "0" in the least significant bit.
⑦ Set "$F0_{16}$" in the I^2C status register (address $002D_{16}$) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occur.
⑧ Set transmit data in the I^2C data shift register (address $002B_{16}$). At this time, an SCL and an ACK clock automatically occur.
⑨ When transmitting control data of more than 1 byte, repeat step ⑧.
⑩ Set "$D0_{16}$" in the I^2C status register (address $002D_{16}$) to generate a STOP condition if ACK is not returned from slave reception side or transmission ends.

Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $002C_{16}$) and "0" in the RWB bit.
② Set the no ACK clock mode and SCL = 400 kHz by setting "65_{16}" in the I^2C clock control register (address $002F_{16}$).
③ Set "00_{16}" in the I^2C status register (address $002D_{16}$) so that transmission/reception mode can become initializing condition.
④ Set a communication enable status by setting "08_{16}" in the I^2C control register (address $002E_{16}$).
⑤ When a START condition is received, an address comparison is performed.
⑥ •When all transmitted addresses are "0" (general call):
AD0 of the I^2C status register (address $002D_{16}$) is set to "1" and an interrupt request signal occurs.
• When the transmitted addresses agree with the address set in ①:
ASS of the I^2C status register (address $002D_{16}$) is set to "1" and an interrupt request signal occurs.
• In the cases other than the above AD0 and AAS of the I^2C status register (address $002D_{16}$) are set to "0" and no interrupt request signal occurs.
⑦ Set dummy data in the I^2C data shift register (address $002B_{16}$).
⑧ When receiving control data of more than 1 byte, repeat step ⑦.
⑨ When a STOP condition is detected, the communication ends.

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■Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I²C-BUS interface are described below.

- I²C data shift register (S0: address 002B16)
  When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I²C address register (S0D: address 002C16)
  When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because H/W changes the read/write bit (RBW) at the above timing.
- I²C status register (S1: address 002D16)
  Do not execute the read-modify-write instruction for this register because all bits of this register are changed by H/W.
- I²C control register (S1D: address 002E16)
  When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because H/W changes the bit counter (BC0-BC2) at the above timing.
- I²C clock control register (S2: address 002F16)
  The read-modify-write instruction can be executed for this register.
- I²C START/STOP condition control register (S2D: address 003016)
  The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 5.

```
    ⋮
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  BBS 5, S1, BUSBUSY     (BB flag confirming and branch process)
BUSFREE:
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of START condition generating)
  CLI                    (Interrupt enabled)
    ⋮
BUSBUSY:
  CLI                    (Interrupt enabled)
    ⋮
```

2. Use “Branch on Bit Set” of “BBS 5, $002D, –” for the BB flag confirming and branch process.
3. Use “STA $2B, STX $2B” or “STY $2B” of the zero page addressing instruction for writing the slave address value to the I²C data shift register.
4. Execute the branch instruction of above 2 and the store instruction of above 3 continuously shown the above procedure example.
5. Disable interrupts during the following three process steps:
   - BB flag confirming
   - Writing of slave address value
   - Trigger of START condition generating

   When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 4.)
   Execute the following procedure when the PIN bit is “0.”

```
    ⋮
  LDM #$00, S1           (Select slave receive mode)
  LDA —                  (Taking out of slave address value)
  SEI                    (Interrupt disabled)
  STA S0                 (Writing of slave address value)
  LDM #$F0, S1           (Trigger of RESTART condition generating)
  CLI                    (Interrupt enabled)
    ⋮
```

2. Select the slave receive mode when the PIN bit is “0.” Do not write “1” to the PIN bit. Neither “0” nor “1” is specified for the writing to the BB bit.
   The TRX bit becomes “0” and the SDA pin is released.
3. The SCL pin is released by writing the slave address value to the I²C data shift register.
4. Disable interrupts during the following two process steps:
   - Writing of slave address value
   - Trigger of RESTART condition generating

(4) Writing to I²C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to “0” from “1” simultaneously when the PIN bit is “1.” It is because it may become the same as above.

(5) Process of after STOP condition generating

Do not write data in the I²C data shift register S0 and the I²C status register S1 until the bus busy flag BB becomes “0” after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

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PULSE WIDTH MODULATION (PWM)

The 3851 group has a PWM function with an 8-bit resolution, based on a signal that is the clock input XIN or that clock input divided by 2.

Data Setting

The PWM output pin also functions as port P44. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = 255 × (n+1) / f(XIN)

= 31.875 × (n+1) µs (when f(XIN) = 8 MHz, count source = f(XIN))

Output pulse "H" term = PWM period × m / 255

= 0.125 × (n+1) × m µs

(when f(XIN) = 8 MHz, count source = f(XIN))

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

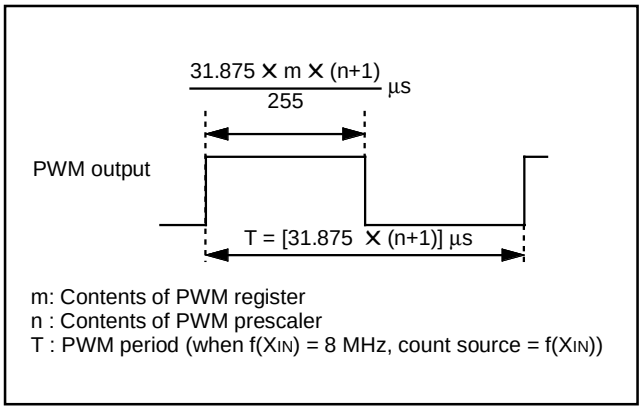


Fig. 32 Timing of PWM period

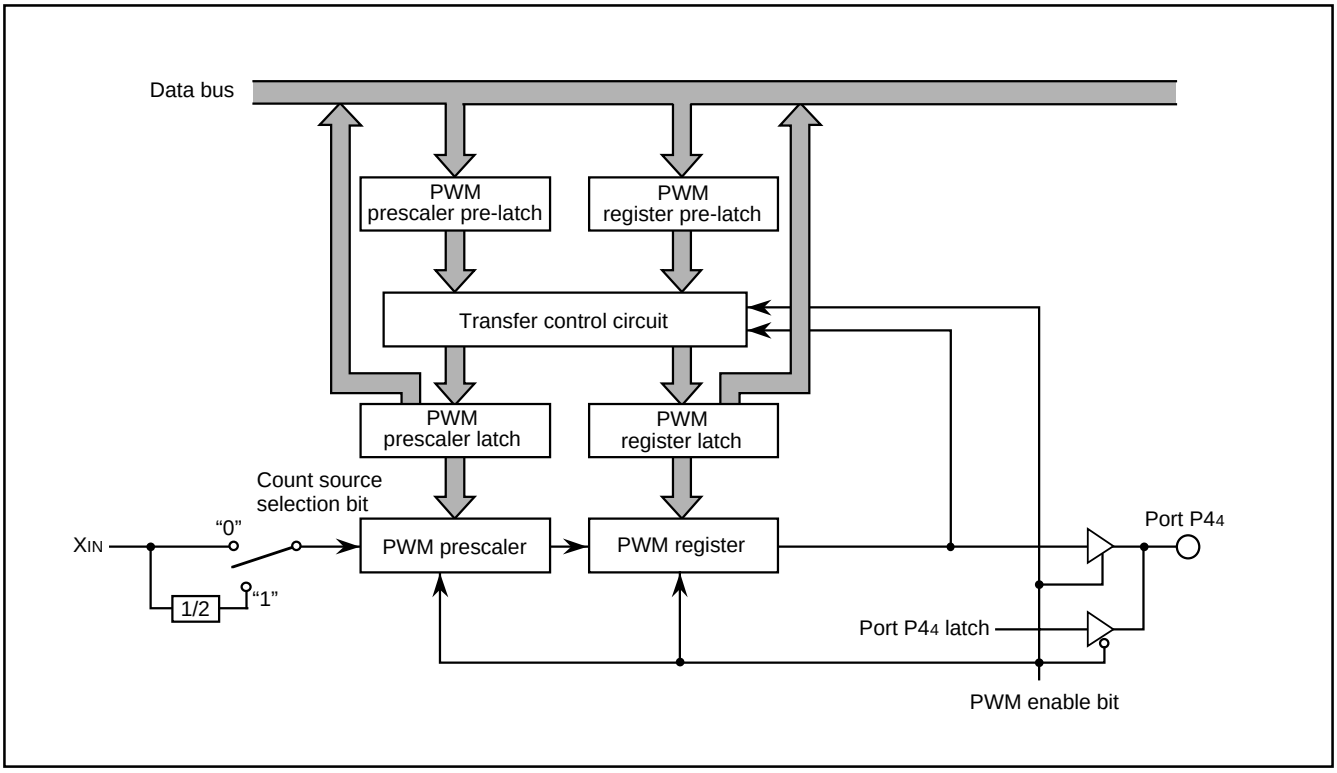


Fig. 33 Block diagram of PWM function

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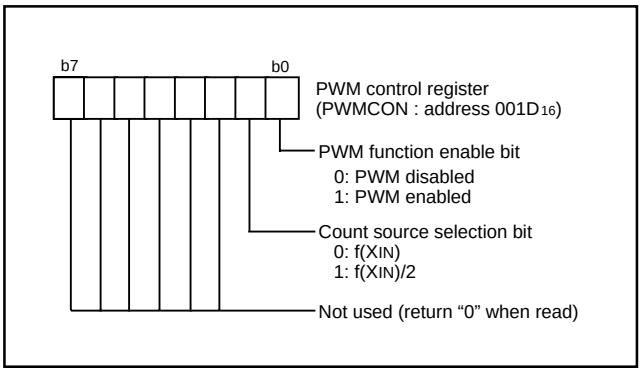


Fig. 34 Structure of PWM control register

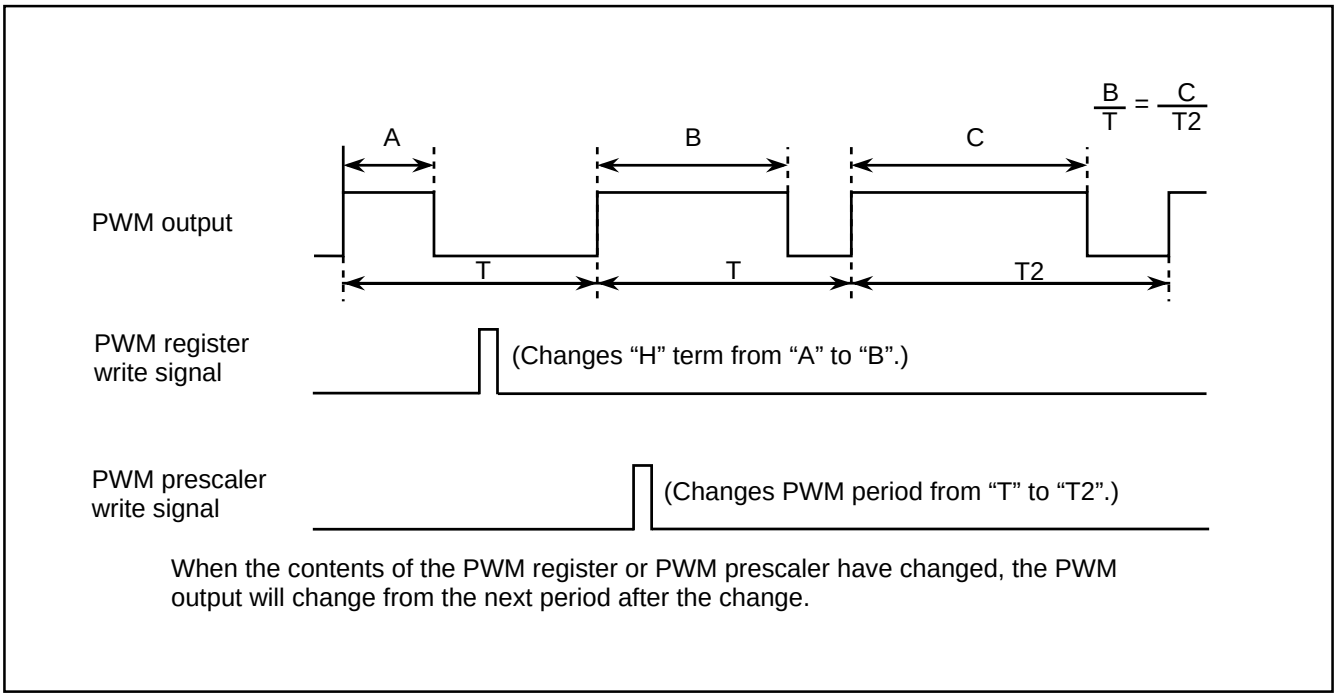


Fig. 35 PWM output timing when PWM register or PWM prescaler is changed

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A-D CONVERTER

[A-D Conversion Registers (ADL, ADH)] 003516, 003616

The A-D conversion registers are read-only registers that store the result of an A-D conversion. Do not read these registers during an A-D conversion

[AD Control Register (ADCON)] 003416

The AD control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 4 indicates the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024 and outputs the divided voltages.

Channel Selector

The channel selector selects one of ports P30/AN0 to P34/AN4 and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage, and the result is stored in the A-D conversion registers. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A-D conversion.

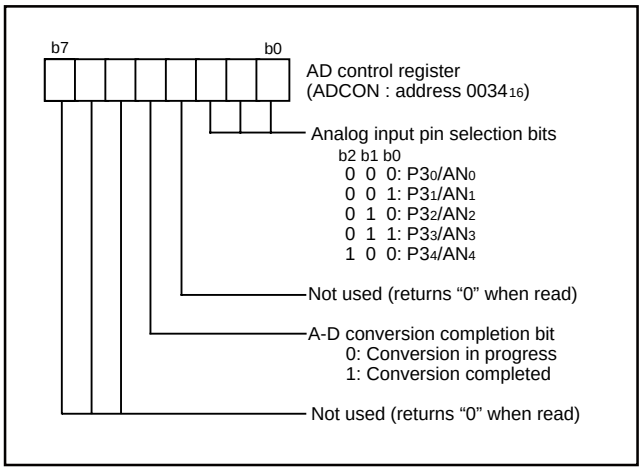


Fig. 36 Structure of AD control register

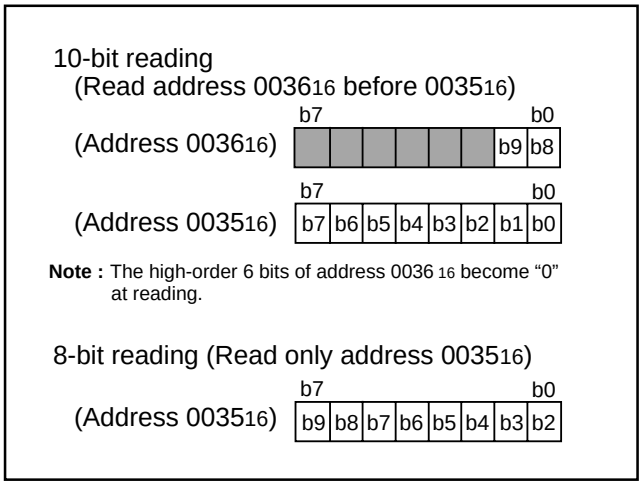


Fig. 37 Structure of A-D conversion registers

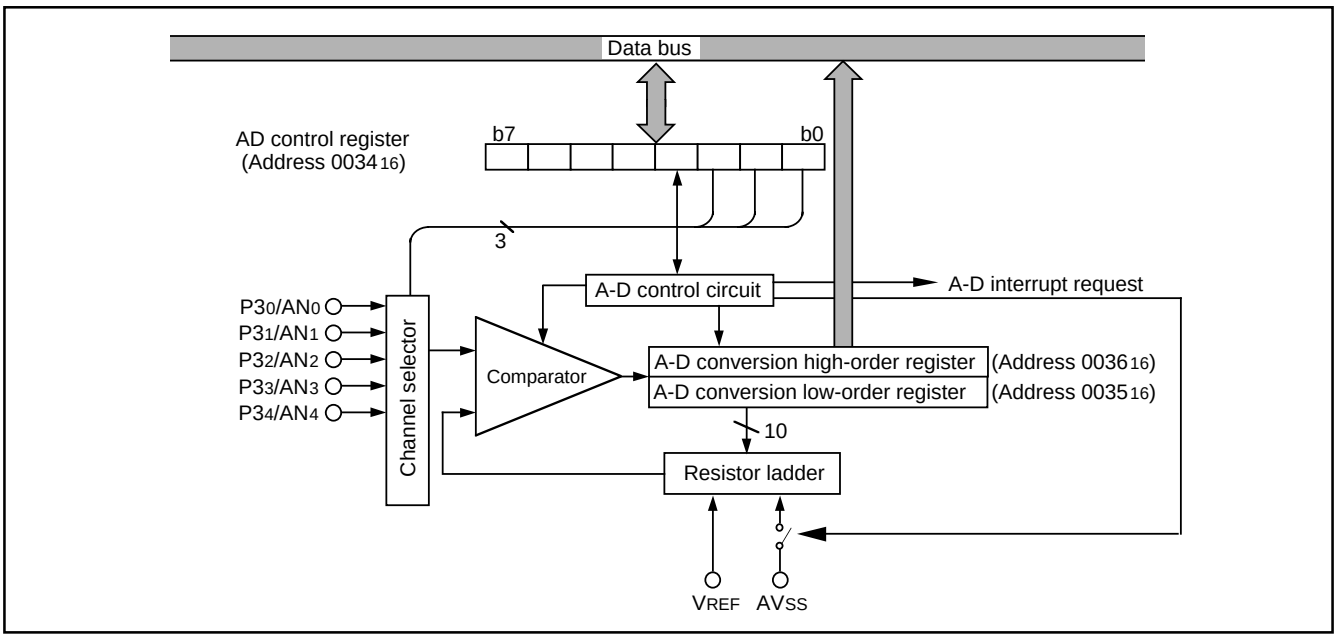


Fig. 38 Block diagram of A-D converter

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WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0039$_{16}$) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0039$_{16}$) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0039$_{16}$) may be started before an underflow. When the watchdog timer control register (address 0039$_{16}$) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

●Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0039$_{16}$), each watchdog timer H and L is set to "FF$_{16}$."

●Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0039$_{16}$) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set to 131.072 ms at f(XIN) = 8 MHz frequency and 32.768 s at f(XCIN) = 32 kHz frequency.

When this bit is set to "1", the count source becomes the signal divided by 16 for f(XIN) (or f(XCIN)). The detection time in this case is set to 512 µs at f(XIN) = 8 MHz frequency and 128 ms at f(XCIN) = 32 kHz frequency. This bit is cleared to "0" after resetting.

●Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0039$_{16}$) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled, once the STP instruction is executed, an internal reset occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after resetting.

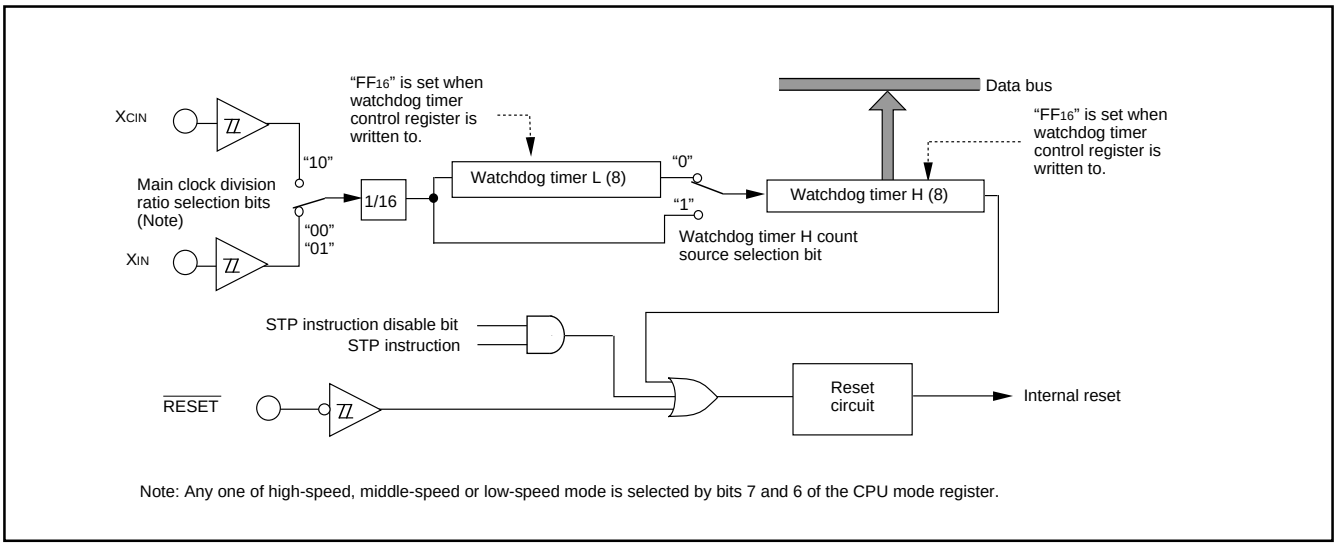


Fig. 39 Block diagram of Watchdog timer

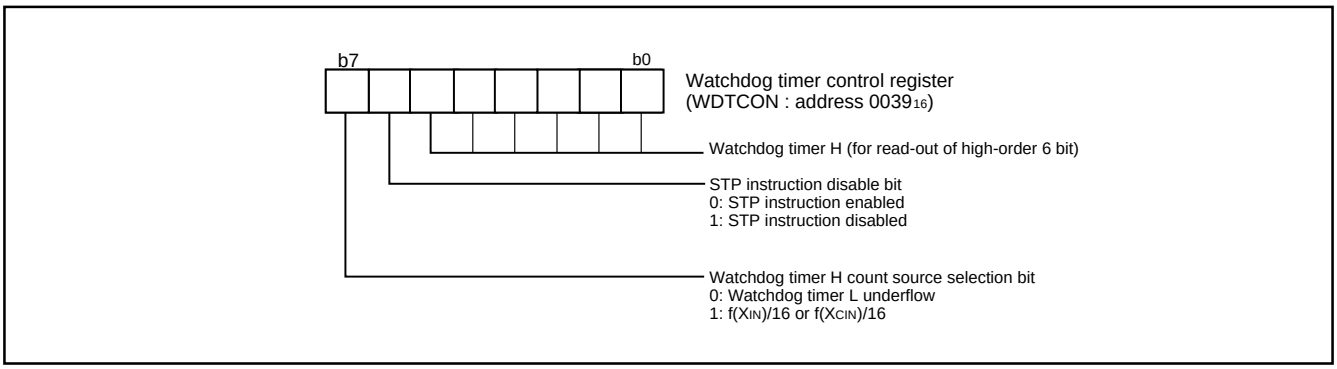


Fig. 40 Structure of Watchdog timer control register

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RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin must be held at an "L" level for 20 cycles or more of X_{IN}. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage must be between 2.7 V and 5.5 V, and the oscillation must be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.54 V for V_{CC} of 2.7 V.

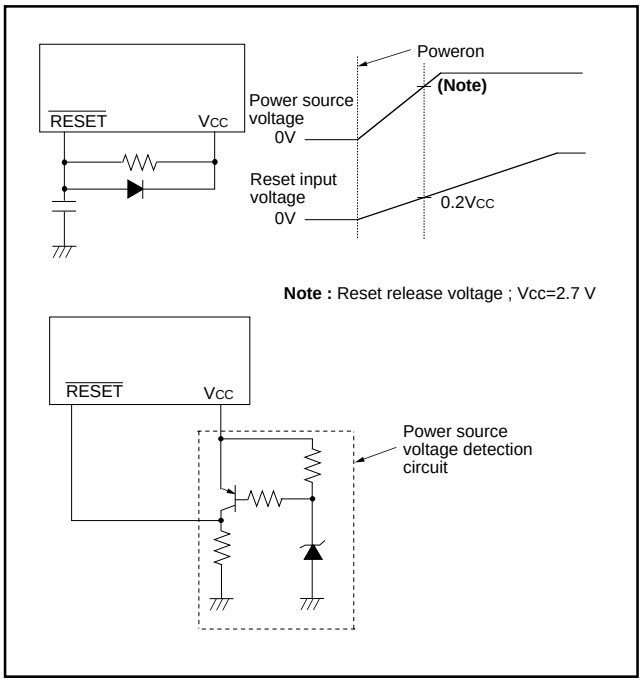


Fig. 41 Reset circuit example

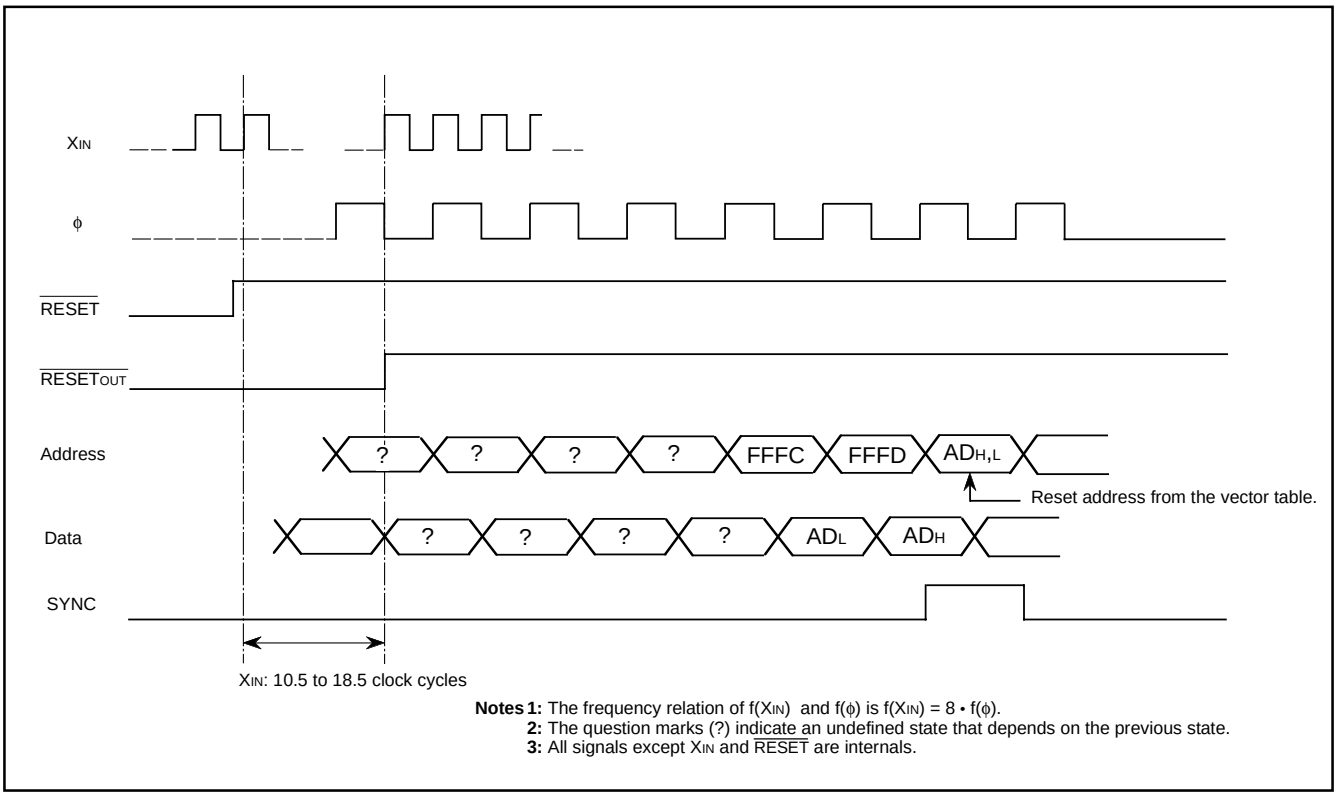


Fig. 42 Reset sequence

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		Address	Register contents
(1)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(2)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(3)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(4)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(5)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(6)	Serial I/O status register (SIOSTS)	0019_{16}	1 0 0 0 0 0 0 0
(7)	Serial I/O control register (SIOCON)	$001A_{16}$	00_{16}
(8)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(9)	PWM control register (PWMCON)	$001D_{16}$	00_{16}
(10)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(11)	Timer 1 (T1)	0021_{16}	01_{16}
(12)	Timer 2 (T2)	0022_{16}	00_{16}
(13)	Timer XY mode register (TM)	0023_{16}	00_{16}
(14)	Prescaler X (PREX)	0024_{16}	FF_{16}
(15)	Timer X (TX)	0025_{16}	FF_{16}
(16)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(17)	Timer Y (TY)	0027_{16}	FF_{16}
(18)	Timer count source select register	0028_{16}	00_{16}
(19)	I^2C address register (S0D)	$002C_{16}$	00_{16}
(20)	I^2C status register (S1)	$002D_{16}$	0 0 0 1 0 0 0 X
(21)	I^2C control register (S1D)	$002E_{16}$	00_{16}
(22)	I^2C clock control register (S2)	$002F_{16}$	00_{16}
(23)	I^2C start/stop condition control register (S2D)	0030_{16}	0 0 0 X X X X X
(24)	AD control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(25)	MISRG	0038_{16}	00_{16}
(26)	Watchdog timer control register (WDTCON)	0039_{16}	0 0 1 1 1 1 1 1
(27)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(28)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(29)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(30)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(31)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(32)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(33)	Processor status register	(PS)	X X X X X 1 X X
(34)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X indicates Not fixed .

Fig. 43 Internal status at reset

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CLOCK GENERATING CIRCUIT

The 3851 group has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.
Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from the stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3•f(XCIN).

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.
The sub-clock XCIN-XCOUT oscillation circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillation stops. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116." When the oscillation stabilizing time set after STP instruction released bit is "1," set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.
Either XIN or XCIN divided by 16 is input to the prescaler 12 as count source. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized. When the oscillator is restarted by reset, apply "L" level to the RESET pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.
When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

■Note

When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

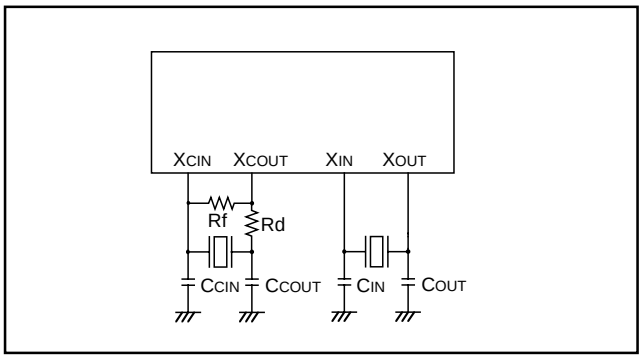


Fig. 44 Ceramic resonator circuit

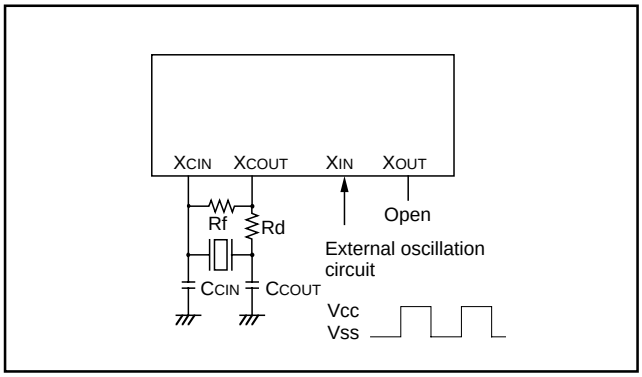


Fig. 45 External clock input circuit

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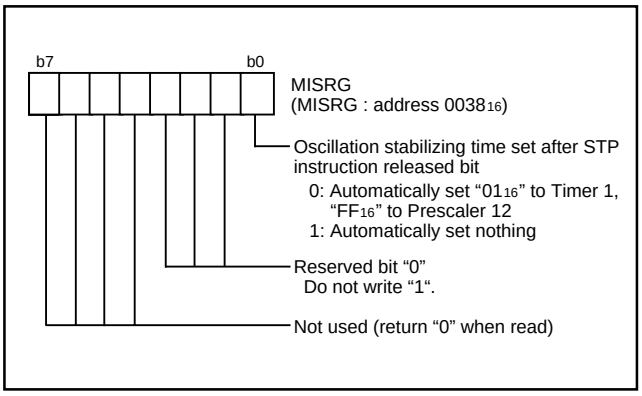
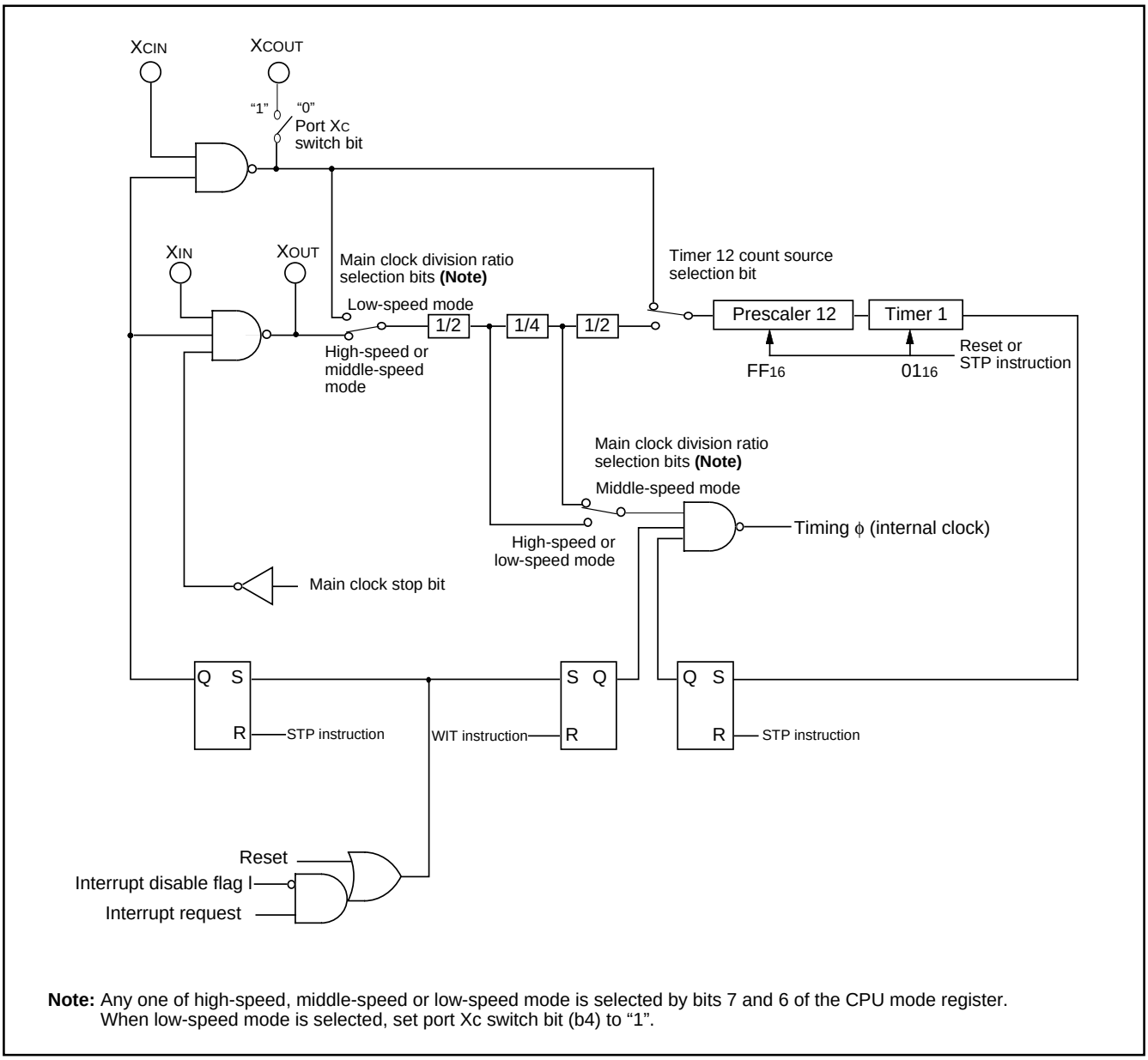


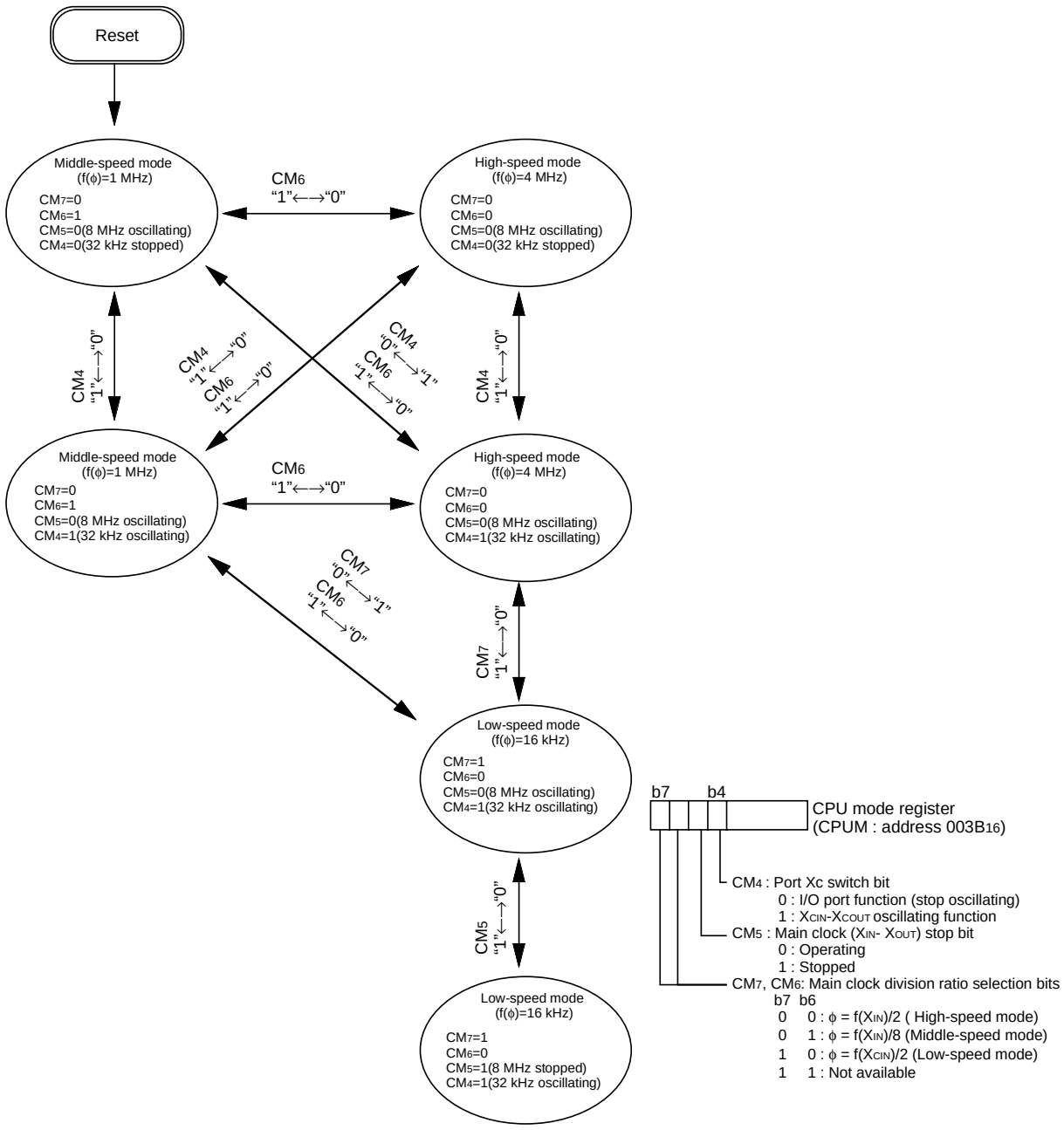
Fig. 46 Structure of MISRG



Note: Any one of high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port Xc switch bit (b4) to "1".

Fig. 47 System clock generating circuit block diagram (Single-chip mode)

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Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)

2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.

3 : Timer operates in the wait mode.

4 : When bit 0 of MISRG is "0" and the stop mode is ended, a delay of approximately 1 ms occurs by connecting timer 1 in middle/high-speed mode.

5 : When bit 0 of MISRG is "0" and the stop mode is ended, the following is performed.
(1) After the clock is restarted, a delay of approximately 256 ms occurs in low-speed mode if Timer 12 count source selection bit is "0".
(2) After the clock is restarted, a delay of approximately 16 ms occurs in low-speed mode if Timer 12 count source selection bit is "1".

6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.

7 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 48 State transitions of system clock

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NOTES ON PROGRAMMING
Processor Status Register
The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts
The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations
- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers
If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions
- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports
The contents of the port direction registers cannot be read. The following cannot be used:
- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O
In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1."

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

When an external clock is used as synchronous clock in serial I/O, write transmission data to the transmit buffer register while the transfer clock is "H."

A-D Converter
The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(XIN) is at least on 500 kHz during an A-D conversion.

Do not execute the STP instruction during an A-D conversion.

Instruction Execution Time
The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency in high-speed mode.

NOTES ON USAGE
Handling of Source Pins
In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin) and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF–0.1μF is recommended.

EPROM Version/One Time PROM Version
The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (VPP pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin or Vcc pin with 1 to 10 kΩ resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

Electric Characteristic Differences Between Mask ROM and One Time PROM Version MCUs
There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between Mask ROM and One Time PROM version MCUs due to the differences in the manufacturing processes.

When manufacturing an application system with the One Time PROM version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

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DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form*
2. Mark Specification Form*
3. Data to be written to ROM, in EPROM form (three identical copies)

DATA REQUIRED FOR ROM WRITING ORDERS

The following are necessary when ordering a ROM writing:

1. ROM Writing Confirmation Form*
2. Mark Specification Form* (only special mark with customer's trade mark logo)
3. Data to be written to ROM, in EPROM form (three identical copies)

*For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (http://www.infomicom.maec.co.jp/indexe.htm).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 10 Programming adapter

Package	Name of Programming Adapter
42P2R-A	PCA4738F-42A
42P4B	PCA4738S-42A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 49 is recommended to verify programming.

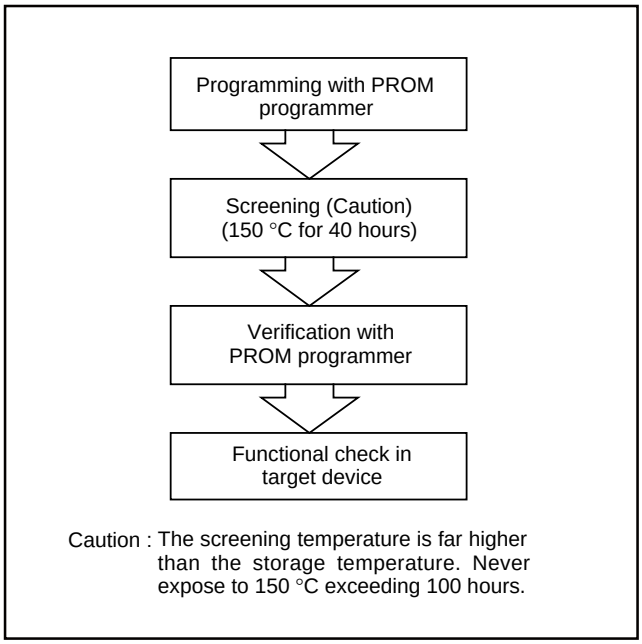


Fig. 49 Programming and testing of One Time PROM version

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ELECTRICAL CHARACTERISTICS

Table 11 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P2_2$, $P2_3$		–0.3 to 5.8	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS}		–0.3 to 13	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P2_2$, $P2_3$		–0.3 to 5.8	V
P_d	Power dissipation	T_a = 25 °C	1000 **(Note)**	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Note : The rating becomes 300 mW at the 42P2R-A/E package.

Table 12 Recommended operating conditions (1)
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage (At 8 MHz)	4.0	5.0	5.5	V
	Power source voltage (At 4 MHz)	2.7	5.0	5.5	
V_{SS}	Power source voltage		0		V
V_{REF}	A-D convert reference voltage	2.0		V_{CC}	V
AV_{SS}	Analog power source voltage		0		V
V_{IA}	Analog input voltage AN_0–AN_4	AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (when I^2C-BUS input level is selected) SDA_1, SCL_1	0.7V_{CC}		5.8	V
V_{IH}	"H" input voltage (when I^2C-BUS input level is selected) SDA_2, SCL_2	0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage (when SMBUS input level is selected) SDA_1, SCL_1	1.4		5.8	V
V_{IH}	"H" input voltage (when SMBUS input level is selected) SDA_2, SCL_2	1.4		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage (when I^2C-BUS input level is selected) SDA_1, SDA_2, SCL_1, SCL_2	0		0.3V_{CC}	V
V_{IL}	"L" input voltage (when SMBUS input level is selected) SDA_1, SDA_2, SCL_1, SCL_2	0		0.6	V
V_{IL}	"L" input voltage $\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	"H" total peak output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_4$ (Note)			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P4_0$–$P4_4$ (Note)			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P0_0$–$P0_7$, $P1_0$–$P1_2$, $P3_0$–$P3_4$ (Note)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P1_3$–$P1_7$ (Note)			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current $P2_0$–$P2_7$,$P4_0$–$P4_4$ (Note)			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_0$–$P3_4$ (Note)			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P4_0$–$P4_4$ (Note)			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P0_0$–$P0_7$, $P1_0$–$P1_2$, $P3_0$–$P3_4$ (Note)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P1_3$–$P1_7$ (Note)			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current $P2_0$–$P2_7$,$P4_0$–$P4_4$ (Note)			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

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Table 13 Recommended operating conditions (2)
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 1)			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_2$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 1)			10	mA
$I_{OL(peak)}$	"L" peak output current	$P1_3$–$P1_7$ (Note 1)			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 2)			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_2$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ (Note 2)			5	mA
$I_{OL(avg)}$	"L" peak output current	$P1_3$–$P1_7$ (Note 2)			15	mA
f(X_{IN})	Internal clock oscillation frequency (V_{CC} = 4.0 to 5.5V) (Note 3)				8	MHz
f(X_{IN})	Internal clock oscillation frequency (V_{CC} = 2.7 to 5.5V) (Note 3)				4	kHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50%.

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Table 14 Electrical characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄ **(Note)**	I_{OH} = –10 mA V_{CC} = 4.0–5.5 V	V_{CC}–2.0			V
		I_{OH} = –1.0 mA V_{CC} = 2.7–5.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage P0₀–P0₇, P1₀–P1₂, P2₀–P2₇ P3₀–P3₄, P4₀–P4₄	I_{OL} = 10 mA V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 1.0 mA V_{CC} = 2.7–5.5 V			1.0	V
V_{OL}	"L" output voltage P1₃–P1₇	I_{OL} = 20 mA V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 10 mA V_{CC} = 2.7–5.5 V			1.0	V
V_{T+}–V_{T-}	Hysteresis CNTR₀, CNTR₁, INT₀–INT₃			0.4		V
V_{T+}–V_{T-}	Hysteresis RxD, SCLK			0.5		V
V_{T+}–V_{T-}	Hysteresis $\overline{\text{RESET}}$			0.5		V
I_{IH}	"H" input current P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{\text{RESET}}$, CNV$_{SS}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current P0₀–P0₇, P1₀–P1₇, P2₀–P2₇ P3₀–P3₄, P4₀–P4₄	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $\overline{\text{RESET}}$,CNV$_{SS}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4		µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V

Note: P2₅ is measured when the P2₅/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

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Table 15 Electrical characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			6.8	13	mA
		High-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			1.6		mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			60	200	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			20	40	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			20	55	µA
		Low-speed mode (V_{CC} = 3 V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			5.0	10.0	µA
		Middle-speed mode $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = stopped Output transistors “off”			4.0	7.0	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			1.5		mA
		Increment when A-D conversion is executed $f(X_{IN})$ = 8 MHz			800		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

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Table 16 A-D converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				10	bit
–	Absolute accuracy (excluding quantization error)				±4	LSB
t_{CONV}	Conversion time				61	tc(ϕ)
R_{LADDER}	Ladder resistor			35		kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5.0 V	50	150	200	μA
$I_{I(AD)}$	A-D port input current			0.5	5.0	μA

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TIMING REQUIREMENTS

Table 17 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	20			X_{IN} cycle
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “L” pulse width	80			ns
$t_{C(SCLK)}$	Serial I/O clock input cycle time (Note)	800			ns
$t_{WH(SCLK)}$	Serial I/O clock input “H” pulse width (Note)	370			ns
$t_{WL(SCLK)}$	Serial I/O clock input “L” pulse width (Note)	370			ns
$t_{su(RxD-SCLK)}$	Serial I/O input setup time	220			ns
$t_{h(SCLK-RxD)}$	Serial I/O input hold time	100			ns

Note : When $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

Table 18 Timing requirements (2)

(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	20			X_{IN} cycle
$t_{C(XIN)}$	External clock input cycle time	250			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “H” pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$, INT_0–INT_3 input “L” pulse width	230			ns
$t_{C(SCLK)}$	Serial I/O clock input cycle time (Note)	2000			ns
$t_{WH(SCLK)}$	Serial I/O clock input “H” pulse width (Note)	950			ns
$t_{WL(SCLK)}$	Serial I/O clock input “L” pulse width (Note)	950			ns
$t_{su(RxD-SCLK)}$	Serial I/O input setup time	400			ns
$t_{h(SCLK-RxD)}$	Serial I/O input hold time	200			ns

Note : When $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

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Table 19 Switching characteristics 1

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH} (SCLK)	Serial I/O clock output "H" pulse width	t_C(SCLK)/2–30			ns
t_{WL} (SCLK)	Serial I/O clock output "L" pulse width	t_C(SCLK)/2–30			ns
t_d (SCLK-TxD)	Serial I/O output delay time (Note 1)			140	ns
t_V (SCLK-TxD)	Serial I/O output valid time (Note 1)	–30			ns
t_r (SCLK)	Serial I/O clock output rising time			30	ns
t_f (SCLK)	Serial I/O clock output falling time			30	ns
t_r (CMOS)	CMOS output rising time (Note 2)		10	30	ns
t_f (CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1: For t_{WH}(SCLK), t_{WL}(SCLK), when the P51/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: The X_{OUT} pin is excluded.

Table 20 Switching characteristics 2

(V_{CC} = 2.7 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WH} (SCLK)	Serial I/O clock output "H" pulse width	t_C(SCLK)/2–50			ns
t_{WL} (SCLK)	Serial I/O clock output "L" pulse width	t_C(SCLK)/2–50			ns
t_d (SCLK-TxD)	Serial I/O output delay time (Note 1)			350	ns
t_V (SCLK-TxD)	Serial I/O output valid time (Note 1)	–30			ns
t_r (SCLK)	Serial I/O clock output rising time			50	ns
t_f (SCLK)	Serial I/O clock output falling time			50	ns
t_r (CMOS)	CMOS output rising time (Note 2)		20	50	ns
t_f (CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1: For t_{WH}(SCLK), t_{WL}(SCLK), when the P51/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: The X_{OUT} pin is excluded.

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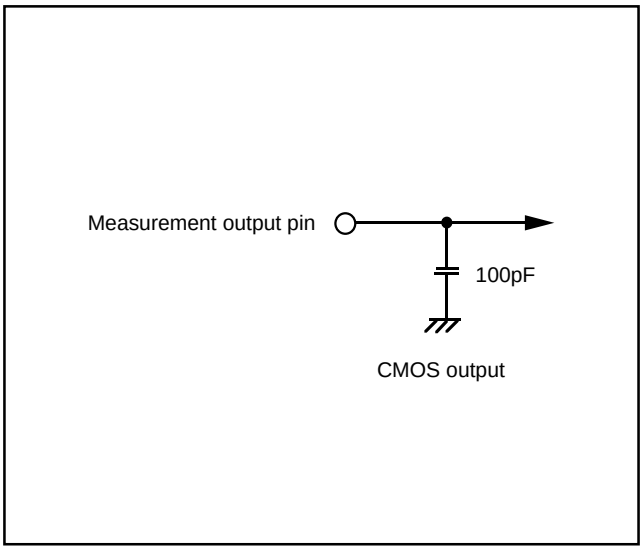


Fig. 50 Circuit for measuring output switching characteristics (1)

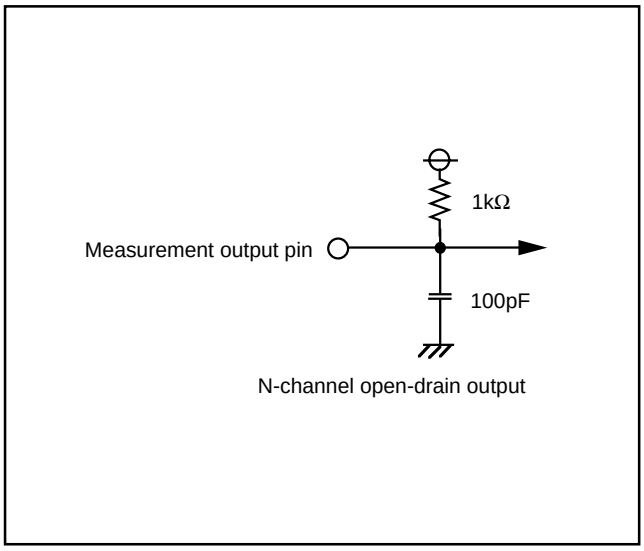


Fig. 51 Circuit for measuring output switching characteristics (2)

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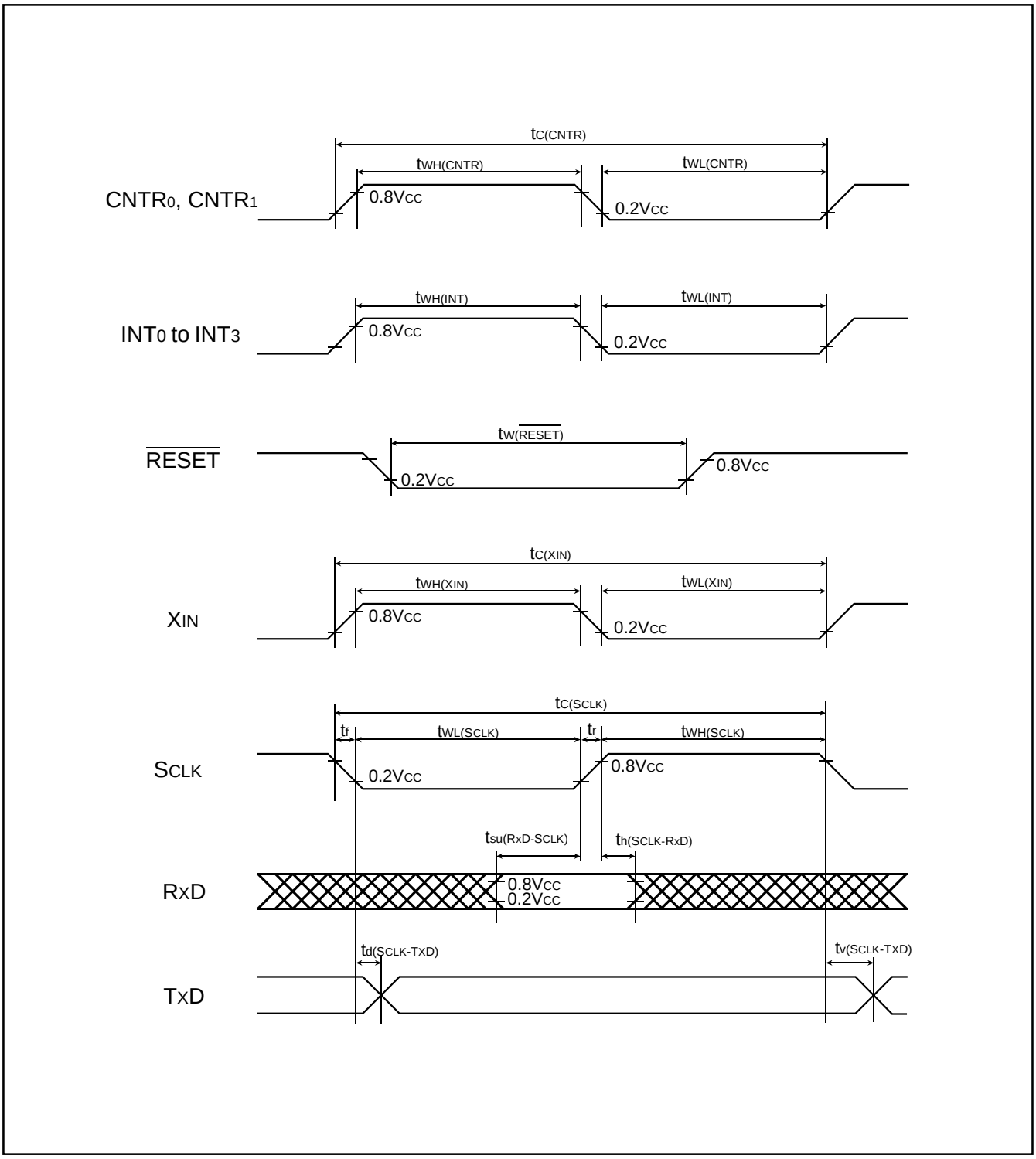


Fig. 52 Timing diagram

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MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Table 21 Multi-master I²C-BUS bus line characteristics

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	Hold time for SCL clock = "0"	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time for SCL clock = "1"	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
$t_{SU;DAT}$	Data setup time	250		100		ns
$t_{SU;STA}$	Setup time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Setup time for STOP condition	4.0		0.6		µs

Note: C_b = total capacitance of 1 bus line

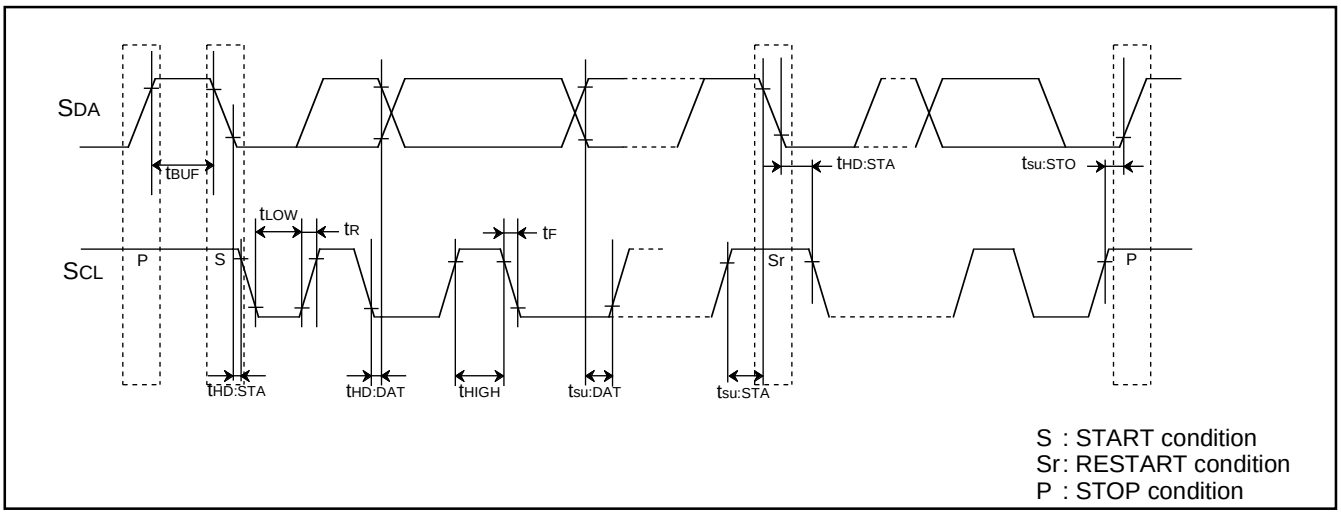


Fig. 53 Timing diagram of multi-master I²C-BUS

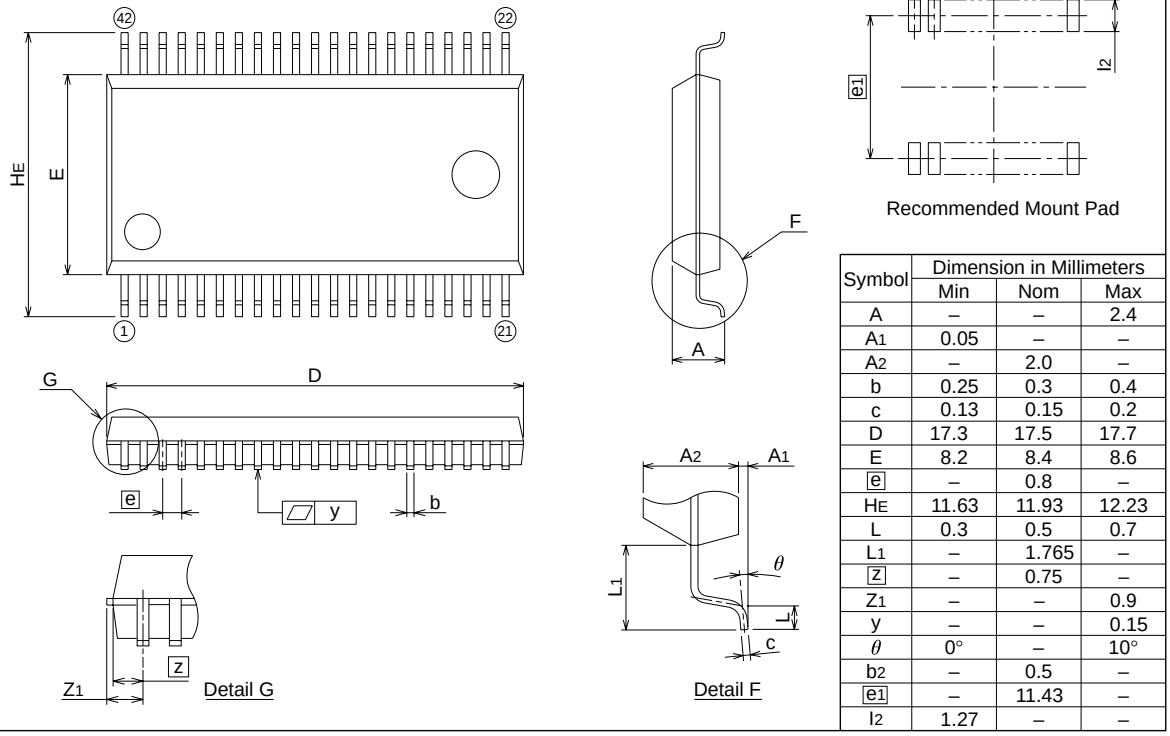
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PACKAGE OUTLINE

42P2R-A/E

Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	–	0.63	Alloy 42

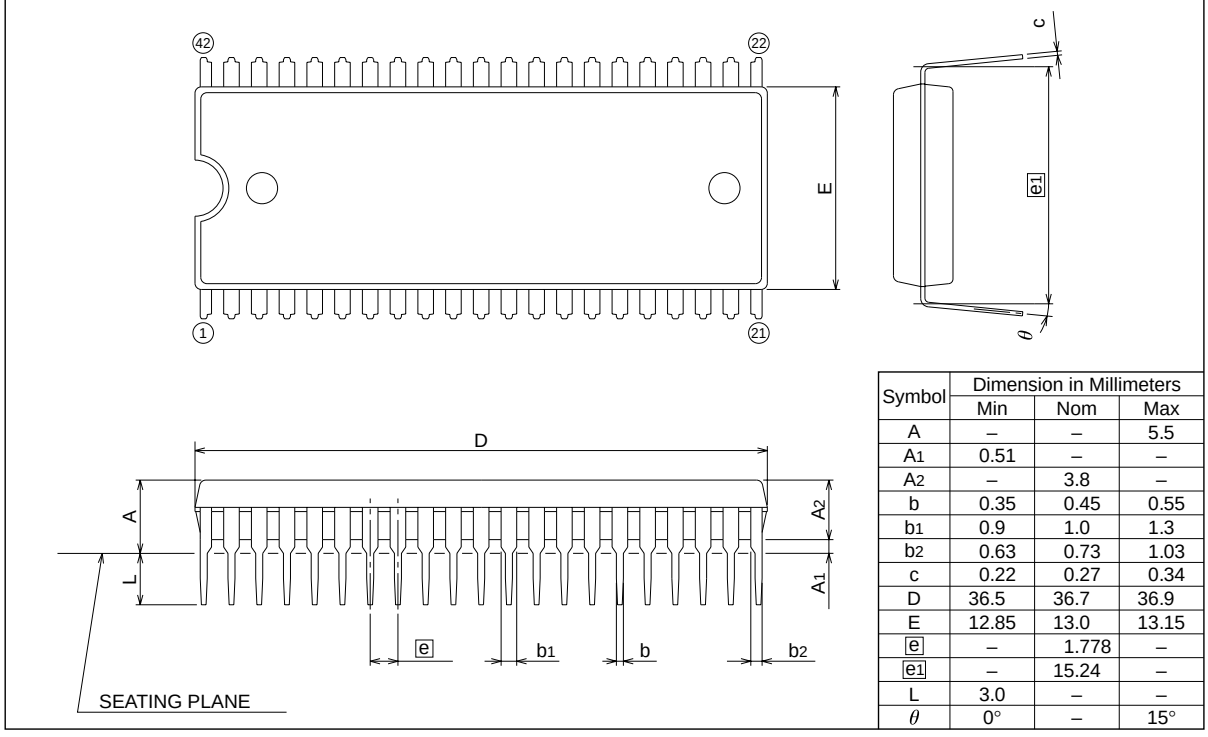


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A1	0.05	–	–
A2	–	2.0	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	0.8	–
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	–	1.765	–
z	–	0.75	–
Z1	–	–	0.9
y	–	–	0.15
θ	0°	–	10°
b2	–	0.5	–
e1	–	11.43	–
l2	1.27	–	–

42P4B

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	–	4.1	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A1	0.51	–	–
A2	–	3.8	–
b	0.35	0.45	0.55
b1	0.9	1.0	1.3
b2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	–	1.778	–
e1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

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MITSUBISHI MICROCOMPUTERS

3851 Group

(Built-in 16 KB ROM)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

Renesas Technology Corp.
Nippon Bldg.,6-2,Otemachi 2-chome,Chiyoda-ku,Tokyo,100-0004 Japan

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REVISION HISTORY	3851 GROUP (built-in 16 KB ROM) DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.0	05/15/98		First Edition
1.1	07/26/02		Group name is changed.
		1	Figure 1 is partly revised.
		3	Table 1 is partly added.
		4	Figure 3 is partly revised.
		7	Figure 6 is partly revised.
		10	Figure 8 is partly revised.
		11	■Notes is revised.
		13	Figure 10 is partly revised.
		18	"2" of ■Notes on Serial I/O is added.
		20	Figure 19 is partly revised.
		21	Explanations of "[I^2C Address Register (S0D)]" is partly revised.
		24	Explanations of "•Bit 2: Slave address comparison flag (AAS)" of "[I^2C Status Register (S1)]" is partly revised.
		26	Figure name of Figure 28 is revised.
		26	Table 8 is partly revised.
		31	Explanations of "Data Setting" are partly revised.
		31	Figure 32 is partly revised.
		33	Explanations of "Comparator and Control Circuit" is partly eliminated.
		35	Explanations of "RESET CIRCUIT" is partly revised.
		35	Figure 42 is partly revised.
		36	Figure 43 is partly revised.
		37	Explanations of "CLOCK GENERATING CIRCUIT" are partly added.
		37	Explanations of "(1) Middle-speed mode" are partly revised.
		38	Figure 47 is partly revised.
		39	Figure 49 is partly revised.
		40	Explanations of "A-D Converter" of "NOTES ON PROGRAMMING" are partly revised.
		40	"NOTES ON USAGE" is added.
		41	Explanations of "DATA REQUIRED FOR ROM WRITING ORDERS" are partly added.
		42	Table 11 is partly revised.
		44	Table 14 is partly revised.
		47	Table 17 is partly revised.
		47	Table 18 is partly revised.
		52	PACKAGE OUTLINE is partly revised.
			Pages 52–58 in Rev.1.0 are eliminated.

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