

Silicon Carbide (SiC) MOSFET – EliteSiC, 32 mohm, 650 V, M3S, TOLL NTBL032N065M3S

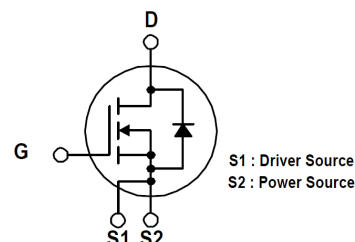
Features

- Typical $R_{DS(on)} = 32\text{ m}\Omega$ @ $V_{GS} = 18\text{ V}$
- Ultra Low Gate Charge ($Q_{G(tot)} = 55\text{ nC}$)
- High Speed Switching with Low Capacitance ($C_{oss} = 113\text{ pF}$)
- 100% Avalanche Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

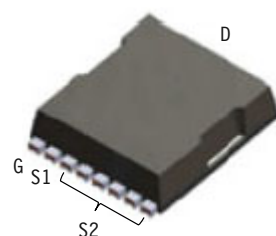
Applications

- SMPS (Switching Mode Power Supplies)
- Solar Inverters
- UPS (Uninterruptable Power Supplies)
- Energy Storage
- EV Charging Infrastructure

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ TYP}$	$I_D\text{ MAX}$
650 V	32 m Ω @ 18 V	55 A

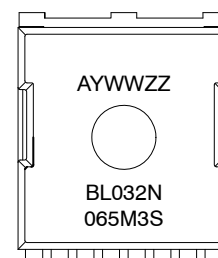


N-Channel MOSFET



H-PSOF8L
CASE 100DC

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
ZZ	= Assembly Lot Code
BL032N065M3S	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

NTBL032N065M3S

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	650	V
Gate-to-Source Voltage	V _{GS}	-8/+22	V
Continuous Drain Current	I _D	55	A
Power Dissipation			
Continuous Drain Current	I _D	39	A
Power Dissipation			
Pulsed Drain Current (Note 1)	I _{DM}	192	A
Continuous Source-Drain Current (Body Diode)	I _S	33	A
		19	
Pulsed Source-Drain Current (Body Diode) (Note 1)	I _{SM}	173	A
Single Pulse Avalanche Energy (I _{LPK} = 16.7 A, L = 1 mH) (Note 2)	E _{AS}	139	mJ
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Lead Temperature for Soldering Purposes (1/8" from Case for 10 s)	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating, limited by max junction temperature.
2. E_{AS} of 139 mJ is based on starting T_J = 25°C, L = 1 mH, I_{AS} = 16.7 A, V_{DD} = 100 V, V_{GS} = 18 V.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 3)	R _{θJC}	0.66	°C/W
Thermal Resistance, Junction-to-Ambient (Note 3)	R _{θJA}	43	°C/W

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operation Values of Gate-to-Source Voltage	V _{GSop}	-5...-3/+18	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NTBL032N065M3S

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	650			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV _{(BR)DSS} /ΔT _J	I _D = 1 mA, Referenced to 25°C		90		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 650 V, T _J = 25°C			10	μA
		V _{DS} = 650 V, T _J = 175°C (Note 5)			500	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = -8/+22 V, V _{DS} = 0 V			±1	μA

ON CHARACTERISTICS

Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 18 V, I _D = 15 A, T _J = 25°C		32	44	mΩ
		V _{GS} = 18 V, I _D = 15 A, T _J = 175°C (Note 5)		47		
		V _{GS} = 15 V, I _D = 15 A, T _J = 25°C		41		
		V _{GS} = 15 V, I _D = 15 A, T _J = 175°C (Note 5)		52		
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 7.5 mA	2.0	2.9	4.0	V
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 15 A		9.9		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 400 V (Note 5)		1396		pF
Output Capacitance	C _{OSS}			113		
Reverse Transfer Capacitance	C _{RSS}			8.9		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -3/18 V, V _{DD} = 400 V, I _D = 15 A (Note 5)		55		nC
Gate-to-Source Charge	Q _{GS}			15		
Gate-to-Drain Charge	Q _{GD}			14		
Gate-Resistance	R _G	f = 1 MHz		5.0		Ω

SWITCHING CHARACTERISTICS

Turn-On Delay Time	t _{d(ON)}	V _{GS} = -3/18 V, V _{DD} = 400 V, I _D = 15 A, R _G = 4.7 Ω, T _J = 25°C (Notes 4, 5)		8.8		ns
Turn-Off Delay Time	t _{d(OFF)}			31		
Rise Time	t _r			12		
Fall Time	t _f			9		
Turn-On Switching Loss	E _{ON}			33		μJ
Turn-Off Switching Loss	E _{OFF}	V _{GS} = -3/18 V, V _{DD} = 400 V, I _D = 15 A, R _G = 4.7 Ω, T _J = 175°C (Notes 4, 5)		16		
Total Switching Loss	E _{TOT}			49		
Turn-On Delay Time	t _{d(ON)}			7.8		ns
Turn-Off Delay Time	t _{d(OFF)}			37		
Rise Time	t _r			12		
Fall Time	t _f			11		
Turn-On Switching Loss	E _{ON}			31		μJ
Turn-Off Switching Loss	E _{OFF}			25		
Total Switching Loss	E _{TOT}			56		

SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = -3 V, I _{SD} = 15 A, T _J = 25°C		4.5	6.0	V
		V _{GS} = -3 V, I _{SD} = 15 A, T _J = 175°C		4.2		

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Reverse Recovery Time	t _{RR}	V _{GS} = -3 V, I _S = 15 A, dI/dt = 1000 A/μs, V _{DS} = 400 V (Note 5)		15.5		ns
Charge Time	t _a			8.9		
Discharge Time	t _b			6.6		
Reverse Recovery Charge	Q _{RR}			72		nC
Reverse Recovery Energy	E _{REC}			4.6		μJ
Peak Reverse Recovery Current	I _{RRM}			9.3		A

4. EON/EOFF result is with body diode.

5. Defined by design, not subject to production test.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



TYPICAL CHARACTERISTICS

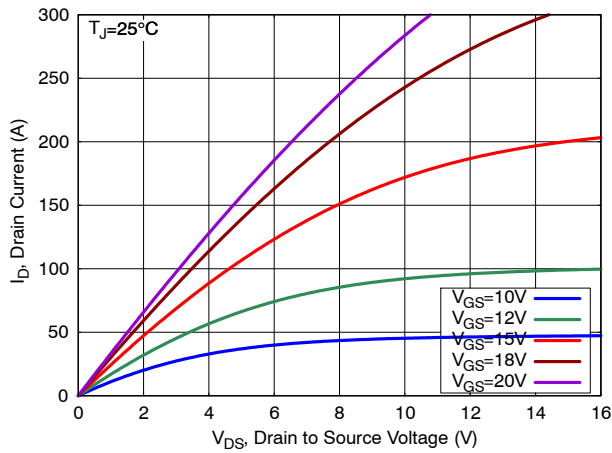


Figure 1. Output Characteristics

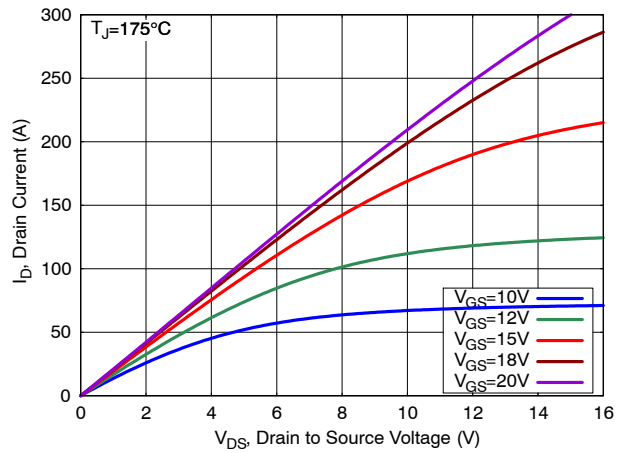


Figure 2. Output Characteristics

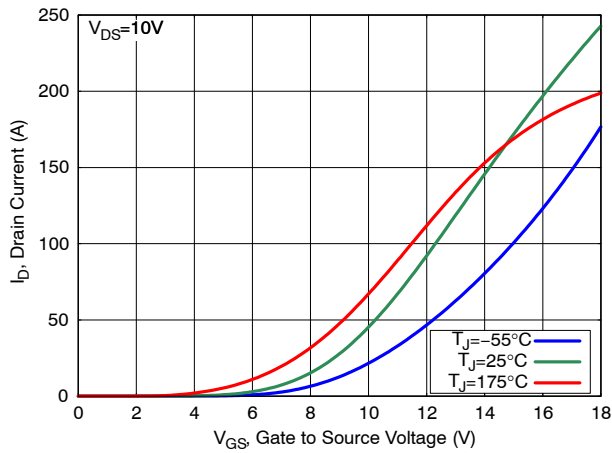


Figure 3. Transfer Characteristics

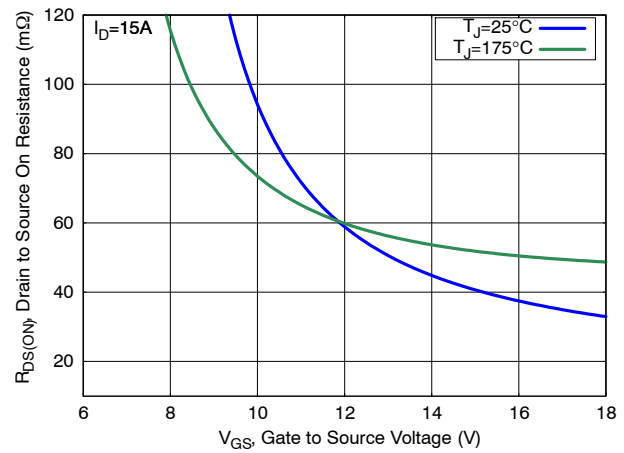


Figure 4. On-Resistance vs. Gate Voltage

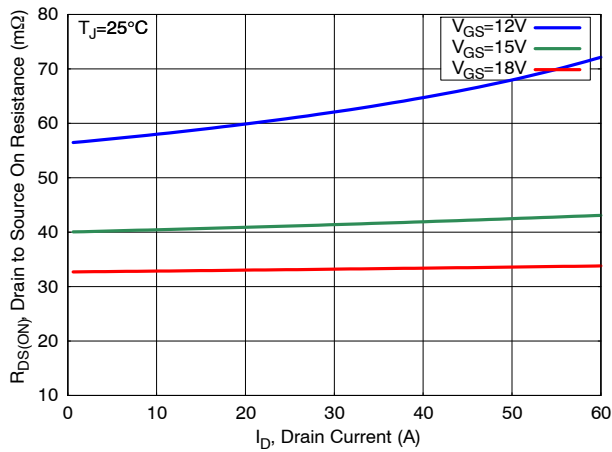


Figure 5. On-Resistance vs. Drain Current

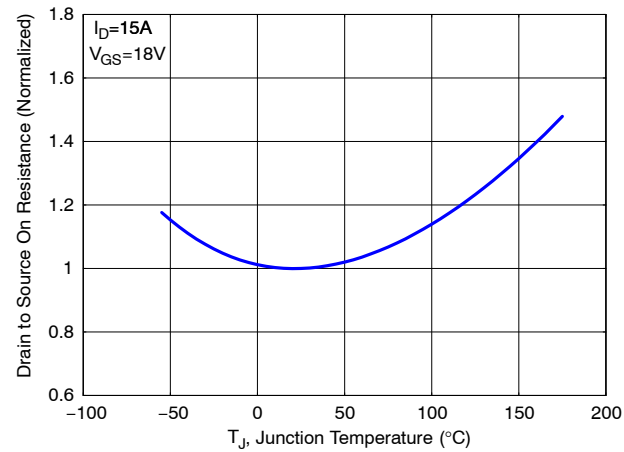


Figure 6. On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

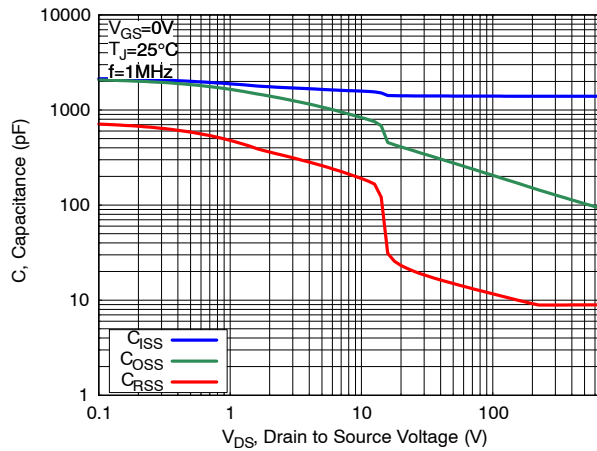


Figure 7. Capacitance Characteristics

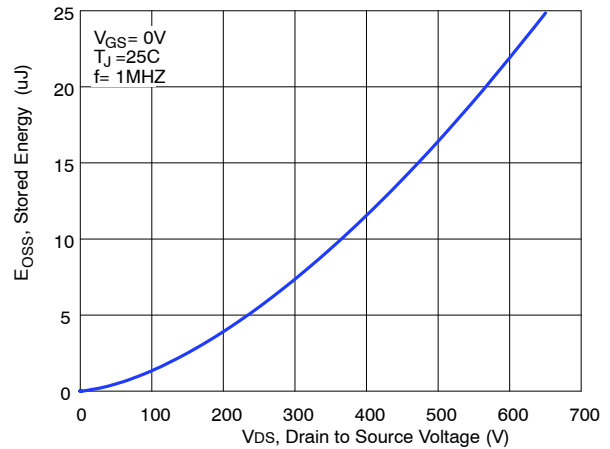


Figure 8. Stored Energy vs. Drain-to-Source Voltage

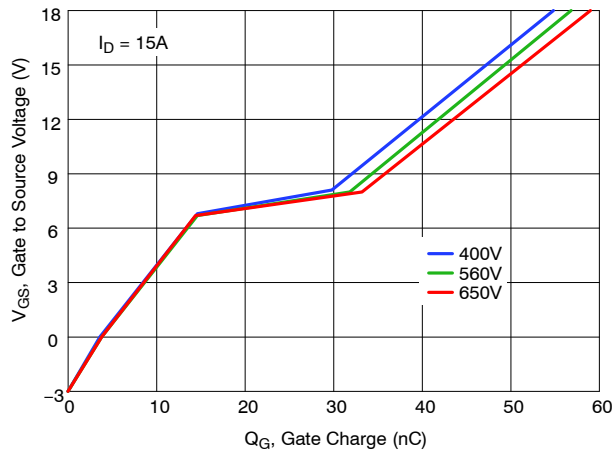


Figure 9. Gate Charge Characteristics

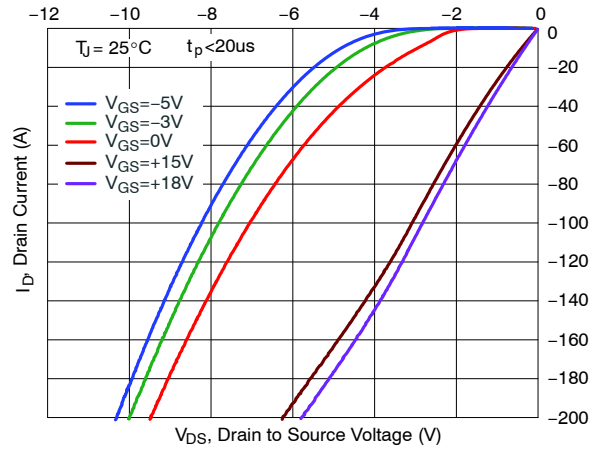


Figure 10. Reverse Conduction Characteristics

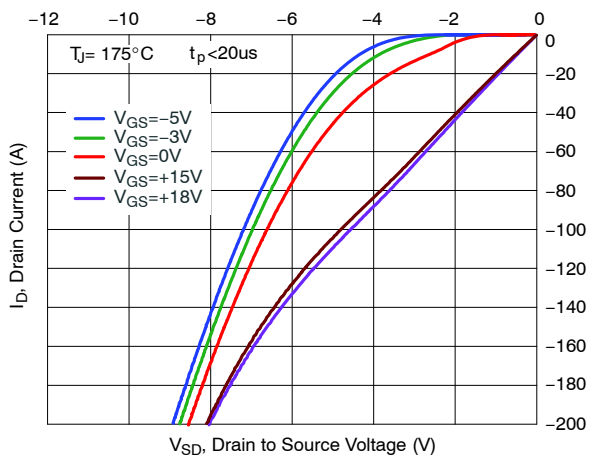


Figure 11. Reverse Conduction Characteristics

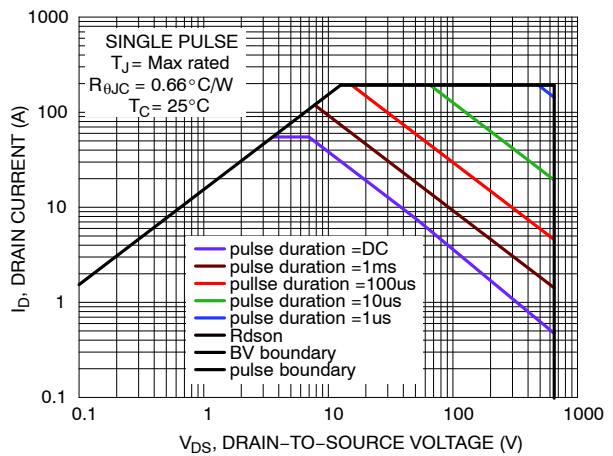


Figure 12. Safe Operating Area

TYPICAL CHARACTERISTICS

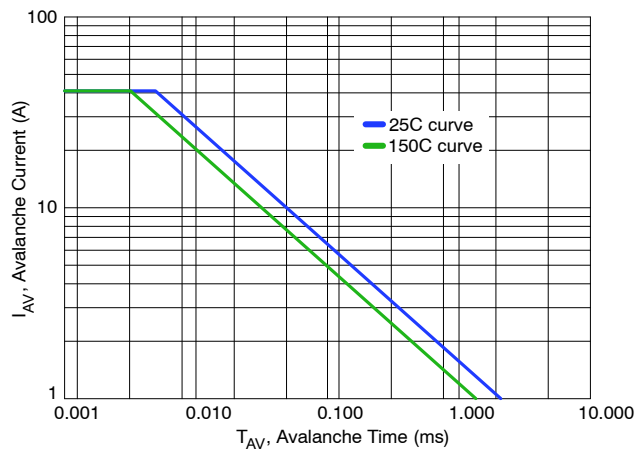


Figure 13. Avalanche Current vs. Pulse Time (UIS)

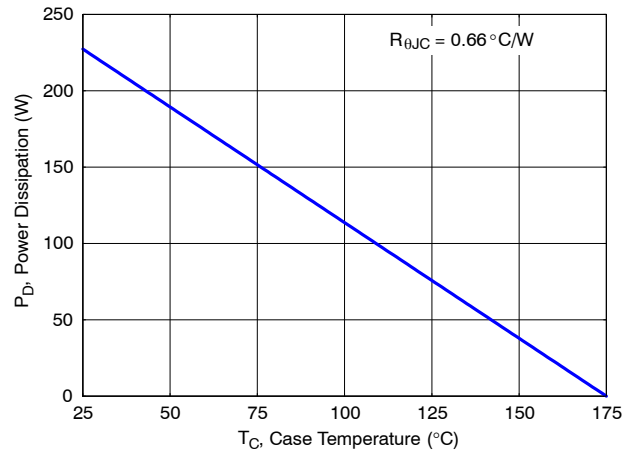


Figure 14. Maximum Power Dissipation vs. Case Temperature

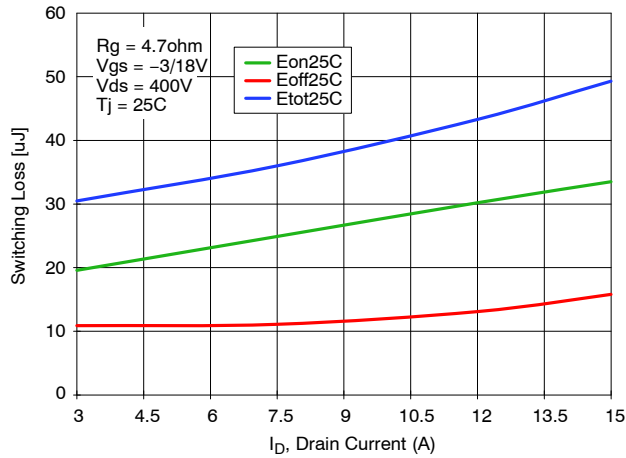


Figure 15. Inductive Switching Loss vs. Drain Current

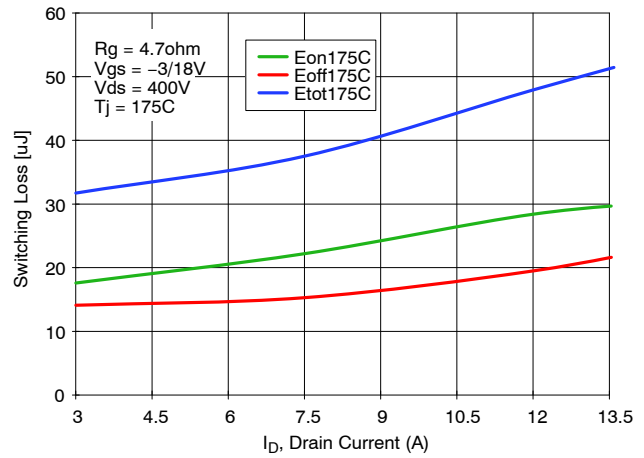


Figure 16. Inductive Switching Loss vs. Drain Current

TYPICAL CHARACTERISTICS

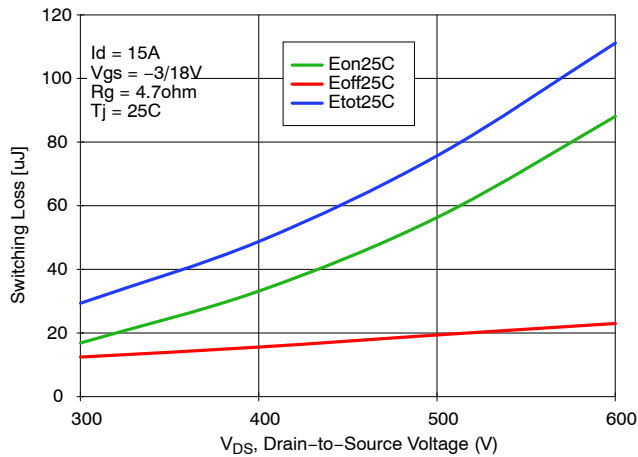


Figure 17. Inductive Switching Loss vs. Drain Voltage

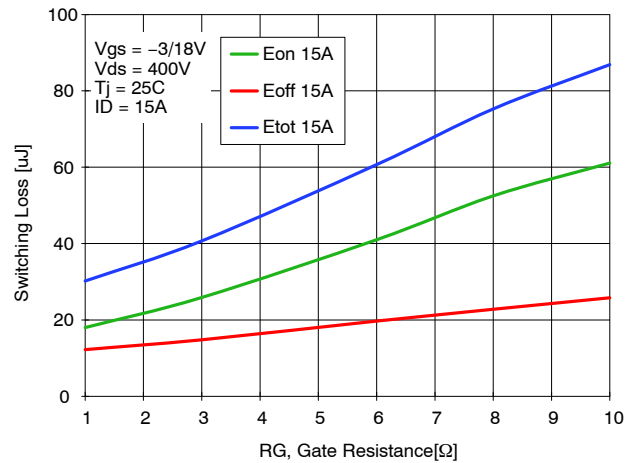


Figure 18. Inductive Switching Loss vs. Gate Resistance

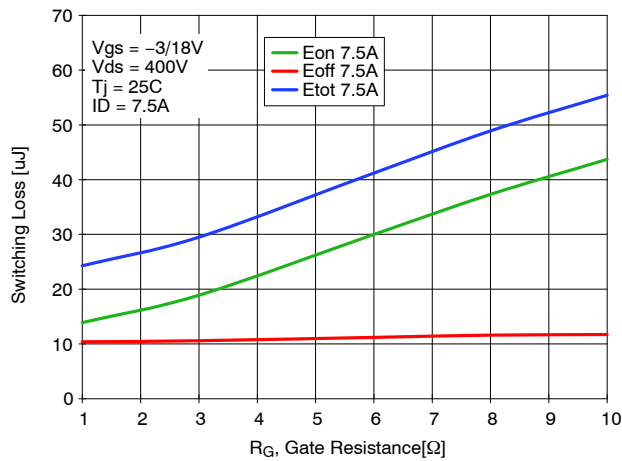


Figure 19. Inductive Switching Loss vs. Gate Resistance

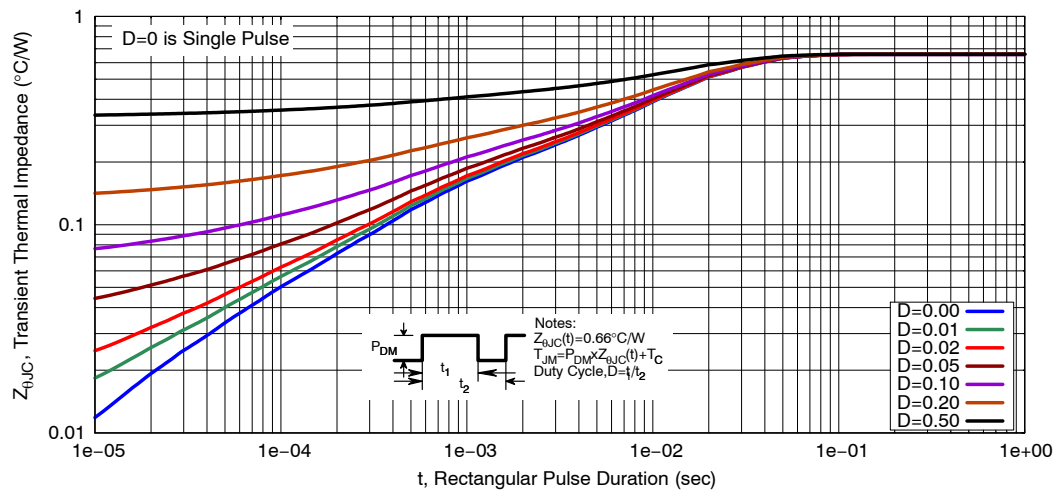


Figure 20. Thermal Response Characteristics

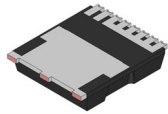
NTBL032N065M3S

DEVICE ORDERING INFORMATION

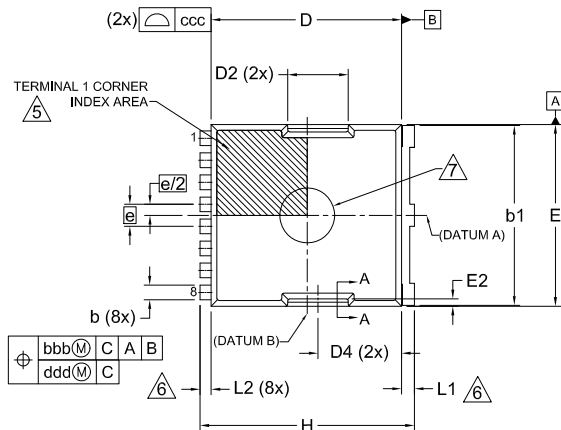
Device	Package	Shipping [†]
NTBL032N065M3S	H-PSOF8L	2000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

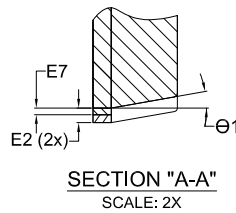
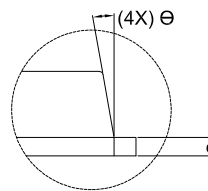
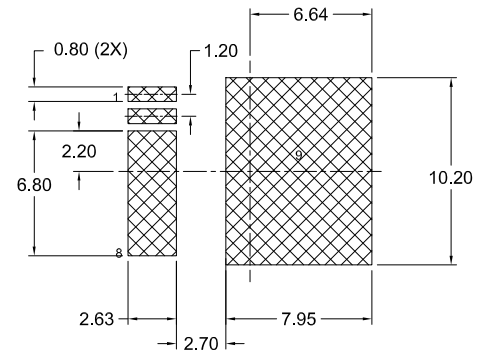



H-PSOF8L 9.90x10.38x2.30, 1.20P
CASE 100DC
ISSUE D

DATE 30 JUL 2024



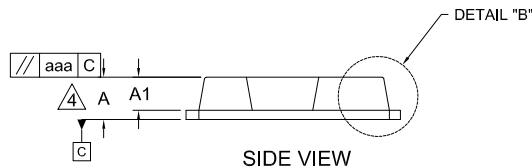
TOP VIEW


SECTION "A-A"
SCALE: 2X

DETAIL "B"
SCALE: 2X

LAND PATTERN
RECOMMENDATION

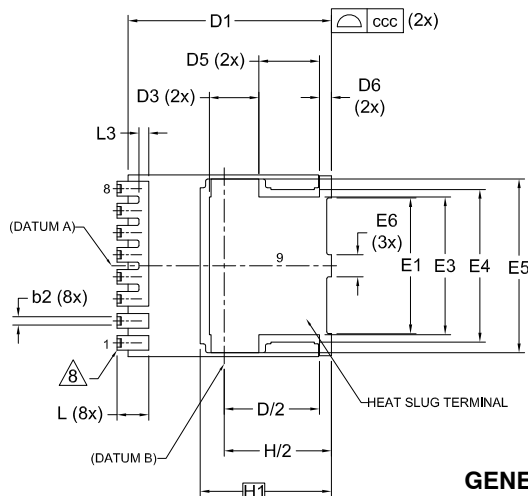
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.



SIDE VIEW



BOTTOM VIEW

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.63	1.73	1.83
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.43	0.53	0.63
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

DOCUMENT NUMBER: 98AON80466G

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DESCRIPTION: H-PSOF8L 9.90x10.38x2.30, 1.20P

PAGE 1 OF 1

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