CY23FS04

Failsafe™ 2.5 V/3.3 V Zero Delay Buffer

Features

- Internal digital controlled crystal oscillator (DCXO) for continuous glitch-free operation
- Zero input-output propagation delay
- Low jitter (35 ps max RMS) outputs
- Low output-to-output skew (200 ps max)
- 4.17 MHz to 166.7 MHz reference input
- Supports industry standard input crystals
- 166.7 MHz outputs
- 5 V tolerant Inputs
- Phase-locked loop (PLL) bypass mode
- Dual reference inputs
- 16-Pin thin shrunk small outline package (TSSOP)
- 2.5 V or 3.3 V output power supplies
- 3.3 V core power supply
- Industrial temperature range

Functional Description

The CY23FS04 is a FailSafe™ zero delay buffer with two reference clock inputs and four phase-aligned outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure.

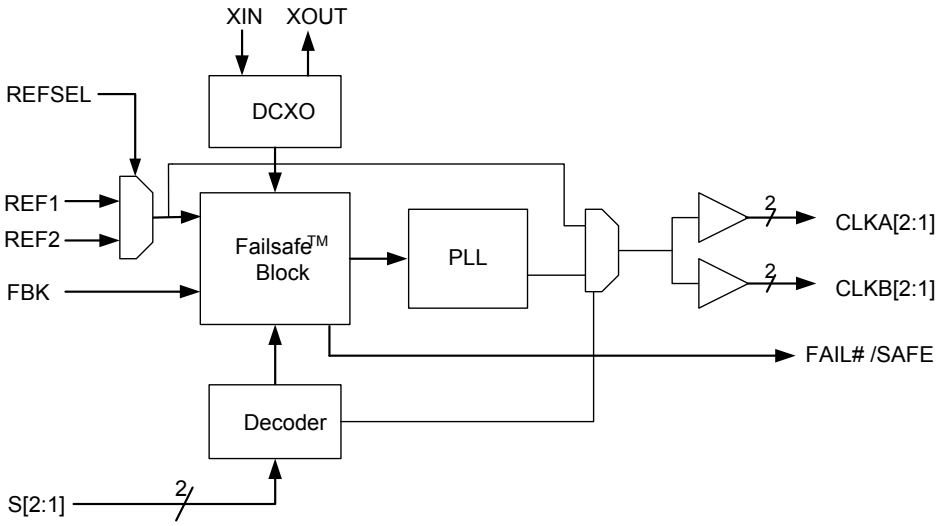
The continuous, glitch-free operation is achieved by using a DCXO. This serves as a redundant clock source in the event of a reference clock failure by maintaining the last frequency and phase information of the reference clock.

The unique feature of the CY23FS04 is that the DCXO is the primary clocking source, which is synchronized (phase-aligned) to the external reference clock. When this external clock is restored, the DCXO automatically resynchronizes to the external clock.

The frequency of the crystal that is connected to the DCXO must be an integer factor of the frequency of the reference clock. This factor is set by two select lines: S[2:1], see Configuration Table on page 3. The output power supply V_{DD} can be connected to either 2.5 V or 3.3 V. VDDC is the power supply pin for internal circuits and must be connected to 3.3 V.

For a complete list of related documentation, click here.

Logic Block Diagram



Downloaded from Arrow.com.

Contents

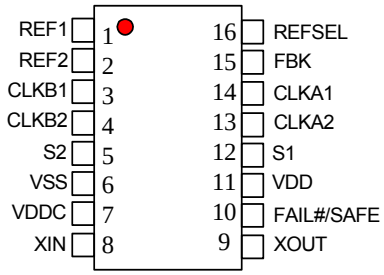
Pin Configuration **3**
Pin Definitions **3**
Configuration Table **3**
FailSafe Function **4**
XTAL Selection Criteria and Application Example **6**
Absolute Maximum Conditions **8**
Recommended Pullable Crystal Specifications **8**
Operating Conditions **9**
Electrical Characteristics **9**
Thermal Resistance **9**
Switching Characteristics **10**
Switching Waveforms **11**
Ordering Information **12**
Ordering Code Definitions 12
Package Diagram **13**
Acronyms **14**
Document Conventions **14**
Units of Measure 14
Document History Page **15**
Sales, Solutions, and Legal Information **16**
Worldwide Sales and Design Support 16
Products 16
PSoC®Solutions 16
Cypress Developer Community 16
Technical Support 16

Downloaded from Arrow.com.

Pin Configuration

Figure 1. 16-pin TSSOP pinout

CY23FS04



Pin Definitions

Pin No.	Pin Name	Description
2, 1	REF[2:1]	Reference clock inputs. 5 V tolerant.[4]
4, 3	CLKB[2:1]	Bank B clock outputs.[1,2]
13, 14	CLKA[2:1]	Bank A clock outputs.[1,2]
15	FBK	Feedback input to the PLL.[1,4]
5, 12	S[2:1]	Frequency select pins and PLL and DCXO bypass mode.[3]
8	XIN	Reference crystal input.
9	XOUT	Reference crystal output.
10	FAIL#/SAFE	Valid reference indicator. A high level indicates a valid reference input.
11	VDD	2.5 V or 3.3 V power supply.
7	VDDC	3.3 V power supply.
6	VSS	Ground.
16	REFSEL	Reference select. Selects the active reference clock from either REF1 or REF2. REFSEL = 1, REF1 is selected; REFSEL = 0, REF2 is selected.

Configuration Table

S[2:1]	XTAL (MHz)		REF (MHz)		OUT (MHz)		REF:OUT Ratio	REF:XTAL Ratio	Out:XTAL Ratio
	Min	Max	Min	Max	Min	Max			
00			PLL and DCXO Bypass Mode						
01	8.33	30.00	4.17	15.00	4.17	15.00	x1	1/2	1/2
10	8.00	25.00	16.00	50.00	16.00	50.00	x1	2	2
11	8.33	27.78	50.00	166.70	50.00	166.70	x1	6	6

Notes
1. For normal operation, connect either one of the four clock outputs to the FBK input.
2. Weak pull-downs on all outputs.
3. Weak pull-ups on these inputs.
4. Weak pull-down on these inputs

Downloaded from Arrow.com.

FailSafe Function

The CY23FS04 is targeted at clock distribution applications that require continued operation should the main reference clock fail. Existing approaches to this requirement have used multiple reference clocks with either internal or external methods to switch between references. The problem with this technique is that it leads to interruptions (or glitches) when transitioning from one reference to another, often requiring complex external circuitry or software to maintain system stability. The technique implemented in this design completely eliminates any switching of references to the PLL, greatly simplifying system design.

The CY23FS04 PLL is driven by the crystal oscillator, which is phase-aligned to an external reference clock so that the output of the device is effectively phase-aligned to the reference via the external feedback loop. This is accomplished by using a digitally controlled capacitor array to pull the crystal frequency over an approximate range of ±300 ppm from its nominal frequency.

In this mode, if the reference frequency fails (stop or disappear), the DCXO maintains its last setting and a flag signal (FAIL#/SAFE) is set to indicate failure of the reference clock.

The CY23FS04 provides two select bits, S1 and S2, to control the reference-to-crystal frequency ratio. The DCXO is internally tuned to the phase and frequency of the external reference only when the reference frequency divided by this ratio is within the DCXO capture range. If the frequency is out of range, a flag is set on the FAIL#/SAFE pin notifying the system that the selected reference is not valid. If the reference moves in range, then the flag is cleared, indicating to the system that the selected reference is valid.

Figure 2. Fail#/Safe Timing for Input Reference Failing Catastrophically

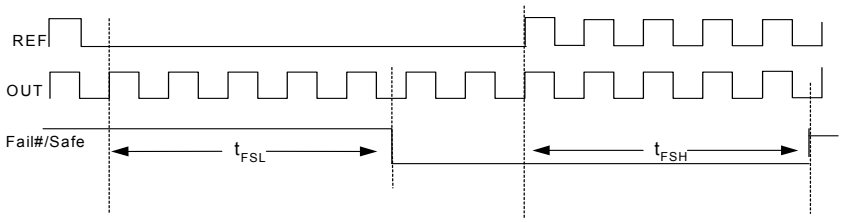


Figure 3. Fail#/Safe Timing Formula

$$t_{FSL(max)} = 2 (t_{REF} \times n) + 25ns$$

$$n = \frac{F_{REF}}{F_{XTAL}} = 4 \text{ (in above example)}$$

$$t_{FSH(min)} = 12 (t_{REF} \times n) + 25ns$$

Table 1. FailSafe Timing Table

Parameter	Description	Conditions	Min	Max	Unit
t_{FSL}	Fail#/safe assert delay	Measured at 80% to 20%, Load = 15 pF	–	See Figure 3 on page 4	ns
t_{FSH}	Fail#/safe assert delay	Measured at 80% to 20%, Load = 15 pF	See Figure 3 on page 4	–	ns

Downloaded from Arrow.com.

Figure 4. FailSafe Timing Diagram: Input Reference Slowly Drifting Out of FailSafe Capture Range

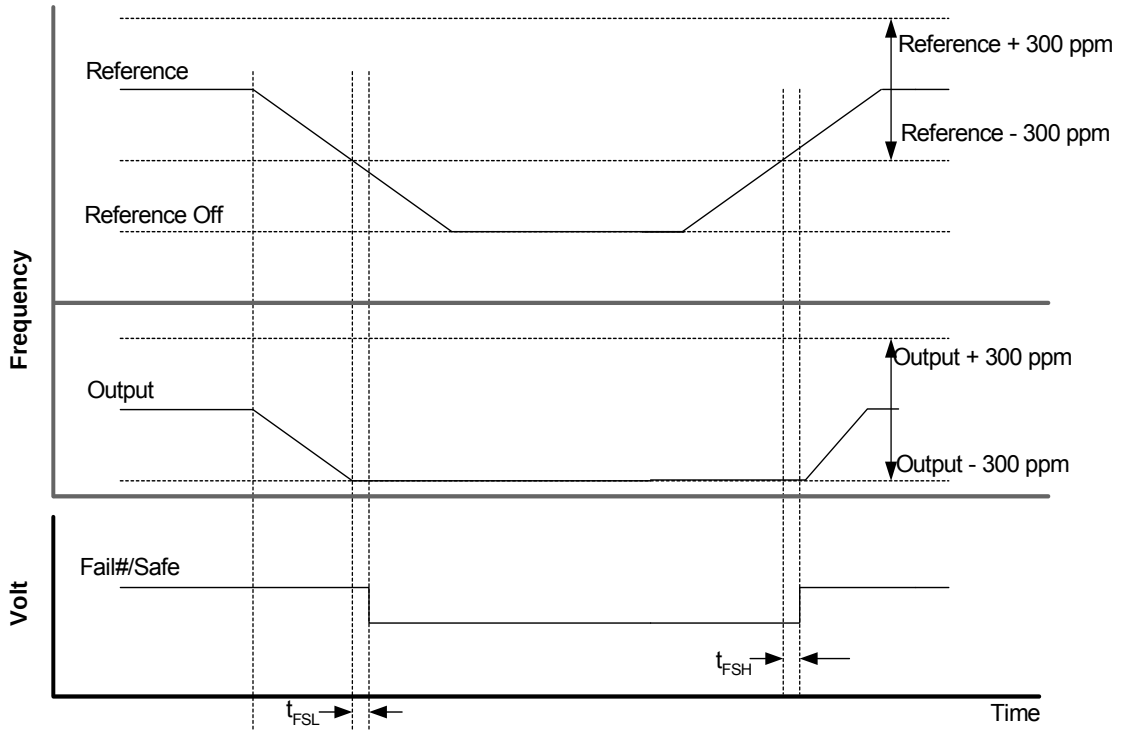
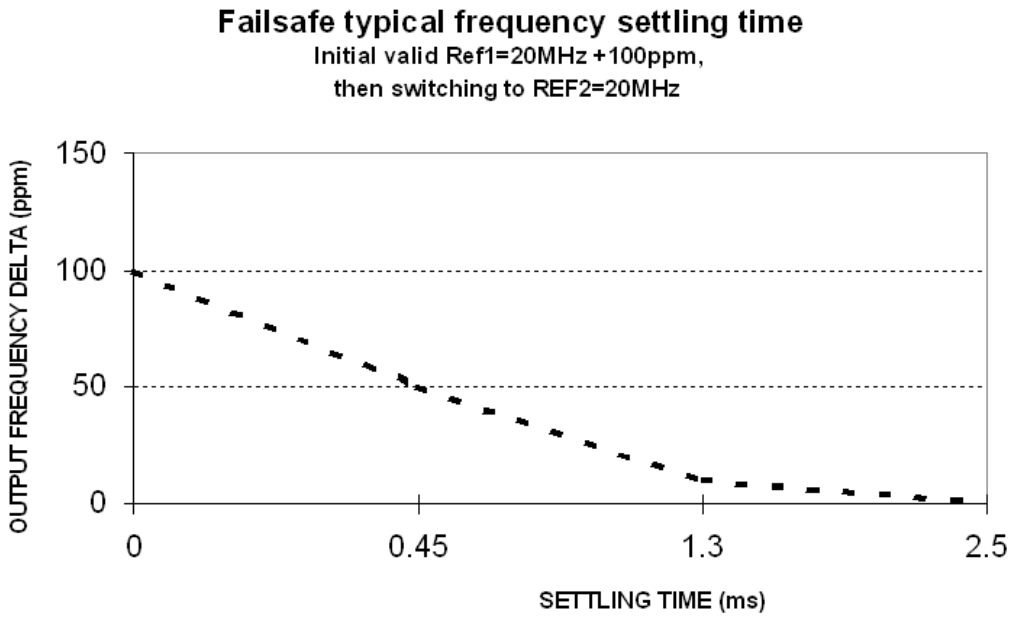


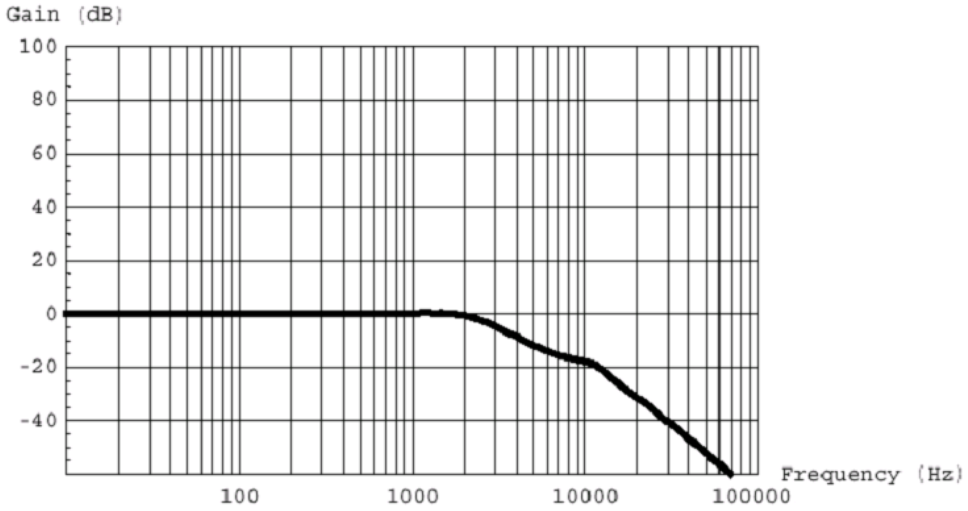
Figure 5. FailSafe Reference Switching Behavior



Downloaded from Arrow.com.

Because of the DCXO architecture, the CY23FS04 has a much lower bandwidth than a typical PLL-based clock generator. This is shown in Figure 6. This low bandwidth makes the CY23FS04 also useful as a jitter attenuator. The loop bandwidth curve is also known as the jitter transfer curve.

Figure 6. FailSafe Effective Loop Bandwidth (min)



XTAL Selection Criteria and Application Example

Choosing the appropriate XTAL ensures the FailSafe device is able to span an appropriate frequency of operation. Also, the XTAL parameters determine the holdover frequency stability. Critical parameters are given here. Cypress recommends that you choose:

- Low C0/C1 ratio (240 or less) so that the XTAL has enough range of pullability
- Low temperature frequency variation
- Low manufacturing frequency tolerance
- Low aging

C0 is the XTAL shunt capacitance (3 pF to 7 pF typ).

C1 is the XTAL motional capacitance (10 fF to 30 fF typ).

The capacitive load as “seen” by the XTAL is across its terminals. It is named $C_{LOADMIN}$ (for minimum value), and $C_{LOADMAX}$ (for maximum value).These are used to calculate the pull range.

Note that the C_{LOAD} range “center” is approximately 20 pF, but you may not want a XTAL calibrated to that load. This is because the pullability is not linear, as represented in the equation. Plotting the pullability of the XTAL shows this expected behavior as shown in Figure 7 on page 7. In this example, specifying a XTAL calibrated to 16 pF load provides a balanced ppm pullability range around the nominal frequency.

Example

$C_{LOADMIN}$ = (12 pF IC input cap + 0 pF pulling cap + 6 pF trace cap on board) / 2 = 9 pF

$C_{LOADMAX}$ = (12 pF IC input cap + 48 pF pulling cap + 6 pF trace cap on board) / 2 = 33 pF

Pull Range = $(fC_{LOADMIN} – fC_{LOADMAX}) / fC_{LOADMIN} = (C1 / 2) * [(1 / (C0 + C_{LOADMIN})) – (1 / (C0 + C_{LOADMAX}))]$

Pull Range in ppm = $(C1 / 2) * [(1 / (C0 + C_{LOADMIN})) – (1 / (C0 + C_{LOADMAX}))] * 10^6$

Downloaded from Arrow.com.

Figure 7. Frequency vs. C_{LOAD} Behavior for Example XTAL

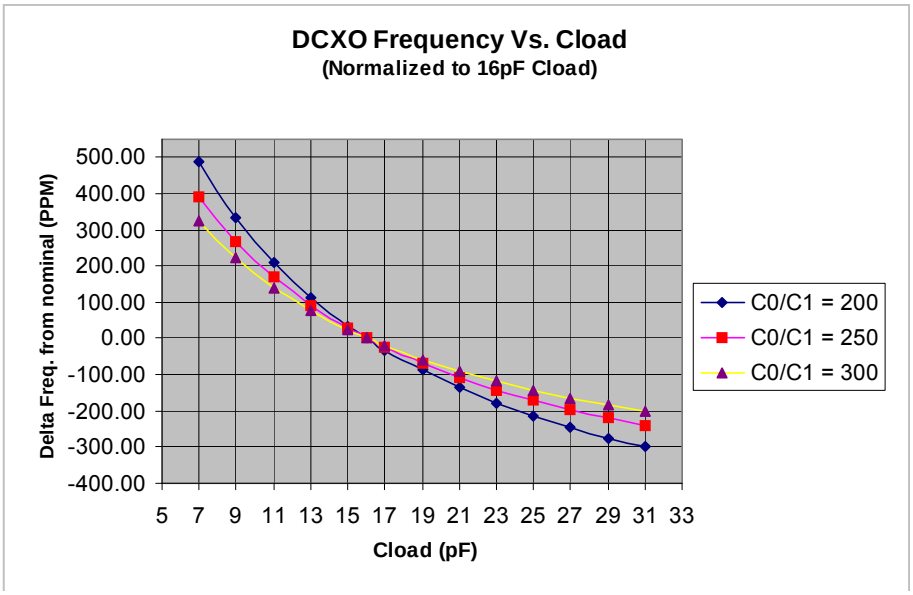


Table 2. Pullability Range from XTAL with Different C_0/C_1 Ratio

C_L	Calculated Pull Range in ppm, (Normalized)		
(pF)	C_0/C_1 = 200	C_0/C_1 = 250	C_0/C_1 = 300
7	489.13	391.30	326.09
9	332.88	266.30	221.92
11	211.35	169.08	140.90
13	114.13	91.30	76.09
15	34.58	27.67	23.06
16	0.00	0.00	0.00
17	–31.70	–25.36	–21.14
19	–87.79	–70.23	–58.53
21	–135.87	–108.70	–90.58
23	–177.54	–142.03	–118.36
25	–213.99	–171.20	–142.66
27	–246.16	–196.93	–164.11
29	–274.76	–219.81	–183.17
31	–300.34	–240.27	–200.23

Calculated value of the pullability range for the XTAL with C_0/C_1 ratio of 200, 250, and 300 are shown in Table 2 on page 7. For this calculation, $C_{LOADMIN}$ = 7 pF and C_{LOAD}(max)= 31 pF is used. Using a XTAL that has a nominal frequency specified at load capacitance of 16 pF, almost symmetrical pullability range is obtained.

Next, it is important to calculate the pullability range including error tolerances. This is the capture range of the input reference frequency that the FailSafe device and XTAL combination can reliably span.

Calculating the capture range involves subtracting error tolerances as follows:

Parameter.....f error (ppm)

Manufacturing frequency tolerance 15

Temperature stability 30

Aging 3

Board/trace variation 5

Total 53

Example: Capture range for XTAL with C0/C1 Ratio of 200

Negative Capture range = –300 ppm + 53 ppm = –247 ppm

Positive Capture range = 489 ppm – 53 ppm = +436 ppm

It is important to note that the XTAL with lower C_0/C_1 ratio has wider pullability/capture range as compared to the higher C_0/C_1 ratio. This helps to select the appropriate XTAL for use in the FailSafe application.

Important Notes

Following are some important notes that should be considered when designing with the failsafe device:

1. The trace capacitance of the XTAL inputs, XIN and XOUT must be kept as small as possible.

2. Specify the DCXO for C_0/C_1 ratio to be less than 250 and the XTAL Load Capacitance to be approximately 16 pF. A typical DCXO specification from Ecliptek is attached here (please see page 6) for reference.

3. XTAL with low temperature frequency variation, low manufacturing frequency tolerance and low aging must be chosen.

4. Pull range must be checked for its upper and lower frequency symmetry from the nominal value as described in this application note.

Downloaded from Arrow.com.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply voltage	–	–0.5	4.6	V
V_{IN}	Input voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	temperature, storage	Non functional	–65	150	°C
T_J	temperature, junction	Functional	–	125	°C
ESD_{HBM}	ESD protection (human body model)	MIL-STD-883, Method 3015	2000	–	V
UL–94	Flammability rating	At 1/8 in.	V–0		
MSL	Moisture sensitivity level	–	3		
Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.					

Recommended Pullable Crystal Specifications

Parameter [5]	Description	Comments	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	8.00	–	30.00	MHz
$C_{LOADNOM}$	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW
F_{3SEPLI}	Third overtone separation from $3*F_{NOM}$	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from $3*F_{NOM}$	Low side	–	–	–150	ppm
C0	Crystal shunt capacitance	–	–	–	7	pF
C0 / C1	Ratio of shunt to motional capacitance	–	180	–	250	
C1	Crystal motional capacitance	–	14.4	18	21.6	fF

Note
5. Ecliptek ECX-5788-13.500M, ECX-5807-19.440M, ECX-5872-19.53125M, ECX-6362-18.432M, ECX-5808-27.000M, ECX-5884-17.664M, ECX-5883-16.384M, ECX-5882-19.200M, ECX-5880-24.576M meet these specifications.

Downloaded from Arrow.com.

Operating Conditions

For FailSafe Devices

Parameter	Description	Min	Max	Unit
V_{DDC}	3.3 V supply voltage	3.135	3.465	V
V_{DD}	2.5 V supply voltage range	2.375	2.625	V
	3.3 V supply voltage range	3.135	3.465	V
T_A	Ambient operating temperature, Commercial	0	70	°C
	Ambient operating temperature, Industrial	–40	85	°C
C_L	Output load capacitance (Fout ≤ 100 MHz)	–	30	pF
	Output load capacitance (Fout > 100 MHz)	–	15	pF
C_{IN}	Input capacitance (except XIN)	–	7	pF
C_{XIN}	Crystal input capacitance (all internal caps off)	10	13	pF
T_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

Electrical Characteristics

For FailSafe Devices

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low voltage	CMOS Levels, 30% of V_{DD}	–	–	0.3 × V_{DD}	V
V_{IH}	Input high voltage	CMOS Levels, 70% of V_{DD}	0.7 × V_{DD}	–		V
I_{IL}	Input low current	V_{IN} = V_{SS} (100k pull up only)	–	–	50	µA
I_{IH}	Input high current	V_{IN} = V_{DD} (100k pull down only)	–	–	50	µA
I_{OL}	Output low current	V_{OL} = 0.5 V, V_{DD} = 2.5 V	–	18	–	mA
		V_{OL} = 0.5 V, V_{DD} = 3.3 V	–	20	–	mA
I_{OH}	Output high current	V_{OH} = V_{DD} – 0.5 V, V_{DD} = 2.5 V	–	18	–	mA
		V_{OH} = V_{DD} – 0.5 V, V_{DD} = 3.3 V	–	20	–	mA
I_{DDQ}	Quiescent current	All inputs grounded, PLL and DCXO in bypass mode, Reference Input = 0	–	–	250	µA

Thermal Resistance

Parameter [6]	Description	Test Conditions	16-pin TSSOP	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	89	°C/W
θ_{JC}	Thermal resistance (junction to case)		12	°C/W

Note
6. These parameters are guaranteed by design and are not tested.

Downloaded from Arrow.com.

Switching Characteristics

For FailSafe Devices

Parameter[8]	Description	Test Conditions	Min	Max	Unit
f_{REF}	Reference frequency	Commercial/Industrial Grades	4.17	166.7	MHz
f_{OUT}	Output frequency	15 pF Load, Commercial/Industrial Grades	4.17	166.7	MHz
f_{XIN}	DCXO frequency		8.0	30	MHz
t_{DC}	Duty cycle	Measured at $V_{DD}/2$	47	53	%
$t_{SR(I)}$	Input slew rate	Measured on REF1 Input, 30% to 70% of V_{DD}	0.5	4.0	V/ns
$t_{SR(O)}$	Output slew rate	Measured from 20% to 80% of V_{DD} = 3.3 V, 15 pF Load	0.8	4.0	V/ns
		Measured from 20% to 80% of V_{DD} = 2.5 V, 15 pF Load	0.4	3.0	V/ns
$t_{SK(O)}$	Output-to-output skew	All outputs equally loaded, measured at $V_{DD}/2$	–	200	ps
$t_{SK(PP)}$	Part-to-part skew	Measured at $V_{DD}/2$	–	500	ps
$t_{(\phi)}$[7]	Static phase offset	Measured at $V_{DD}/2$	–	250	ps
$t_{D(\phi)}$[7]	Dynamic phase offset	Measured at $V_{DD}/2$	–	500	ps
$t_{J(CC)}$	Cycle-to-cycle jitter	Load = 15 pF, $f_{OUT} \geq 6.25$ MHz	–	200	ps
			–	35	ps_{RMS}

Notes

7. The $t_{(\phi)}$ reference feedback input delay is guaranteed for a maximum 4:1 input edge ratio between the two signals as long as $t_{SR(I)}$ is maintained. Static phase offset excludes jitter; dynamic phase offset includes jitter.
8. Parameters guaranteed by design and characterization, not 100% tested in production

Downloaded from Arrow.com.

Switching Waveforms

Figure 8. Duty Cycle

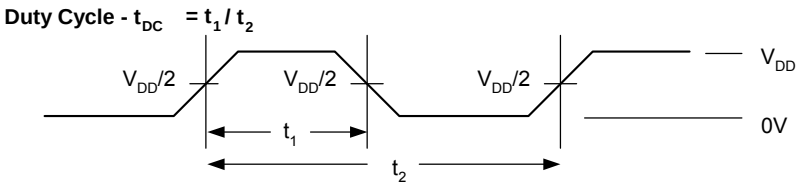


Figure 9. Input Slew Rate

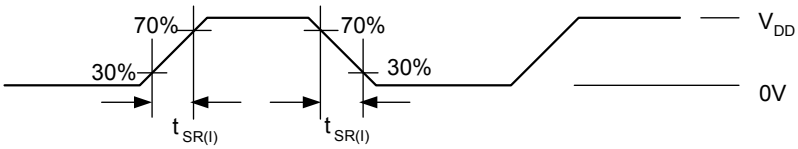


Figure 10. Output Slew Rate

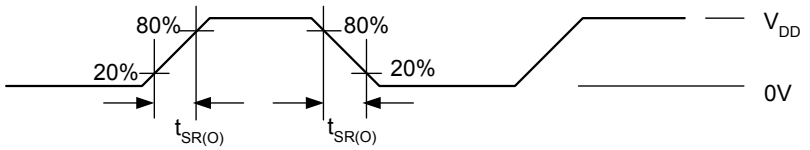


Figure 11. Output to Output Skew and Intrabank Skew

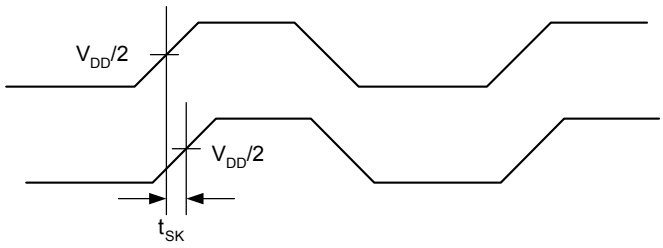
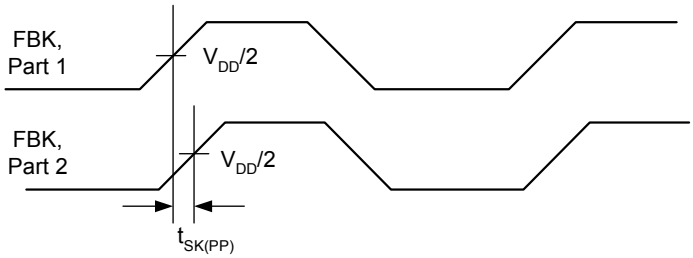


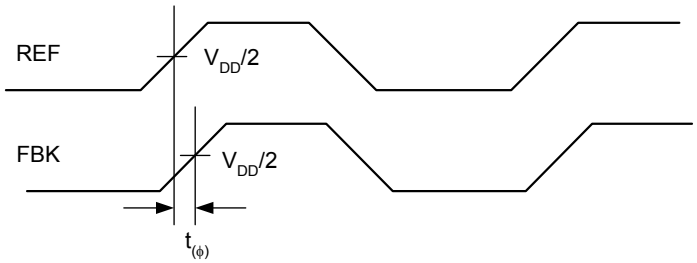
Figure 12. Part to Part Skew



Downloaded from Arrow.com.

Switching Waveforms (continued)

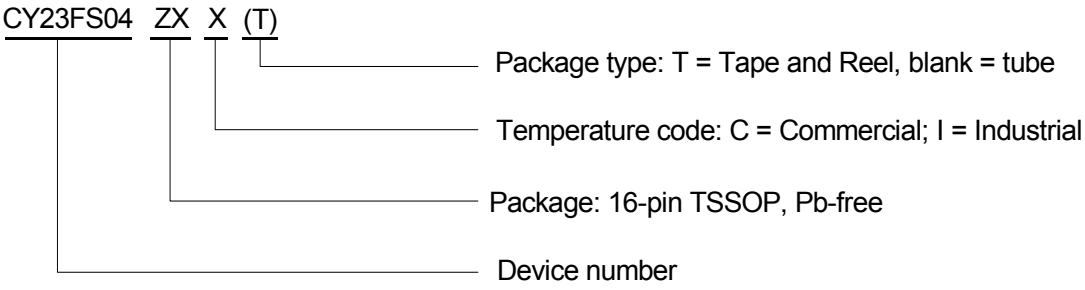
Figure 13. Phase Offset



Ordering Information

Part Number	Package Type	Product Flow
Pb-free		
CY23FS04ZXI	16-pin TSSOP	Industrial, –40 °C to 85 °C
CY23FS04ZXIT	16-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C
CY23FS04ZXC	16-pin TSSOP	Commercial, 0 °C to 70 °C
CY23FS04ZXCT	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C

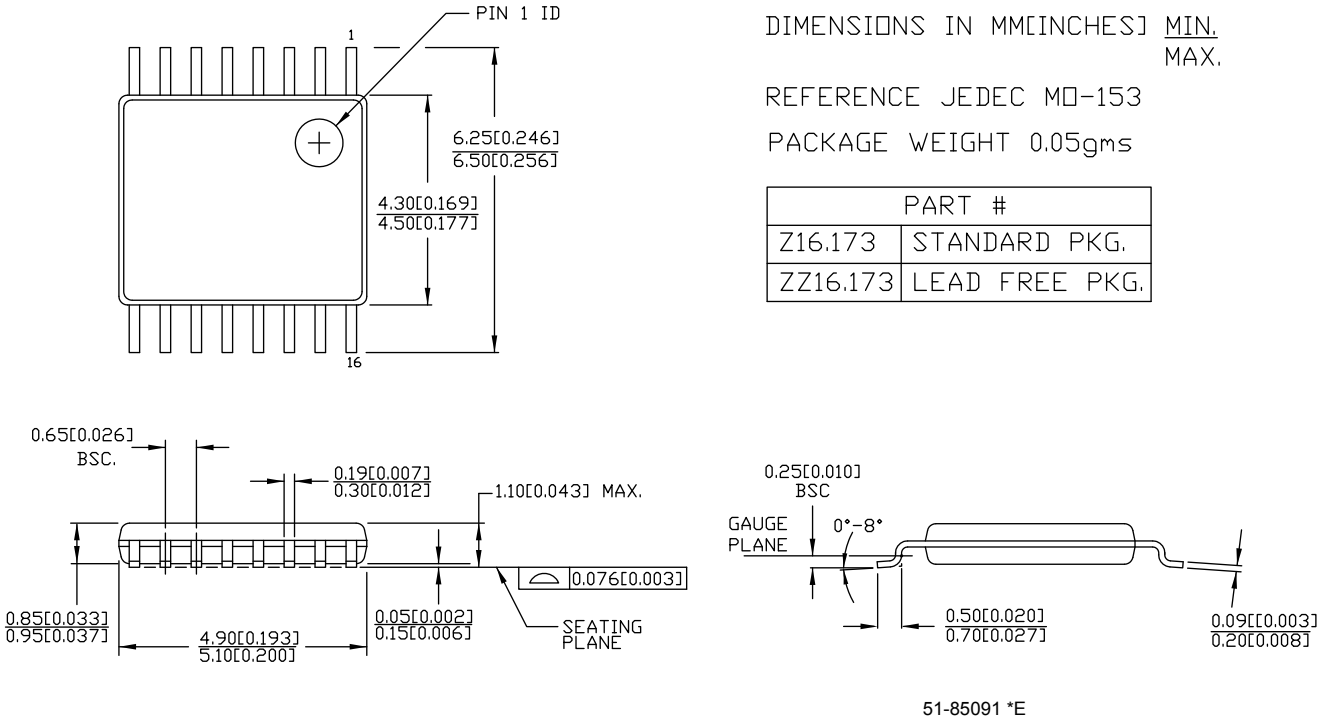
Ordering Code Definitions



Downloaded from Arrow.com.

Package Diagram

Figure 14. 16-pin TSSOP (4.40 mm Body) Z16.173/ZZ16.173 Package Outline, 51-85091



Downloaded from Arrow.com.

Acronyms

Acronym	Description
DCXO	digitally controlled crystal oscillator
ESD	electrostatic discharge
PLL	phase locked loop
RMS	root mean square
SSOP	shrunk small outline package
TSSPO	thin shrunk small outline package
XTAL	crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microampere
mA	milliampere
ms	milli second
MHz	megahertz
ns	nanosecond
pF	picofarad
ps	picosecond
V	volt

Downloaded from Arrow.com.

Document History Page

Document Title: CY23FS04, Failsafe™ 2.5 V/3.3 V Zero Delay Buffer Document Number: 38-07304				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	123698	04/24/03	RGL	New data sheet.
*A	223811	See ECN	RGL/ZJX	Changed the XTAL Specifications table.
*B	276712	See ECN	RGL	Removed (T_{LOCK}) Lock Time Specification
*C	378918	See ECN	RGL	Added Lead-free devices
*D	2865337	01/25/2010	CXQ	Updated format. Changed max output frequency from 170 MHz to 166.7 MHz. Added “Contents” section on page 2. Removed previous Figures 5 and 6. Added/separated Figures 7 through 12. Changed references of “Cl” to “C_{LOAD}”. Removed extra T_A reference in Absolute Maximum Conditions. Changed table captions for Tables 4, 5, and 6 to section headings. Removed note 5 regarding programming cap array. Replaced crystal ECX–5806–18.432M with ECX–6362–18.432M in Note 5. Removed obsolete/pruned Pb-devices from Ordering Information. Removed unreferenced Note 9. Updated package drawing specification to rev *B.
*E	2925613	04/30/10	KVM	Post to external web.
*F	3054919	10/11/2010	KVM	Revised Dynamic Phase Offset value. Added phase offset definition. Added Ordering Code Definitions. Updated Package Diagram. Added Acronyms, and Units of Measure.
*G	3342812	08/12/2011	PURU	Updated Ordering Code Definitions.
*H	3695677	08/03/2012	PURU	Updated XTAL Selection Criteria and Application Example: Updated Figure 7. Updated Table 2. Added Important Notes. Updated Ordering Code Definitions under Ordering Information Replaced SSOP with TSSOP. Updated Package Diagram: spec 51-85091 – Changed revision from *C to *D.
*I	4580603	11/26/2014	AJU	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated Package Diagram: spec 51-85091 – Changed revision from *D to *E.
*J	4930960	09/23/2015	TAVA	Updated to new template. Completing Sunset Review.
*K	5275836	05/27/2016	PSR	Updated Absolute Maximum Conditions: Removed $Ø_{JC}$, $Ø_{JA}$ parameters and their details. Added Thermal Resistance. Updated to new template.
*L	5451081	09/27/2016	TAVA	Updated to new template. Completing Sunset Review.

Downloaded from Arrow.com.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2003-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

FailSafe™ is a trademark of Cypress Semiconductor Corporation.

Purchase of I²C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips. As from October 1st, 2006 Philips Semiconductors has a new trade name - NXP Semiconductors.

Downloaded from Arrow.com.