# Low Duty LCD Segment Driver For Automotive COG Application

## BU91R64CH-M3BW Max 320 Segments (80SEG x 4COM)

### General Description

BU91R64CH-M3BW is a 1/4, 1/3, 1/2 Duty or Static COG type LCD driver that can be used for automotive applications and can drive up to 320 LCD Segments.
This driver can be cascaded up-to maximum of 4 drivers for larger LCD panel application.
It supports VA LCD displays, which has better optical performance with higher LCD voltage driving and higher frame frequency driving.
This driver includes read function for display data and command registers, wherein it is possible to detect malfunction due to noise.
It can also support other error detections such as interface checksum detection, glass breaking detection, logic error detection and SEG / COM toggle detection.
A defective mounting of COG can easily be controlled by using terminals to measure ITO resistance.
It can support operating temperature of up to +105°C and compliant for AEC-Q100, as required for Automotive Application.

### Features

- AEC-Q100 Compliant *(Note 1)*
- 1/4, 1/3, 1/2 Duty or Static Drive Selectable
  - 1/4 Duty Drive: Max 320 Segments
  - 1/3 Duty Drive: Max 240 Segments
  - 1/2 Duty Drive: Max 160 Segments
  - Static Drive: Max 80 Segments
- Integrated Buffer AMP for LCD Driving
- Integrated Oscillator Circuit and Software Programmable Frame Frequency from 66Hz to 488Hz
- Support External Clock Input
- Integrated EVR Function to Adjust LCD Contrast
- Integrated Power On Reset Circuit
- No External Components
- Low Power Consumption Design
- Support Display Inhibit Control
- Configurable COM Driving Order
- Support Max 4 Drivers Cascade Connection (BU91R64 / R65 / R66CH-M3BW Available)
- Support Register and Display Data Read-back Function
- Support LCD Contact Resistance Measurement
- Support Error Detection and Status Read Function
  - Glass Breaking Detection
  - Interface Checksum
  - Logic Error Detection
  - SEG / COM Toggle Detection

*(Note 1)* Quality Information:
There is data when LSI was put on a temporary package.
Please use it as reference data.

### Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- LCD Drive Power Supply Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments: 320 Segments
- Display Duty: 1/4, 1/3, 1/2, Static Selectable
- Bias: 1/2, 1/3 Selectable
- Interface: 2-wire / 3-wire Serial Interface Selectable

### Special Characteristics

- ESD(HBM) *(Note 2)*: ±2000V(Typ)
- Latch-up Current *(Note 2)*: ±100mA(Typ)

*(Note 2)* There is data when LSI was put on a temporary package.

### Applications

- Instrument Clusters
- Climate Controls
- Car Audios / Radios
- Meters
- White Goods
- Healthcare Products
- Battery Operated Applications

etc.

### Package

Au Bump Chip


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Contents

General Description ....1
Features ....1
Key Specifications ....1
Special Characteristics ....1
Applications ....1
Package ....1
Contents ....2
Typical Application Circuit ....6
Block Diagram ....6
Terminal Description ....7
Recommended ITO Layout (Top view) ....8
  Terminal Resistance ....10
PAD Arrangement (Top view) ....11
Dimension ....12
PAD Coordinates ....13
Absolute Maximum Ratings (VSS = 0V) ....15
Recommended Operating Conditions ....15
Electrical Characteristics ....16
  DC Characteristics ....16
  Oscillation Characteristics ....17
  2-wire Serial Interface Characteristics ....18
  3-wire Serial Interface Characteristics ....19
I/O Equivalence Circuit ....20
MCU Interface ....21
  START and STOP Condition (2-wire) ....21
  Acknowledge (ACK) (2-wire) ....21
  Command / Display Data Transfer Method (2-wire) ....22
  Display Data Transfer Method (2-wire) ....23
  Display Data Read-back Method (2-wire) ....24
  Command Registers Read-back Method (2-wire) ....25
  Command / Display Data Transfer Method (3-SPI) ....26
  Command Transfer Method (3-SPI) ....26
  Display Data Transfer Method (3-SPI) ....27
  Display Data Read-back Method (3-SPI) ....28
  Command Registers Read-back Method (3-SPI) ....28
OSC (Oscillator) ....29
SYNC CTRL (Multi-chip Structure) ....30
LCD Driver Voltage Generator / LCD Bias Selector ....33
POR and Reset Initialize Condition ....33
Blink Control (Blink Timing Generator) ....33
Error Detection ....34
  Glass Breaking Detection ....35
  Checksum Detection ....37
  Logic Error Detection ....38
  SEG / COM Toggle Detection ....39
  Contact Resistance Check ....39
Command / Function List ....40
Detailed Command Description ....40
  1. Mode Set 1 (MODESET1) ....40
  2. Address Set (ADSET) ....41
  3. Sub Address Set (SADSET) ....41
  4. Frame Rate Set (FRSET) ....42


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

5. Blink Control1 (BLKCTL1) ....43
6. Blink Control2 (BLKCTL2) ....43
7. Command Extension (CMDXTN) ....44
8. Software Reset (SWRST) ....44
9. Mode Set 2 (MODESET2) ....45
10. Mode Set 3 (MODESET3) ....45
11. Contrast Setting (CNTSET) ....46
12. Read Control (RDCTL) ....47
13. Checksum (CHKSUM) ....47
14. COM Set (COMSET) ....48

LCD Driving Waveform ....49
1/3 Bias, 1/4 Duty Drive ....49
1/2 Bias, 1/4 Duty Drive ....50
1/3 Bias, 1/3 Duty Drive ....51
1/2 Bias, 1/3 Duty Drive ....52
1/3 Bias, 1/2 Duty Drive ....53
1/2 Bias, 1/2 Duty Drive ....54
Static Drive ....55

Example of Display Data ....56

Initialize Sequence ....57

Start Sequence ....58
Start Sequence Example1 ....58
Start Sequence Example2 ....59

Cautions in Power On / Off ....60

Display Off Operation in External Clock Mode ....61
In Multi-chip Structure in Internal Clock Mode ....61

Note on The Multiple Device Connection to 2-wire Serial Interface. ....62

Note in Case that the SDA is Stuck at LOW ....62

Operational Notes ....63
**1. Reverse Connection of Power Supply** ....63
**2. Power Supply Lines** ....63
**3. Ground Voltage** ....63
**4. Ground Wiring Pattern** ....63
**5. Recommended Operating Conditions** ....63
**6. Inrush Current** ....63
**7. Operation Under Strong Electromagnetic Field** ....63
**8. Testing on Application Boards** ....63
**9. Inter-pin Short and Mounting Errors** ....63
**10. Unused Input Pins** ....63
**11. Regarding the Input Pin of the IC** ....63
**12. Ceramic Capacitor** ....63
**13. Disturbance Light** ....64

Ordering Information ....65

Lineup ....65

Marking Diagram ....65

Packing Quantity ....66

Pallet Drawing ....66

Package Condition ....67

Physical Dimension Tray Information ....68

Revision History ....69


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

Figure 1. Typical Application Circuit ..... 6
Figure 2. Block Diagram ..... 6
Figure 3. Recommended ITO Layout A ..... 8
Figure 4. Recommended ITO Layout B ..... 9
Figure 5. PAD Alignment ..... 11
Figure 6. PAD / Bump Information ..... 12
Figure 7. Operating Current vs Power Supply Voltage ..... 16
Figure 8. Frame Frequency vs Temperature ..... 17
Figure 9. Interface Timing of 2-wire Serial Interface ..... 18
Figure 10. Interface Timing of 3-wire Serial Interface ..... 19
Figure 11. I/O Equivalence Circuit ..... 20
Figure 12. 2-wire Command / Data Transfer Format ..... 21
Figure 13. Acknowledge Timing ..... 21
Figure 14. Wrong Slave Address Case ..... 21
Figure 15. 2-wire Interface Protocol ..... 22
Figure 16. Wrong Slave Address Case ..... 22
Figure 17. Display Data Transfer in 2-wire ..... 23
Figure 18. DDRAM Address Map in Write Mode ..... 23
Figure 19. Display Data Read-back in 2-wire ..... 24
Figure 20. Bit-Assignment in Display Data Read-back in 2-wire ..... 24
Figure 21. DDRAM Address Map in Read Mode ..... 24
Figure 22. Command Registers Read-back Method in 2-wire ..... 25
Figure 23. Command / Data Transfer in 3-SPI Command / Data Transfer in 3-SPI ..... 26
Figure 24. Escape from Data Transfer Condition in 3-SPI ..... 26
Figure 25. Case of Less Than 8-bit Data Transfer in 3-SPI ..... 26
Figure 26. Display Data Transfer and Bit Assignment in 3-SPI ..... 27
Figure 27. Case of Less Than 4-bit Write Data Transfer in 3-SPI ..... 27
Figure 28. Display Data Read-back in 3-SPI ..... 28
Figure 29. Display Data Read-back in 3-SPI ..... 28
Figure 30. Command Registers Read-back in 3-SPI ..... 28
Figure 31. Internal Clock Mode ..... 29
Figure 32. External Clock Mode ..... 29
Figure 33. Synchronization of Multi-chip Cascaded Connection ..... 31
Figure 34. Example of Cascaded Connection ..... 32
Figure 35. Example Different Duty Drive Panel Configuration ..... 32
Figure 36. Bank Blink Mode Function (Blink Frequency as 32 Frame Case) ..... 33
Figure 37. DDRAM Address Map of Blink Area (Bank Blink Mode) ..... 33
Figure 38. Detection Block and Data Path ..... 34
Figure 39. Glass Breaking Detection ..... 35
Figure 40. Sequence of Glass Breaking Detection ..... 36
Figure 41. Sequence of Checksum Detection ..... 37
Figure 42. Example of Checksum Calculation ..... 37
Figure 43. Sequence of Logic Error Detection ..... 38
Figure 44. Sequence of SEG / COM Toggle Detection ..... 39
Figure 45. DUMMY PADs for the Contact Resistance Measurement ..... 39
Figure 46. COM Scan Direction Image ..... 48
Figure 47. LCD Waveform (1/3 Bias, 1/4 Duty Drive) ..... 49
Figure 48. LCD Waveform (1/2 Bias, 1/4 Duty Drive) ..... 50
Figure 49. LCD Waveform (1/3 Bias, 1/3 Duty Drive) ..... 51
Figure 50. LCD Waveform (1/2 Bias, 1/3 Duty Drive) ..... 52
Figure 51. LCD Waveform (1/3 Bias, 1/2 Duty Drive) ..... 53
Figure 52. LCD Waveform (1/2 Bias, 1/2 Duty Drive) ..... 54
Figure 53. LCD Waveform (Static Drive) ..... 55
Figure 54. Example COM Line Pattern ..... 56
Figure 55. Example SEG Line Pattern ..... 56
Figure 56. Example Display Pattern ..... 56
Figure 57. Recommended Power On / Off Sequence ..... 60
Figure 58. Power On / Off Waveform ..... 60
Figure 59. Dummy Clock / STOP / START Condition ..... 60
Figure 60. CSB Timing ..... 60
Figure 61. External Clock Stop Timing ..... 61
Figure 62. DISPOFF Sequence in Multi-chip Structure ..... 61
Figure 63. Example of BUS Connection ..... 62
Figure 64. SDA Output Cell Structure ..... 62
Figure 65. Recovery Sequence from SDA Stuck ..... 62


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

Table 1. Pin Description ....7
Table 2. Dimension (Completion Size) ....12
Table 3. Bump Specs and Dimensions ....12
Table 4. Pad Coordinates ....13
Table 5. Command Register Map for Read-back ....25
Table 6. Detection Functions ....34
Table 7. Command / Function List ....40
Table 8. Frame Frequency (Internal Clock Mode) ....42
Table 9. Frame Frequency (External Clock Mode) ....42
Table 10. V0 Voltage Setting ....46
Table 11. DDRAM Data Example ....56


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Typical Application Circuit

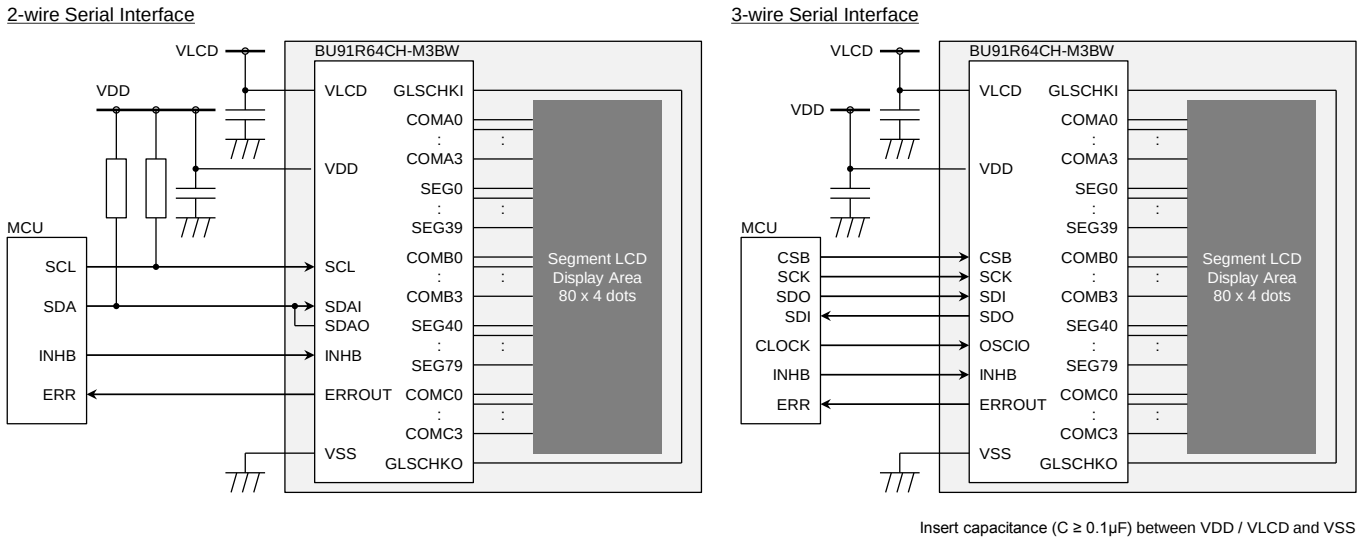



Figure 1. Typical Application Circuit

## Block Diagram

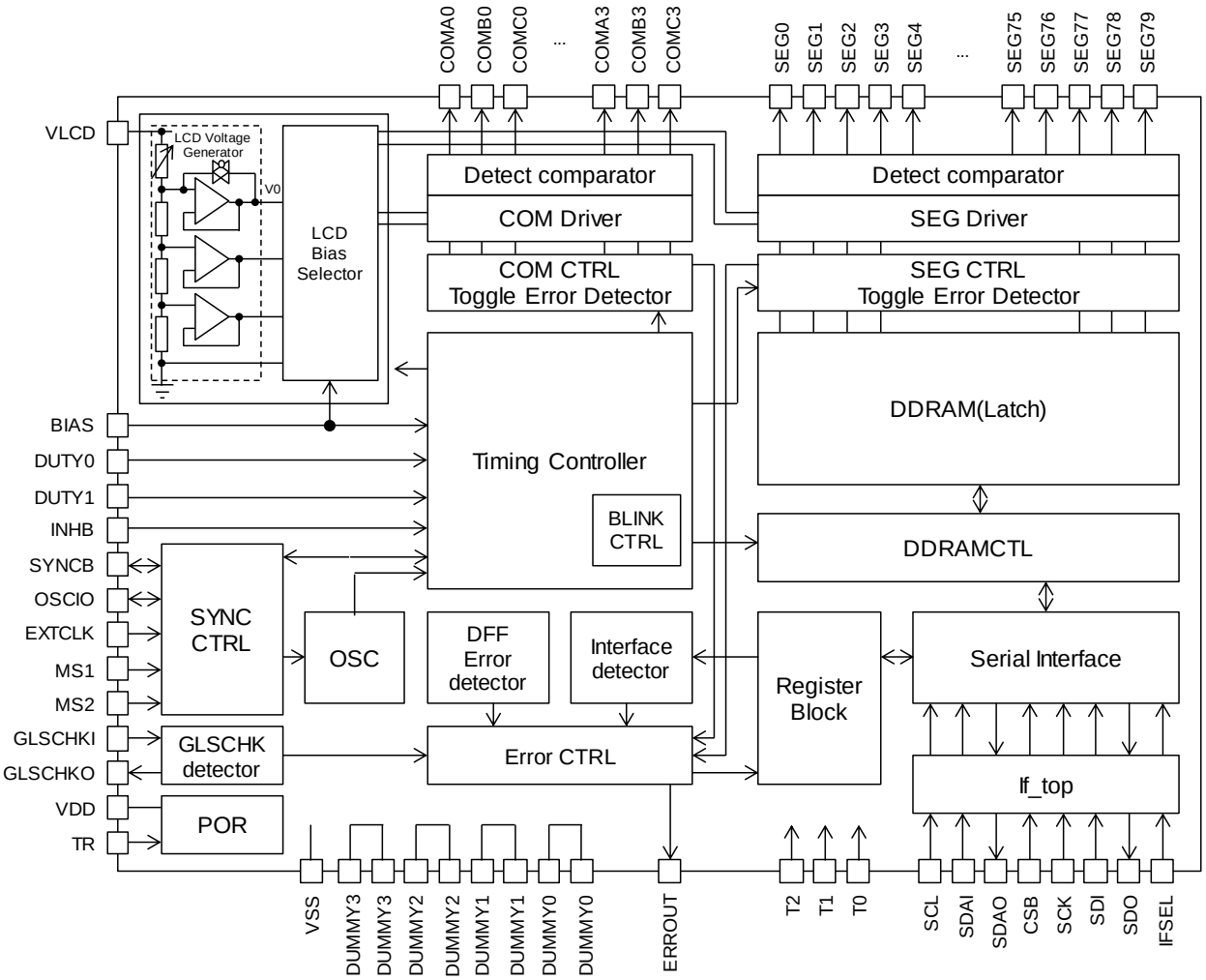



Figure 2. Block Diagram


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Terminal Description

Table 1. Terminal Description

<table>
<tr><th>Terminal Name</th><th>I/O</th><th>Function</th><th>Handling when unused</th></tr>
<tr><td>VDD</td><td>I</td><td>Power supply for logic</td><td>-</td></tr>
<tr><td>VLCD</td><td>I</td><td>Power supply for LCD driving circuit</td><td>-</td></tr>
<tr><td>VSS</td><td>I</td><td>Ground</td><td>-</td></tr>
<tr><td>MS1</td><td>I</td><td rowspan="2">Single / Multi-chip setting
<table>
<tr><th rowspan="2">MS2</th><th rowspan="2">MS1</th><th colspan="2">2-wire Interface</th><th>3-wire Interface</th></tr>
<tr><th>Function</th><th>Slave Address[7:1]</th><th>Function</th></tr>
<tr><td>VSS</td><td>VSS</td><td>Master</td><td>0111110 / 0111000</td><td>Master</td></tr>
<tr><td>VSS</td><td>VDD</td><td>Slave1</td><td>0111111 / 0111001</td><td>Slave1</td></tr>
<tr><td>VDD</td><td>VSS</td><td>Slave2</td><td>0111110 / 0111000</td><td>Slave2</td></tr>
<tr><td>VDD</td><td>VDD</td><td>Slave3</td><td>0111111 / 0111001</td><td>Slave3</td></tr>
</table></td><td>VDD / VSS</td></tr>
<tr><td>MS2</td><td>I</td><td>VDD / VSS</td></tr>
<tr><td>EXTCLK</td><td>I</td><td>Clock mode setting<br>VDD: External Clock Mode, VSS: Internal Clock Mode</td><td>VDD / VSS</td></tr>
<tr><td>OSCIO</td><td>I/O</td><td>Clock input / output setting<br>External Clock Mode: input of external clock<br>Internal Clock Mode: output of internal clock</td><td>OPEN</td></tr>
<tr><td>SYNCB</td><td>I/O</td><td>Synchronous signal input / output for multi-chip mode<br>Master: Synchronous signal output<br>Slave: master SYNCB signal input</td><td>OPEN</td></tr>
<tr><td>IFSEL</td><td>I</td><td>MCU Interface select<br>VDD: 3-wire Serial Interface<br>VSS: 2-wire Serial Interface</td><td>VDD / VSS</td></tr>
<tr><td>SDAI</td><td>I</td><td>Serial data input for 2-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SDAO</td><td>O</td><td>Serial data output for 2-wire Serial Interface</td><td>OPEN</td></tr>
<tr><td>SCL</td><td>I</td><td>Serial clock for 2-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select for 3-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SCK</td><td>I</td><td>Serial clock for 3-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SDI</td><td>I</td><td>Serial data input for 3-wire Serial Interface</td><td>VSS</td></tr>
<tr><td>SDO</td><td>O</td><td>Serial data output for 3-wire Serial Interface</td><td>OPEN</td></tr>
<tr><td>INHB</td><td>I</td><td>Inhibit display status in spite of Display On by command setting<br>VDD: Keep display status by command setting<br>VSS: Inhibit display status. All SEG and COM terminals output VSS level.</td><td>VDD</td></tr>
<tr><td>DUTY0</td><td>I</td><td rowspan="2">Duty Drive select
<table>
<tr><th>DUTY1</th><th>DUTY0</th><th>Duty Drive</th></tr>
<tr><td>VSS</td><td>VSS</td><td>1/4 Duty Drive</td></tr>
<tr><td>VSS</td><td>VDD</td><td>1/3 Duty Drive</td></tr>
<tr><td>VDD</td><td>VSS</td><td>1/2 Duty Drive</td></tr>
<tr><td>VDD</td><td>VDD</td><td>Static Drive (also set to 1/1 Bias)</td></tr>
</table></td><td>VDD / VSS</td></tr>
<tr><td>DUTY1</td><td>I</td><td>VDD / VSS</td></tr>
<tr><td>BIAS</td><td>I</td><td>LCD Bias select<br>VDD: 1/2 Bias, VSS: 1/3 Bias (Static Drive: don’t care)</td><td>VDD / VSS</td></tr>
<tr><td>GLSCHKO</td><td>O</td><td>Output for glass breaking detection<br>Connect to GLSCHKI for glass breaking detection.</td><td>OPEN</td></tr>
<tr><td>GLSCHKI</td><td>I</td><td>Input for glass breaking detection<br>Connect to GLSCHKO for glass breaking detection.</td><td>VSS</td></tr>
<tr><td>ERROUT</td><td>O</td><td>Output data of error detection<br>VDD: Abnormal status, VSS: Normal status</td><td>OPEN</td></tr>
<tr><td>DUMMY0 to DUMMY3</td><td>-</td><td>Can be used for the contact resistance measurement.</td><td>OPEN</td></tr>
<tr><td>DUMMY</td><td>-</td><td>Open</td><td>OPEN</td></tr>
<tr><td>TR</td><td>I</td><td>POR enable setting (Note 1)<br>VDD: POR disable, VSS: POR enable</td><td>VSS</td></tr>
<tr><td>T0,T1,T2</td><td>I</td><td>Test input (ROHM use only)<br>Must be connected to VSS.</td><td>VSS</td></tr>
<tr><td>SEG0 to SEG79</td><td>O</td><td>Segment output for LCD driving</td><td>OPEN</td></tr>
<tr><td>COMA0 to COMA3</td><td>O</td><td>Common output for LCD driving</td><td>OPEN</td></tr>
<tr><td>COMB0 to COMB3</td><td>O</td><td>Common output for LCD driving</td><td>OPEN</td></tr>
<tr><td>COMC0 to COMC3</td><td>O</td><td>Common output for LCD driving</td><td>OPEN</td></tr>
</table>

*(Note 1)* This function is guaranteed by design, not tested in production process. Software Reset is necessary to initialize IC in case of TR = VDD.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

### Recommended ITO Layout (Top view)

| Function | Setting |
|---|---|
| POR | USE<br>TR = VSS |
| Error Detection | YES<br>(Glass Breaking Detection,<br>Contact Resistance Check) |
| Multi-chip Mode | NO |
| Duty Drive | 1/4 Duty Drive<br>(DUTY0, DUTY1) = (VSS, VSS) |
| Bias Setting | 1/3 Bias<br>BIAS = VSS |
| I/F | 2-wire Serial Interface<br>IFSEL = VSS |
| Clock Mode | Internal Clock Mode<br>EXTCLK = VSS |
| Master/Slave | Master<br>(MS1, MS2) = (VSS, VSS) |
| Inhibit Function | NO<br>INHB = VDD |

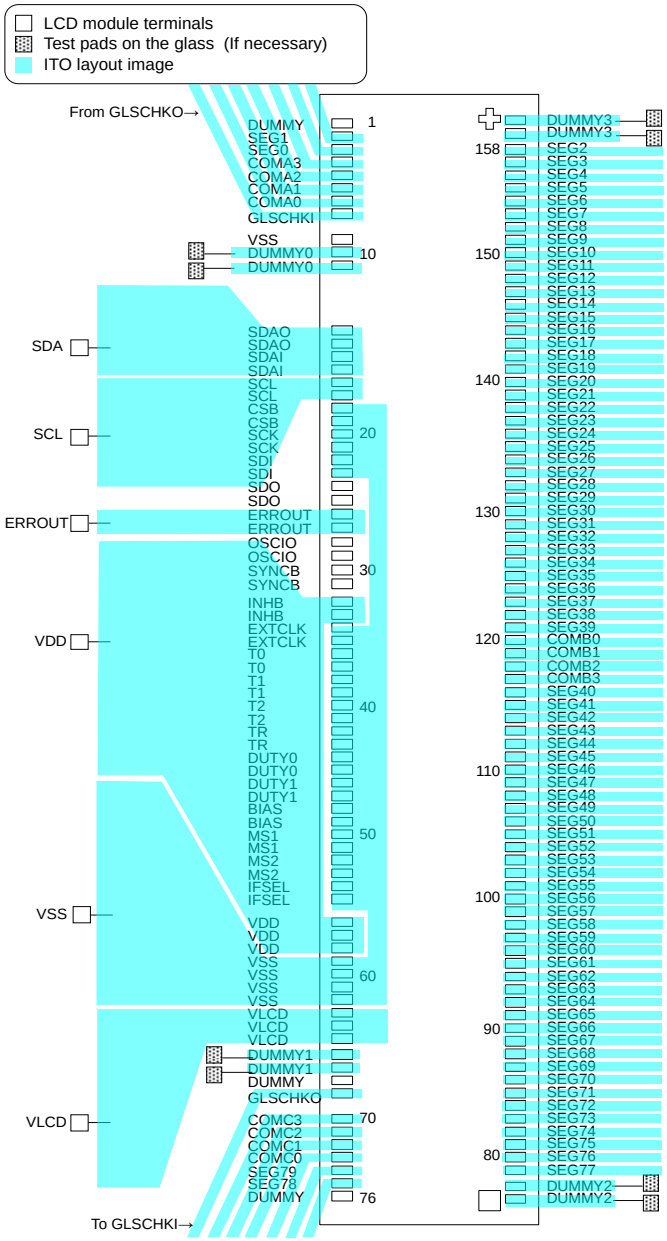



Figure 3. Recommended ITO Layout A


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

### Recommended ITO Layout (Top view) – continued

| Function | Setting |
|---|---|
| POR | Not USE<br>TR = VDD |
| Error Detection | NO |
| Multi-chip Mode | YES |
| Duty Drive | Static Drive<br>(DUTY0, DUTY1) = (VDD, VDD) |
| Bias Setting | Static Drive<br>BIAS = VSS |
| I/F | 3-wire Serial Interface<br>IFSEL = VDD |
| Clock Mode | Internal Clock Mode<br>EXTCLK = VSS |
| Master/Slave | Slave1<br>(MS1, MS2) = (VDD, VSS) |
| Inhibit Function | YES<br>INHB = MCU control |

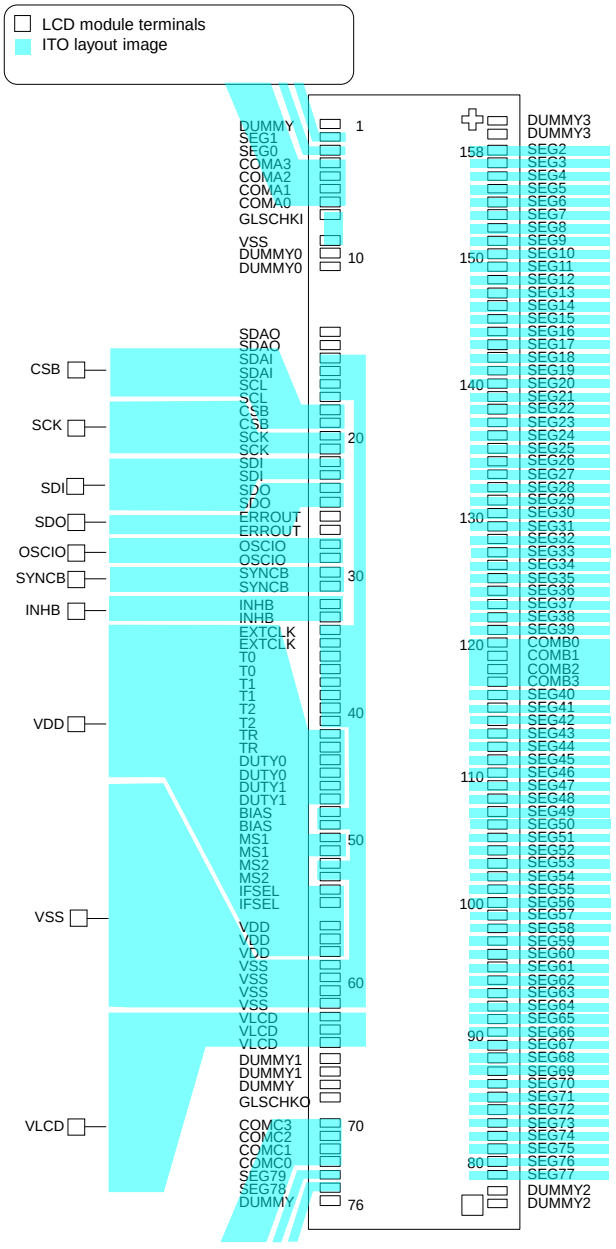



Figure 4. Recommended ITO Layout B


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Recommended ITO Layout (Top view) – continued

### Terminal Resistance

| PAD No. | Terminal Name | Maximum Resistance |
|---|---|---|
| 12, 13 | SDAO | 1,500Ω |
| 14, 15 | SDAI | 1,500Ω |
| 16, 17 | SCL | 1,500Ω |
| 18, 19 | CSB | 1,500Ω |
| 20, 21 | SCK | 1,500Ω |
| 22, 23 | SDI | 1,500Ω |
| 24, 25 | SDO | 1,500Ω |
| 26, 27 | ERROUT | 1,500Ω |
| 28, 29 | OSCIO | 1,500Ω |
| 30, 31 | SYNCB | 1,500Ω |
| 32, 33 | INHB | 1,500Ω |
| 56 to 58 | VDD | 400Ω |
| 59 to 62 | VSS | 400Ω |
| 63 to 65 | VLCD | 400Ω |

Refer to **Glass Breaking Detection** for GLSCHKI and GLSCHKO terminal resistance


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

**PAD Arrangement (Top view)**

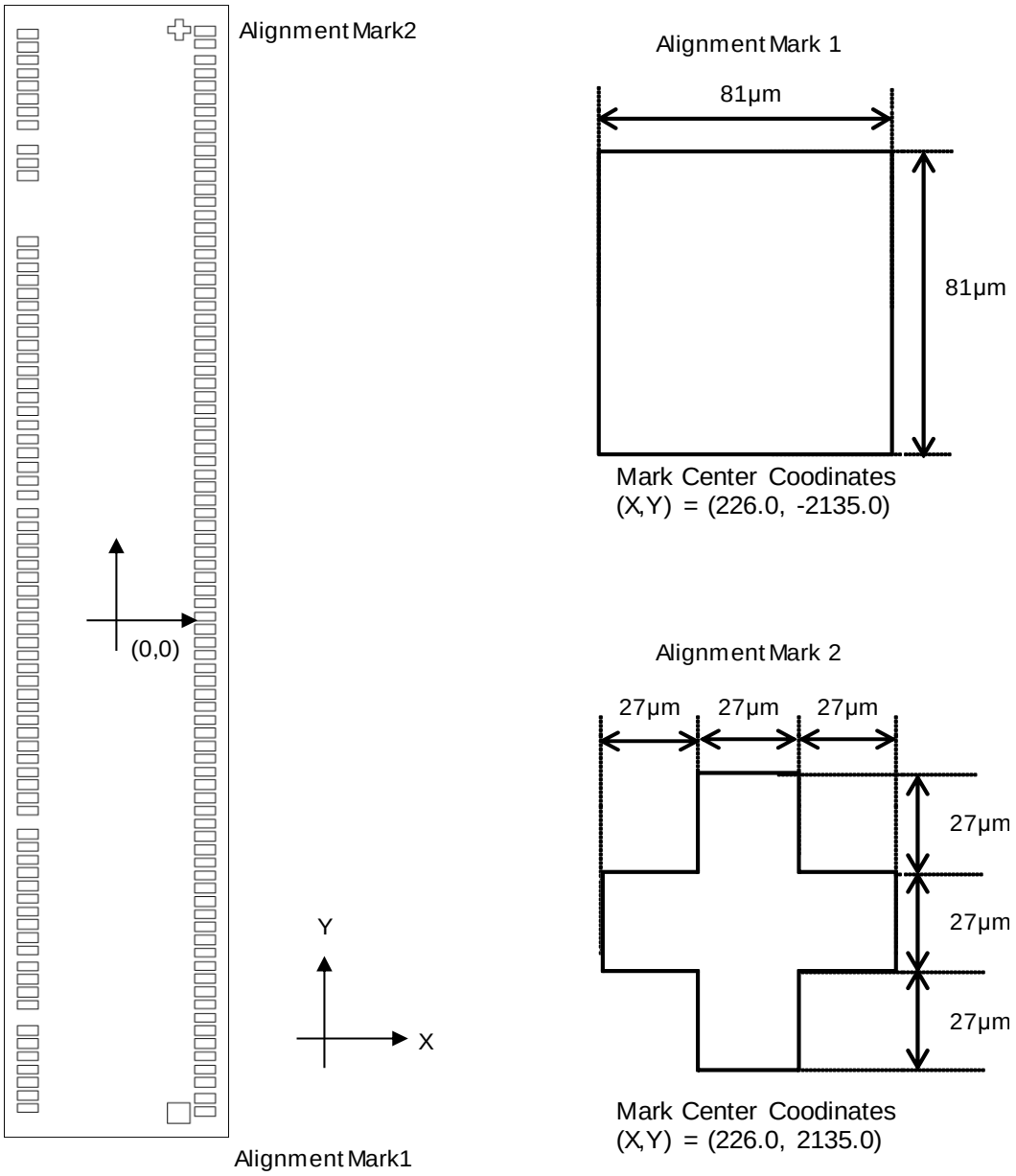



Figure 5. PAD Alignment


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Dimension

Table 2. Dimension (Completion Size)

| Mark | | Topic | Specification Limit |
|---|---|---|---|
| Chip Size X | | Chip Size : X Direction | 785 ± 40 μm |
| Chip Size Y | | Chip Size : Y Direction | 4435 ± 40 μm |
| Chip Thickness | | Chip Thickness | 300 ± 20 μm |
| PAD | A (PAD1 to PAD160) | Bump Size : X Direction | 75 ± 3.0 μm |
| | B (PAD1 to PAD160) | Bump Size : Y Direction | 36 ± 3.0 μm |
| | C (PAD1 to PAD160) | Average of Bump Height | 15 ± 3.0 μm |

Table 3. Bump Specs and Dimensions

| Topic | Specification Limit |
|---|---|
| Bump Structure | Straight Bump |
| Bump Co-planarity on Chip | 3.0 μm or less |
| Bump Hardness (Microvicker's Meter) | 50 Hv ± 20 Hv |
| Bump Strength | 7.35 mg / μm$^2$ or more |

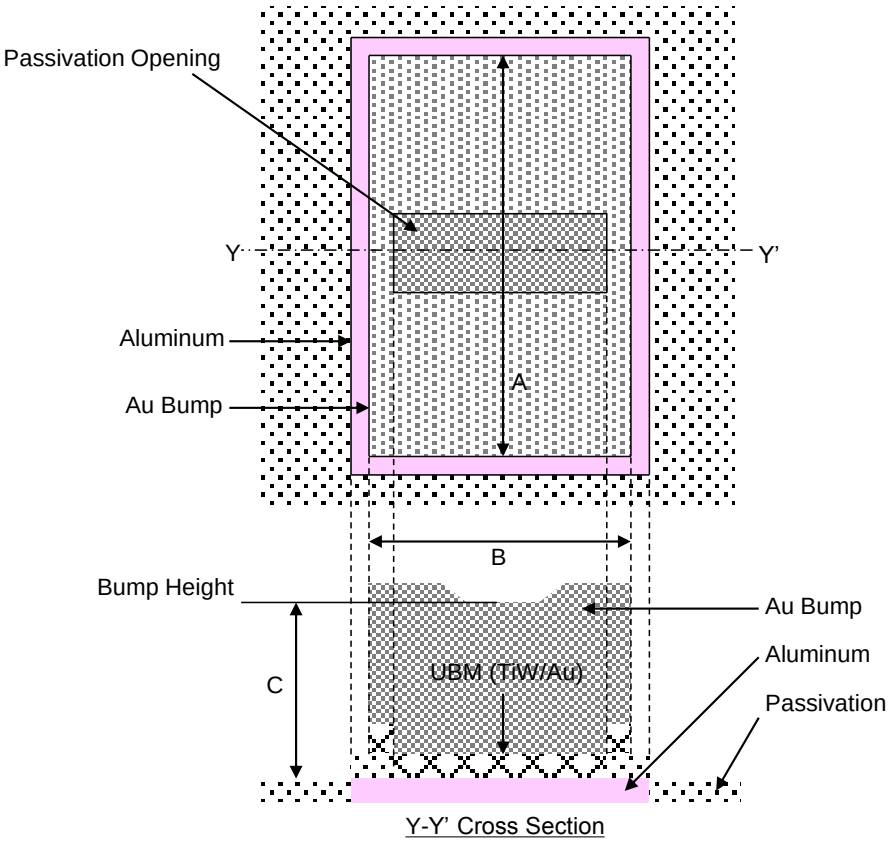



Figure 6. PAD / Bump Information


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## PAD Coordinates

Table 4. PAD Coordinates

Unit: μm

| PAD No | Terminal Name | Bump Center X | Bump Center Y | Bump Size X | Bump Size Y |
|---|---|---|---|---|---|
| 1 | DUMMY | -320.50 | 2116.50 | 75 | 36 |
| 2 | SEG1 | -320.50 | 2065.50 | 75 | 36 |
| 3 | SEG0 | -320.50 | 2014.50 | 75 | 36 |
| 4 | COMA3 | -320.50 | 1963.50 | 75 | 36 |
| 5 | COMA2 | -320.50 | 1912.50 | 75 | 36 |
| 6 | COMA1 | -320.50 | 1861.50 | 75 | 36 |
| 7 | COMA0 | -320.50 | 1810.50 | 75 | 36 |
| 8 | GLSCHKI | -320.50 | 1759.50 | 75 | 36 |
| 9 | VSS | -320.50 | 1659.50 | 75 | 36 |
| 10 | DUMMY0 | -320.50 | 1608.50 | 75 | 36 |
| 11 | DUMMY0 | -320.50 | 1557.50 | 75 | 36 |
| 12 | SDAO | -320.50 | 1298.80 | 75 | 36 |
| 13 | SDAO | -320.50 | 1247.80 | 75 | 36 |
| 14 | SDAI | -320.50 | 1196.80 | 75 | 36 |
| 15 | SDAI | -320.50 | 1145.80 | 75 | 36 |
| 16 | SCL | -320.50 | 1094.80 | 75 | 36 |
| 17 | SCL | -320.50 | 1043.80 | 75 | 36 |
| 18 | CSB | -320.50 | 992.80 | 75 | 36 |
| 19 | CSB | -320.50 | 941.80 | 75 | 36 |
| 20 | SCK | -320.50 | 890.80 | 75 | 36 |
| 21 | SCK | -320.50 | 839.80 | 75 | 36 |
| 22 | SDI | -320.50 | 788.80 | 75 | 36 |
| 23 | SDI | -320.50 | 737.80 | 75 | 36 |
| 24 | SDO | -320.50 | 685.05 | 75 | 36 |
| 25 | SDO | -320.50 | 630.05 | 75 | 36 |
| 26 | ERROUT | -320.50 | 575.05 | 75 | 36 |
| 27 | ERROUT | -320.50 | 520.05 | 75 | 36 |
| 28 | OSCIO | -320.50 | 465.05 | 75 | 36 |
| 29 | OSCIO | -320.50 | 410.05 | 75 | 36 |
| 30 | SYNCB | -320.50 | 355.05 | 75 | 36 |
| 31 | SYNCB | -320.50 | 300.05 | 75 | 36 |
| 32 | INHB | -320.50 | 228.85 | 75 | 36 |
| 33 | INHB | -320.50 | 177.85 | 75 | 36 |
| 34 | EXTCLK | -320.50 | 126.85 | 75 | 36 |
| 35 | EXTCLK | -320.50 | 75.85 | 75 | 36 |
| 36 | T0 | -320.50 | 24.85 | 75 | 36 |
| 37 | T0 | -320.50 | -26.15 | 75 | 36 |
| 38 | T1 | -320.50 | -77.15 | 75 | 36 |
| 39 | T1 | -320.50 | -128.15 | 75 | 36 |
| 40 | T2 | -320.50 | -179.15 | 75 | 36 |
| 41 | T2 | -320.50 | -230.15 | 75 | 36 |
| 42 | TR | -320.50 | -281.15 | 75 | 36 |
| 43 | TR | -320.50 | -332.15 | 75 | 36 |
| 44 | DUTY0 | -320.50 | -383.15 | 75 | 36 |
| 45 | DUTY0 | -320.50 | -434.15 | 75 | 36 |
| 46 | DUTY1 | -320.50 | -485.15 | 75 | 36 |
| 47 | DUTY1 | -320.50 | -536.15 | 75 | 36 |
| 48 | BIAS | -320.50 | -587.15 | 75 | 36 |
| 49 | BIAS | -320.50 | -638.15 | 75 | 36 |
| 50 | MS1 | -320.50 | -689.15 | 75 | 36 |
| 51 | MS1 | -320.50 | -740.15 | 75 | 36 |
| 52 | MS2 | -320.50 | -791.15 | 75 | 36 |
| 53 | MS2 | -320.50 | -842.15 | 75 | 36 |
| 54 | IFSEL | -320.50 | -893.15 | 75 | 36 |
| 55 | IFSEL | -320.50 | -944.15 | 75 | 36 |
| 56 | VDD | -320.50 | -1035.55 | 75 | 36 |
| 57 | VDD | -320.50 | -1086.55 | 75 | 36 |
| 58 | VDD | -320.50 | -1137.55 | 75 | 36 |
| 59 | VSS | -320.50 | -1188.55 | 75 | 36 |
| 60 | VSS | -320.50 | -1239.55 | 75 | 36 |
| 61 | VSS | -320.50 | -1290.55 | 75 | 36 |
| 62 | VSS | -320.50 | -1341.55 | 75 | 36 |
| 63 | VLCD | -320.50 | -1392.55 | 75 | 36 |
| 64 | VLCD | -320.50 | -1443.55 | 75 | 36 |
| 65 | VLCD | -320.50 | -1494.55 | 75 | 36 |
| 66 | DUMMY1 | -320.50 | -1557.50 | 75 | 36 |
| 67 | DUMMY1 | -320.50 | -1608.50 | 75 | 36 |
| 68 | DUMMY | -320.50 | -1659.50 | 75 | 36 |
| 69 | GLSCHKO | -320.50 | -1710.50 | 75 | 36 |
| 70 | COMC3 | -320.50 | -1810.50 | 75 | 36 |
| 71 | COMC2 | -320.50 | -1861.50 | 75 | 36 |
| 72 | COMC1 | -320.50 | -1912.50 | 75 | 36 |
| 73 | COMC0 | -320.50 | -1963.50 | 75 | 36 |
| 74 | SEG79 | -320.50 | -2014.50 | 75 | 36 |
| 75 | SEG78 | -320.50 | -2065.50 | 75 | 36 |
| 76 | DUMMY | -320.50 | -2116.50 | 75 | 36 |
| 77 | DUMMY2 | 320.50 | -2128.60 | 75 | 36 |
| 78 | DUMMY2 | 320.50 | -2077.60 | 75 | 36 |
| 79 | SEG77 | 320.50 | -2014.50 | 75 | 36 |
| 80 | SEG76 | 320.50 | -1963.50 | 75 | 36 |
| 81 | SEG75 | 320.50 | -1912.50 | 75 | 36 |
| 82 | SEG74 | 320.50 | -1861.50 | 75 | 36 |
| 83 | SEG73 | 320.50 | -1810.50 | 75 | 36 |
| 84 | SEG72 | 320.50 | -1759.50 | 75 | 36 |
| 85 | SEG71 | 320.50 | -1708.50 | 75 | 36 |
| 86 | SEG70 | 320.50 | -1657.50 | 75 | 36 |
| 87 | SEG69 | 320.50 | -1606.50 | 75 | 36 |
| 88 | SEG68 | 320.50 | -1555.50 | 75 | 36 |
| 89 | SEG67 | 320.50 | -1504.50 | 75 | 36 |
| 90 | SEG66 | 320.50 | -1453.50 | 75 | 36 |
| 91 | SEG65 | 320.50 | -1402.50 | 75 | 36 |
| 92 | SEG64 | 320.50 | -1351.50 | 75 | 36 |
| 93 | SEG63 | 320.50 | -1300.50 | 75 | 36 |
| 94 | SEG62 | 320.50 | -1249.50 | 75 | 36 |
| 95 | SEG61 | 320.50 | -1198.50 | 75 | 36 |
| 96 | SEG60 | 320.50 | -1147.50 | 75 | 36 |
| 97 | SEG59 | 320.50 | -1096.50 | 75 | 36 |
| 98 | SEG58 | 320.50 | -1045.50 | 75 | 36 |
| 99 | SEG57 | 320.50 | -994.50 | 75 | 36 |
| 100 | SEG56 | 320.50 | -943.50 | 75 | 36 |
| 101 | SEG55 | 320.50 | -892.50 | 75 | 36 |
| 102 | SEG54 | 320.50 | -841.50 | 75 | 36 |
| 103 | SEG53 | 320.50 | -790.50 | 75 | 36 |
| 104 | SEG52 | 320.50 | -739.50 | 75 | 36 |
| 105 | SEG51 | 320.50 | -688.50 | 75 | 36 |
| 106 | SEG50 | 320.50 | -637.50 | 75 | 36 |
| 107 | SEG49 | 320.50 | -586.50 | 75 | 36 |
| 108 | SEG48 | 320.50 | -535.50 | 75 | 36 |
| 109 | SEG47 | 320.50 | -484.50 | 75 | 36 |
| 110 | SEG46 | 320.50 | -433.50 | 75 | 36 |
| 111 | SEG45 | 320.50 | -382.50 | 75 | 36 |
| 112 | SEG44 | 320.50 | -331.50 | 75 | 36 |
| 113 | SEG43 | 320.50 | -280.50 | 75 | 36 |
| 114 | SEG42 | 320.50 | -229.50 | 75 | 36 |
| 115 | SEG41 | 320.50 | -178.50 | 75 | 36 |
| 116 | SEG40 | 320.50 | -127.50 | 75 | 36 |
| 117 | COMB3 | 320.50 | -76.50 | 75 | 36 |
| 118 | COMB2 | 320.50 | -25.50 | 75 | 36 |
| 119 | COMB1 | 320.50 | 25.50 | 75 | 36 |
| 120 | COMB0 | 320.50 | 76.50 | 75 | 36 |


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## PAD Coordinates – continued

Unit µm

| PAD No | Terminal Name | Bump Center | | Bump Size | |
|---|---|---|---|---|---|
| | | X | Y | X | Y |
| 121 | SEG39 | 320.50 | 127.50 | 75 | 36 |
| 122 | SEG38 | 320.50 | 178.50 | 75 | 36 |
| 123 | SEG37 | 320.50 | 229.50 | 75 | 36 |
| 124 | SEG36 | 320.50 | 280.50 | 75 | 36 |
| 125 | SEG35 | 320.50 | 331.50 | 75 | 36 |
| 126 | SEG34 | 320.50 | 382.50 | 75 | 36 |
| 127 | SEG33 | 320.50 | 433.50 | 75 | 36 |
| 128 | SEG32 | 320.50 | 484.50 | 75 | 36 |
| 129 | SEG31 | 320.50 | 535.50 | 75 | 36 |
| 130 | SEG30 | 320.50 | 586.50 | 75 | 36 |
| 131 | SEG29 | 320.50 | 637.50 | 75 | 36 |
| 132 | SEG28 | 320.50 | 688.50 | 75 | 36 |
| 133 | SEG27 | 320.50 | 739.50 | 75 | 36 |
| 134 | SEG26 | 320.50 | 790.50 | 75 | 36 |
| 135 | SEG25 | 320.50 | 841.50 | 75 | 36 |
| 136 | SEG24 | 320.50 | 892.50 | 75 | 36 |
| 137 | SEG23 | 320.50 | 943.50 | 75 | 36 |
| 138 | SEG22 | 320.50 | 994.50 | 75 | 36 |
| 139 | SEG21 | 320.50 | 1045.50 | 75 | 36 |
| 140 | SEG20 | 320.50 | 1096.50 | 75 | 36 |
| 141 | SEG19 | 320.50 | 1147.50 | 75 | 36 |
| 142 | SEG18 | 320.50 | 1198.50 | 75 | 36 |
| 143 | SEG17 | 320.50 | 1249.50 | 75 | 36 |
| 144 | SEG16 | 320.50 | 1300.50 | 75 | 36 |
| 145 | SEG15 | 320.50 | 1351.50 | 75 | 36 |
| 146 | SEG14 | 320.50 | 1402.50 | 75 | 36 |
| 147 | SEG13 | 320.50 | 1453.50 | 75 | 36 |
| 148 | SEG12 | 320.50 | 1504.50 | 75 | 36 |
| 149 | SEG11 | 320.50 | 1555.50 | 75 | 36 |
| 150 | SEG10 | 320.50 | 1606.50 | 75 | 36 |
| 151 | SEG9 | 320.50 | 1657.50 | 75 | 36 |
| 152 | SEG8 | 320.50 | 1708.50 | 75 | 36 |
| 153 | SEG7 | 320.50 | 1759.50 | 75 | 36 |
| 154 | SEG6 | 320.50 | 1810.50 | 75 | 36 |
| 155 | SEG5 | 320.50 | 1861.50 | 75 | 36 |
| 156 | SEG4 | 320.50 | 1912.50 | 75 | 36 |
| 157 | SEG3 | 320.50 | 1963.50 | 75 | 36 |
| 158 | SEG2 | 320.50 | 2014.50 | 75 | 36 |
| 159 | DUMMY3 | 320.50 | 2077.60 | 75 | 36 |
| 160 | DUMMY3 | 320.50 | 2128.60 | 75 | 36 |


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

### Absolute Maximum Ratings (VSS = 0V)

| Parameter | Symbol | Ratings | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Maximum Voltage1 | VDD | -0.5 | - | +7.0 | V | Power Supply |
| Supply Current1 | $I_{VDD}$ | -5 | - | +5 | mA | For VDD |
| Maximum Voltage2 | VLCD | -0.5 | - | +7.0 | V | LCD Drive Voltage |
| Supply Current2 | $I_{VLCD}$ | -5 | - | +5 | mA | For VLCD |
| Input Voltage Range | $V_{IN}$ | -0.5 | - | +7.0 | V | - |
| Output Voltage Range | $V_{OUT}$ | -0.5 | - | +7.0 | V | - |
| Human Body Model (HBM) *(Note 1)*, *(Note 2)* | $V_{ESD}$ | - | ±2000 | - | V | - |
| Latch-up Current *(Note 1)*, *(Note 3)* | $I_{LU}$ | - | ±100 | - | mA | - |
| Maximum Junction Temperature | Tjmax | -55 | - | +125 | °C | - |
| Storage Temperature Range | Tstg | -55 | - | +125 | °C | - |

*(Note 1)* Not 100% tested. There is data when LSI was put on a temporary package. Use as a reference data.
*(Note 2)* Testing standards: JESD22-A114E
*(Note 3)* Testing standards: JESD78

***Caution :*** *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

### Recommended Operating Conditions

| Parameter | Symbol | Ratings | | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Operational Temperature | Topr | -40 | - | +105 | °C | - |
| Power Supply Voltage 1 | VDD | 2.7 | - | 6.0 | V | Power Supply |
| Power Supply Voltage 2 | VLCD | 2.7 | - | 6.0 | V | LCD Drive Voltage |


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Electrical Characteristics

### DC Characteristics

(Unless otherwise specified, Ta = -40°C to +105°C, VDD / VLCD = 2.7V to 6.0V, VSS = 0V)

| Parameter | | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| “H” Level Input Voltage1 | | $V_{IH1}$ | 0.7VDD | - | VDD | V | SCL, SDAI |
| “L” Level Input Voltage1 | | $V_{IL1}$ | VSS | - | 0.3VDD | V | |
| “H” Level Input Voltage2 | | $V_{IH2}$ | 0.8VDD | - | VDD | V | CSB, SCK, SDI, INHB, OSCIO*(Note)* |
| “L” Level Input Voltage2 | | $V_{IL2}$ | 0 | - | 0.2VDD | V | |
| “H” Level Input Current | | $I_{IH}$ | - | - | 1 | µA | SCL, SDAI, CSB, SCK, SDI, INHB, OSCIO, TR, MS1, MS2, EXTCLK, IFSEL, DUTY0, DUTY1, BIAS, GLSCHKI |
| “L” Level Input Current | | $I_{IL}$ | -1 | - | - | µA | |
| “H” Level Output Voltage1 | | $V_{OH1}$ | VDD-0.9 | - | VDD | V | SDO, ERROUT (Iload = -1mA) |
| “L” Level Output Voltage1 | | $V_{OL1}$ | VSS | - | 0.9 | V | SDO, ERROUT (Iload = +1mA) |
| “L” Level Output Voltage2 | | $V_{OL2}$ | VSS | - | 0.4 | V | SDAO (Iload = +3mA) |
| LCD Driver On Resistance | SEG | $R_{ON1}$ | - | 3 | - | kΩ | Iload = ±10µA |
| | COM | $R_{ON2}$ | - | 3 | - | kΩ | |
| Standby Current | | $I_{VDD1}$ | - | - | 5.0 | µA | Display Off (DISPOFF), Oscillation stop |
| | | $I_{VLCD1}$ | - | - | 5.0 | µA | |
| Operating Current | | $I_{VDD2}$ | - | 0.5 | 20.0 | µA | VDD = 5.0V, VLCD = 5.0V, Ta = +25°C, 1/4 Duty Drive, 1/3 Bias Frame Inversion FR = 155.3Hz setting (External Clock = 3.42kHz) All outputs are open |
| | | $I_{VLCD2}$ | - | 6.5 | 30.0 | µA | |

*(Note)* For External Clock Mode and slave mode.

[Reference Data]

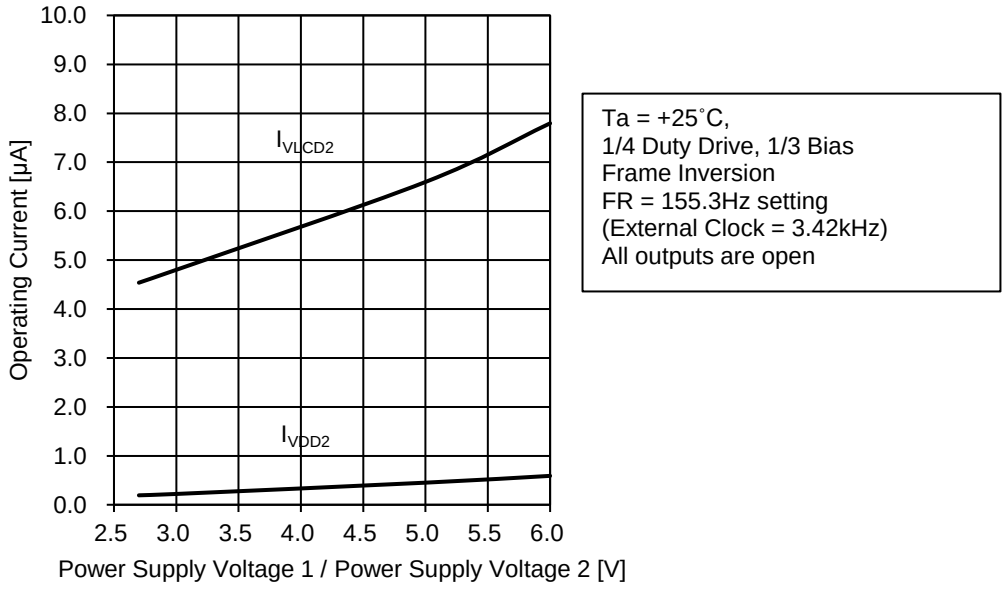



Figure 7. Operating Current vs Power Supply Voltage


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

## Electrical Characteristics – continued

### Oscillation Characteristics

(Unless otherwise specified, Ta = -40°C to +105°C, VDD / VLCD = 2.7V to 6.0V, VSS = 0V)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Frame Frequency 1 | $f_{CLK1}$ | 108.7 | 155.3 | 201.9 | Hz | MODESET3 P0 = "0", FRSET(P2 to P0) = "110" (155.3Hz setting) VDD = 2.7V to 6.0V, Ta = -40°C to +105°C |
| Frame Frequency 2 | $f_{CLK2}$ | 139.8 | 155.3 | 170.8 | Hz | MODESET3 P0 = "0", FRSET(P2 to P0) = "110" (155.3Hz setting) VDD = 5.0V, Ta = -40°C to +105°C |
| External Clock Rise Time | $tr_{CLK}$ | - | - | 0.3 | µs | External Clock Mode |
| External Clock Fall Time | $tf_{CLK}$ | - | - | 0.3 | µs | |
| External Clock Frequency | $f_{CLK3}$ | 800 | - | 12,000 | Hz | |
| External Clock Duty | $t_{DTY}$ | 30 | 50 | 70 | % | |
| Frame Frequency Range in External Clock Mode | $f_{FRAME}$ | 33 | - | 500 | Hz | |

Keep Frame Frequency range from 33Hz to 500Hz in case of External Clock Mode, also keep external clock frequency range from 800Hz to 12,000Hz.
The calculation formula is shown in **4. Frame Rate Set (FRSET)**.

[Reference Data]

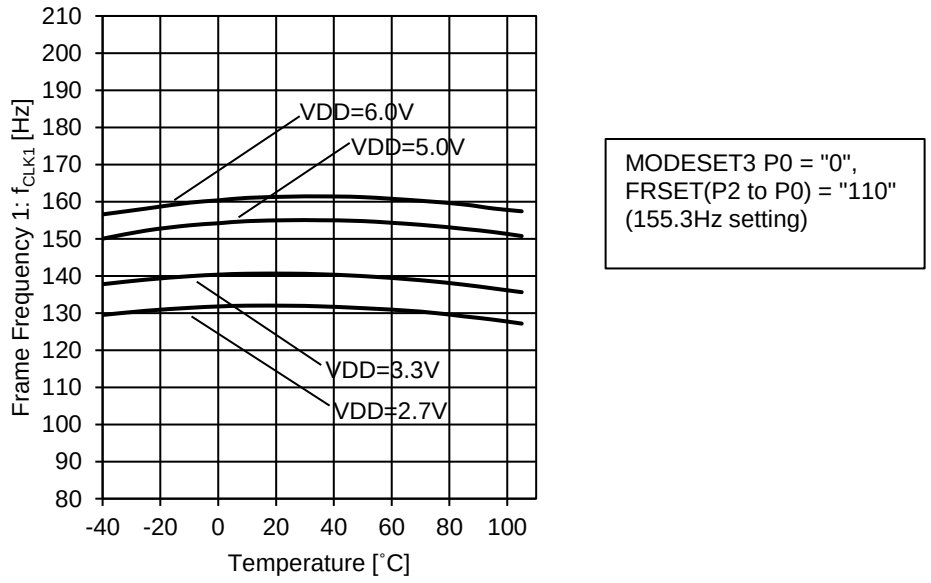



Figure 8. Frame Frequency vs Temperature


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

## Electrical Characteristics – continued

### 2-wire Serial Interface Characteristics

(Unless otherwise specified, Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0V)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input Rise Time | tr | - | - | 0.3 | µs | - |
| Input Fall Time | tf | - | - | 0.3 | µs | - |
| SCL Cycle Time | $t_{CYC}$ | 2.5 | - | - | µs | - |
| “H” Level SCL Pulse Width | $t_{SHW}$ | 0.6 | - | - | µs | - |
| “L” Level SCL Pulse Width | $t_{SLW}$ | 1.3 | - | - | µs | - |
| SDA Setup Time | $t_{SDS}$ | 0.1 | - | - | µs | - |
| SDA Hold Time | $t_{SDH}$ | 0.1 | - | - | µs | - |
| Bus Free Time | $t_{BUF}$ | 1.3 | - | - | µs | - |
| START Condition Hold Time | $t_{HD;STA}$ | 0.6 | - | - | µs | - |
| START Condition Setup Time | $t_{SU;STA}$ | 0.6 | - | - | µs | - |
| STOP Condition Setup Time | $t_{SU;STO}$ | 0.6 | - | - | µs | - |

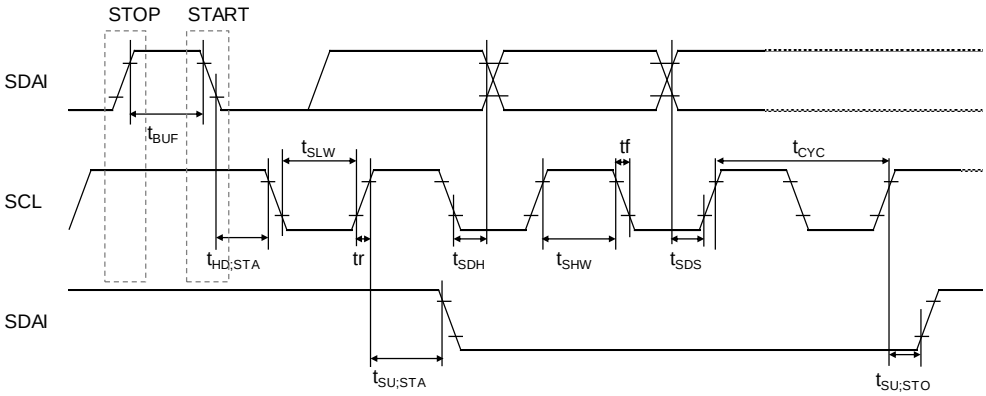
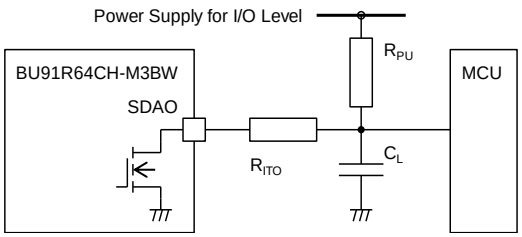



Figure 9. Interface Timing of 2-wire Serial Interface

Since SDAO is an open-drain output, Read access time depends on ITO resistance $R_{ITO}$, Pull-up resistance $R_{PU}$ and load capacitance $C_L$.

$R_{ITO}$: ITO resistance on the LCD glass. (Any component is not necessary to be attached.)
$R_{PU}$: Pull-up resistance on PCB. 1kΩ ≤ $R_{PU}$ ≤ 10kΩ is recommended.
$C_L$: A parasitic capacitance to VSS in an application circuit. (Any component is not necessary to be attached.)

$R_{PU}$ should be determined with consideration of $V_{IL}$ in MCU side.





© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

## Electrical Characteristics – continued

### 3-wire Serial Interface Characteristics

(Unless otherwise specified, Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0V)

| Parameter | Symbol | Limits | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input Rise Time | tr | - | - | 80 | ns | - |
| Input Fall Time | tf | - | - | 80 | ns | - |
| SCK Cycle Time | $t_{SCYC}$ | 400 | - | - | ns | - |
| “H” Level SCK Pulse Width (Write) | $t_{SHWW}$ | 120 | - | - | ns | Write Access |
| “H” Level SCK Pulse Width (Read) | $t_{SHWR}$ | 200 | - | - | ns | Read Access |
| “L” Level SCK Pulse Width (Write) | $t_{SLWW}$ | 120 | - | - | ns | Write Access |
| “L” Level SCK Pulse Width (Read) | $t_{SLWR}$ | 1.6 | - | - | µs | Read Access |
| SDI Setup Time | $t_{SDS}$ | 120 | - | - | ns | - |
| SDI Hold Time | $t_{SDH}$ | 120 | - | - | ns | - |
| CSB Setup Time | $t_{CSS}$ | 120 | - | - | ns | - |
| CSB Hold Time | $t_{CSH}$ | 120 | - | - | ns | - |
| “H” CSB Pulse Width | $t_{CHW}$ | 120 | - | - | ns | - |
| SDO Output Delay Time | $t_{DC}$ | - | - | 1.5 | µs | $R_{ITO}$ = 1.0kΩ, $C_L$ = 10pF |
| SDO Rise Time | $t_{DR}$ | - | - | 1.5 | µs | $R_{ITO}$ = 1.0kΩ, $C_L$ = 10pF |

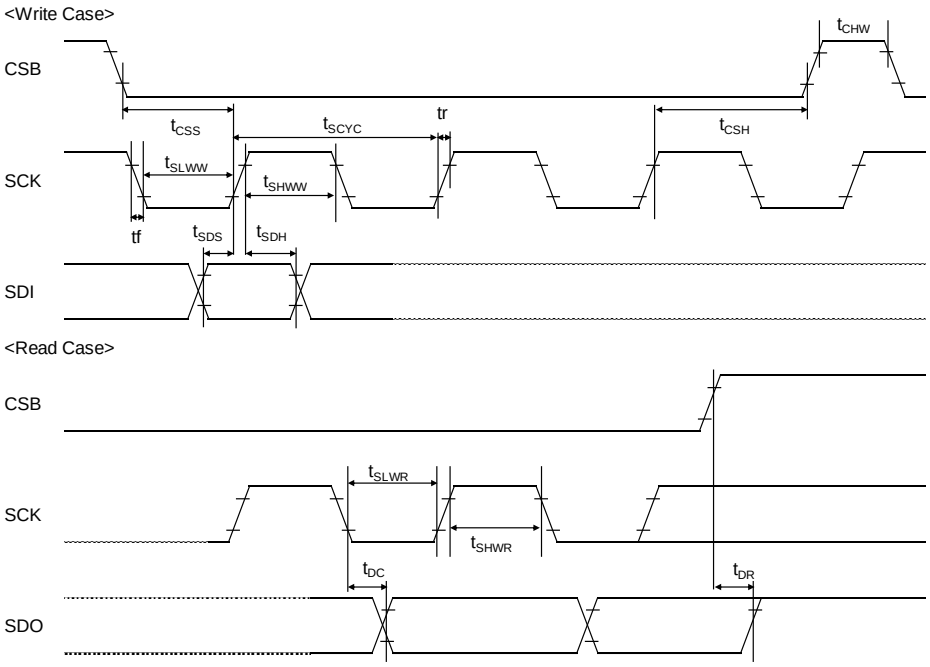
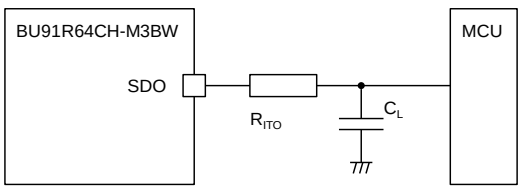



Figure 10. Interface Timing of 3-wire Serial Interface

“$t_{DC}$” and “$t_{DR}$” depend on ITO resistance $R_{ITO}$ and load capacitance $C_L$.

$R_{ITO}$: ITO resistance on the LCD glass. (Any component is not necessary to be attached.)

$C_L$: A parasitic capacitance to VSS in an application circuit. (Any component is not necessary to be attached.)





© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

### I/O Equivalence Circuit

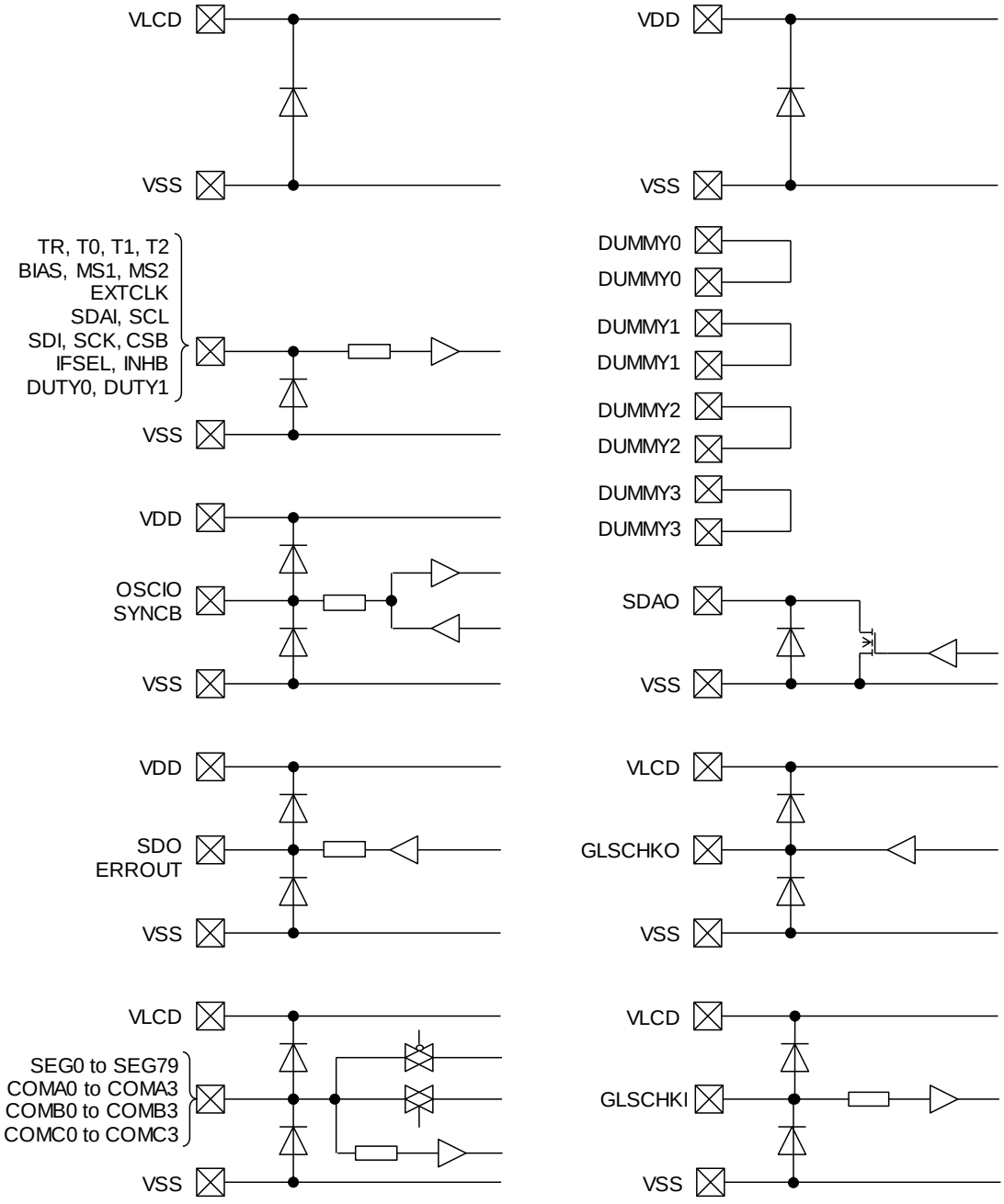



Figure 11. I/O Equivalence Circuit


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## MCU Interface

BU91R64CH-M3BW supports two MCU Interfaces. In IFSEL = VSS, 2-wire Serial Interface (hereinafter referred to as "2-wire") is available. And in IFSEL = VDD, 3-wire Serial Interface (hereinafter referred to as "3-SPI") is available.

### START and STOP Condition (2-wire)

In IFSEL = VSS, BU91R64CH-M3BW is controlled by 2-wire signals (SDAI, SCL).
It is necessary to generate "START condition" and "STOP condition" when sending command or Display Data.

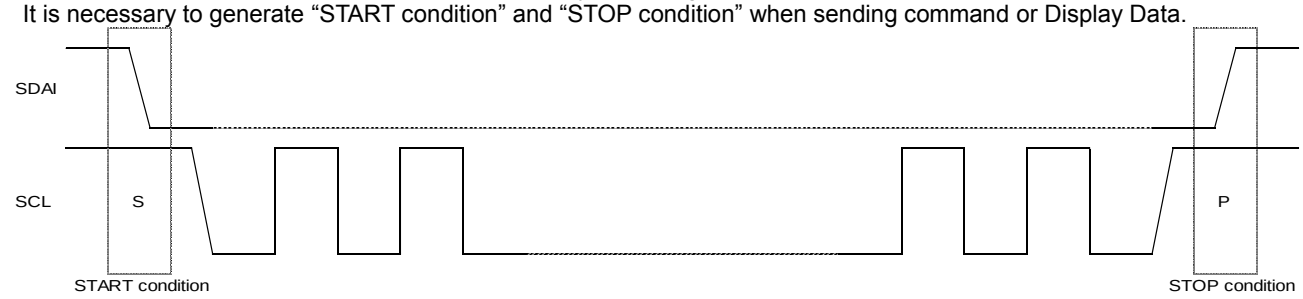



Figure 12. 2-wire Command / Data Transfer Format

### Acknowledge (ACK) (2-wire)

Data format is comprised of 8-bit data to SDAI. And an acknowledge bit is returned from SDAO terminal after 8-bit data sent. SDAO is also used in Display Data read-back and Command Registers read-back. The serial data input line (SDAI) and the serial data output line (SDAO) are separated in PAD assignment, but both terminals can be connected together to facilitate a single line SDA.

After the transfer of 8-bit data (Slave Address, Control Byte, Command, Display Data), release the SDA line at the falling edge of the eighth clock. The SDA line is then pulled low until the falling edge of the ninth clock SCL. (Output cannot be pulled high because of open-drain NMOS output structure). If the acknowledge function is not required, keep SDA line at low level from the eighth falling edge to the ninth falling edge of SCL.

Not acknowledged bit (NACK) will be returned in following cases.

(1) Incorrect Slave Address
(2) Different Sub Address (in receiving Display Data, CNTSET and COMSET commands)

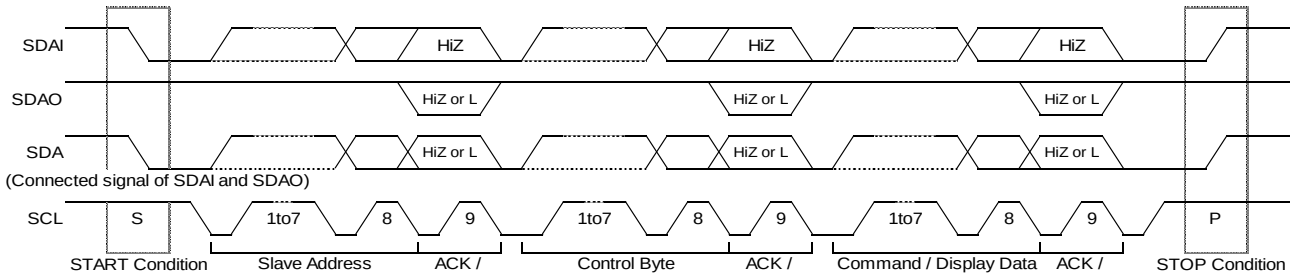



Figure 13. Acknowledge Timing

When Slave Address cannot be recognized correctly in the first data transfer, NACK will be generated and next transfer will be invalid. Even in the invalid status, BU91R64CH-M3BW will return to valid status by receiving "START condition" again.

Consider MCU Interface Characteristics such as Input rise time and Setup / Hold time when transferring command and data. Refer to **2-wire Serial Interface Characteristics**.

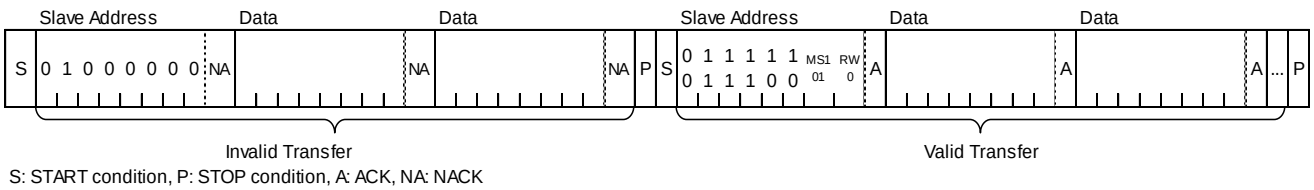



Figure 14. Wrong Slave Address Case


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## MCU Interface - continued

### Command / Display Data Transfer Method (2-wire)

Issue Slave Address after generating “START condition”. The first byte after Slave Address must be Control Byte. The Control Byte consists of 8bits: CO, RS, and 6 undefined bits. The first bit is CO: continuous data bytes / single data byte selector and the second bit is RS: Command / Display Data selector and the others are undefined bits.

| CO | Function |
|---|---|
| 0 | Continuous data bytes available after the Control Byte. |
| 1 | Only single data byte available after the Control Byte.<br>After the data byte, Control Byte can be accepted again. |

| RS | Function |
|---|---|
| 0 | Command is received after the Control Byte. |
| 1 | Display Data is received after the Control Byte.<br>Continuous Display Data is available regardless of CO value. |

The following procedure shows how to transfer Command and Display Data.

(1) Generate “START condition”.
(2) Issue Slave Address. *(Note 1)*
(3) Transfer Control Byte.
(4) Transfer Command and Display Data.
(5) Generate “STOP condition”.

*(Note 1)* Slave Address is specified by MS1 setting. (2-wire mode only)

| MS1 | Slave Address [7:1] |
|---|---|
| 0 | 0111110 / 0111000 |
| 1 | 0111111 / 0111001 |

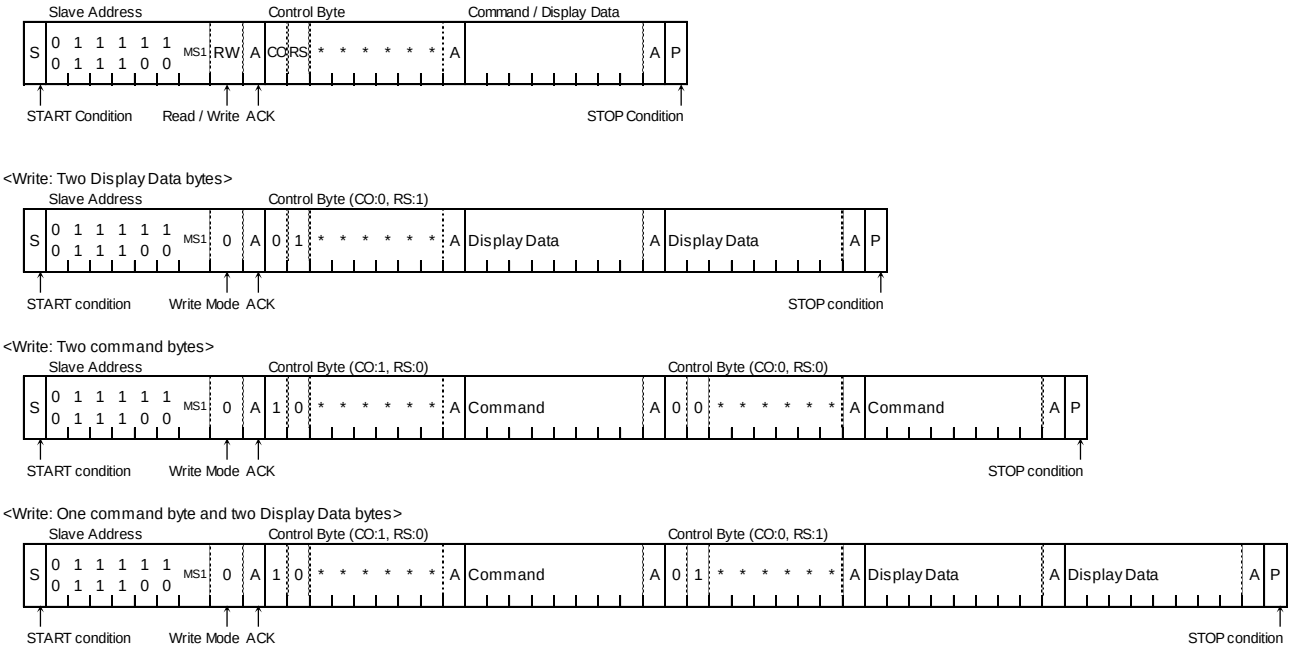



Figure 15. 2-wire Interface Protocol

BU91R64CH-M3BW cannot accept Control Byte / Command once it enters into continuous data transfer state. “STOP condition” and “START condition” are necessary in order to accept Command again. If “START condition” or “STOP condition” is received during Command / Display Data transfer, the byte in transferring will be cancelled.
Then if Slave Address is received after the “START condition”, BU91R64CH-M3BW enters into Control Byte transfer state.

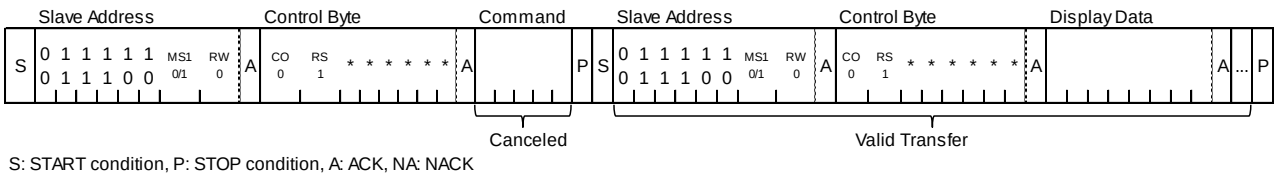



Figure 16. Wrong Slave Address Case


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## MCU Interface - continued

### Display Data Transfer Method (2-wire)

For Display Data write, set R/W bit in Slave Address byte to '0' (Write Mode) and Bit6 in Control Byte to '1'. BU91R64CH-M3BW has a Display Data RAM (DDRAM) of 80×4 = 320-bit. SADSET and ADSET commands specify the address where the first Display Data Byte is written. The address is automatically incremented in every 4-bit data and the Display Data is written to DDRAM at the same timing. Smaller Display Data than 4-bit will be cancelled in the transfer.

Burst write into DDRAM is available by transferring data continuously. The address is returned to 00h by the auto-increment function after writing Display Data to the last address. BU91R64CH-M3BW escapes from the burst mode by STOP condition. Ex) in 1/4 Duty Drive, the address is returned to 00h (for SEG0) after writing data into address = 4Fh (for SEG79). In case of Static Drive Mode, maximum address is 13h (for SEG76 to SEG79).

The relationships between input Display Data, DDRAM address map and SEG output are as follows.

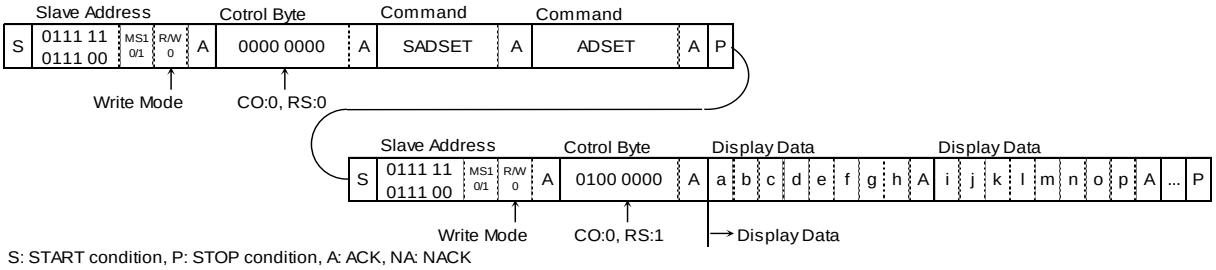



Figure 17. Display Data Transfer in 2-wire

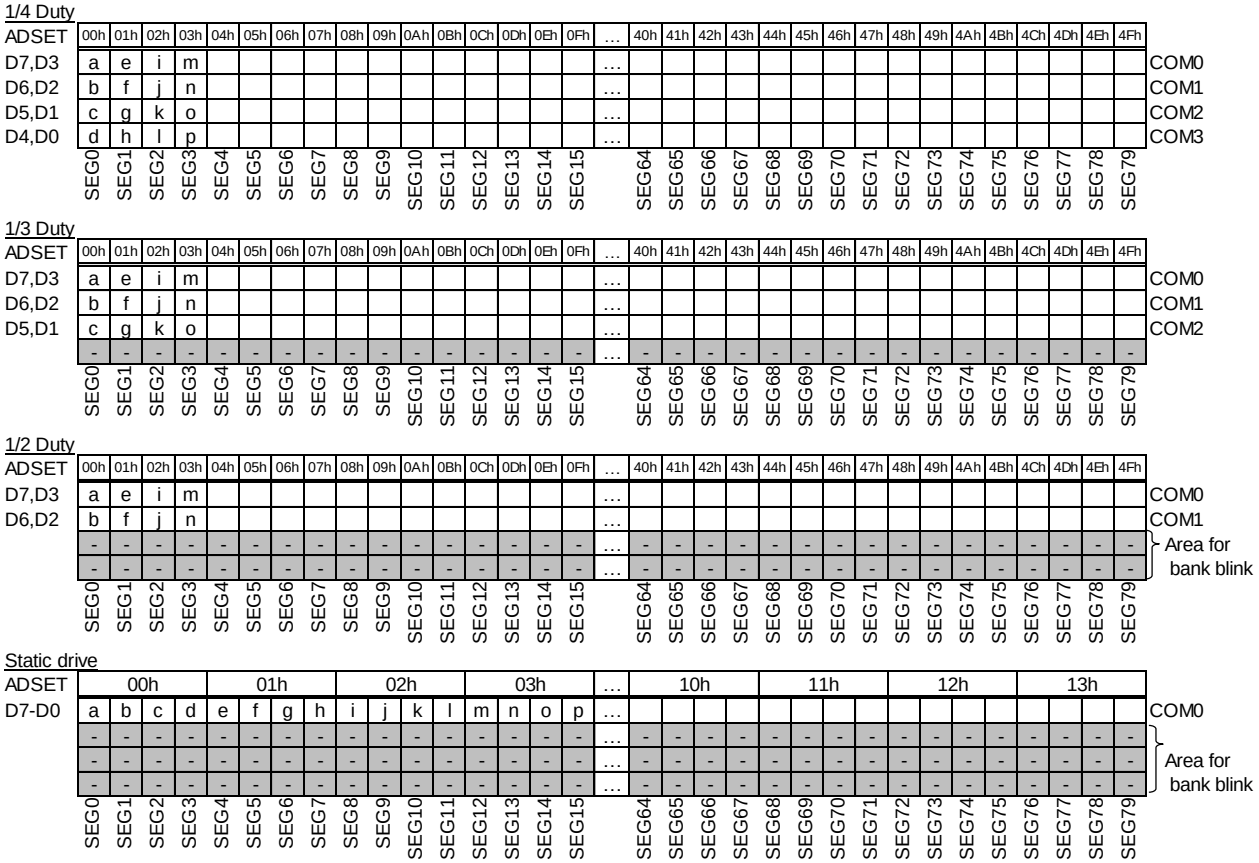



Figure 18. DDRAM Address Map in Write Mode


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

## MCU Interface - continued

### Display Data Read-back Method (2-wire)

For Read Mode, set R/W bit in Slave Address byte to '1'. In advance, Read_data bit in RDCTL must be set to '1' for reading Display Data. The Display Data values can be read during Read Mode. The sequence of the Display Data read-back is shown below.

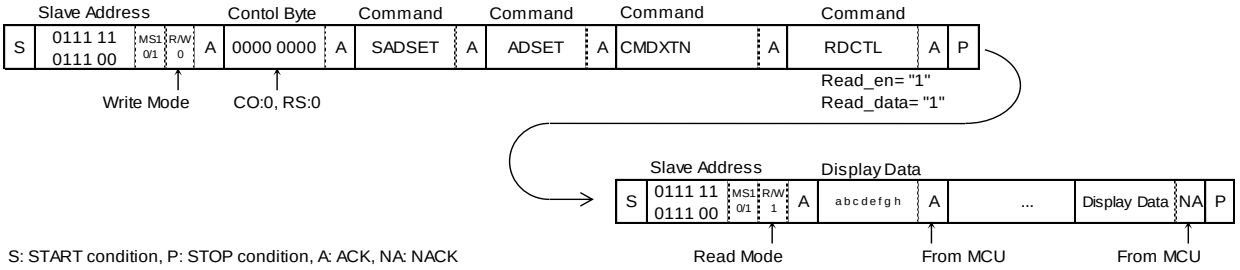



Figure 19. Display Data Read-back in 2-wire

During Read Mode, the Display Data can be read from the DDRAM through the SDAO line. The data will output synchronized with falling edge of SCL input.
SADSET and ADSET must be set first during Write Mode in advance. If DDRAM address is not specified before Display Data read, the current DDRAM address is used as the first read address. Address will be incremented automatically by +2 addresses after 8-bit data output. The Address will be set to 00h automatically after maximum address.
MCU must reply ACK to BU91R64CH-M3BW after each 8-bit data output to keep Read Mode. If MCU replies no ACK response (NACK), BU91R64CH-M3BW will escape Read Mode and SDAO output status will be released.

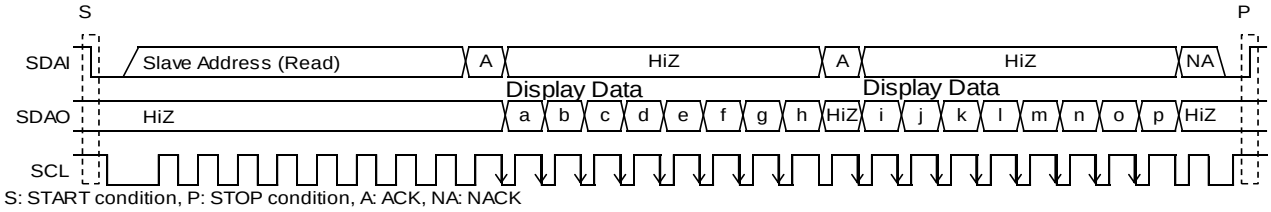



Figure 20. Bit-Assignment in Display Data Read-back in 2-wire

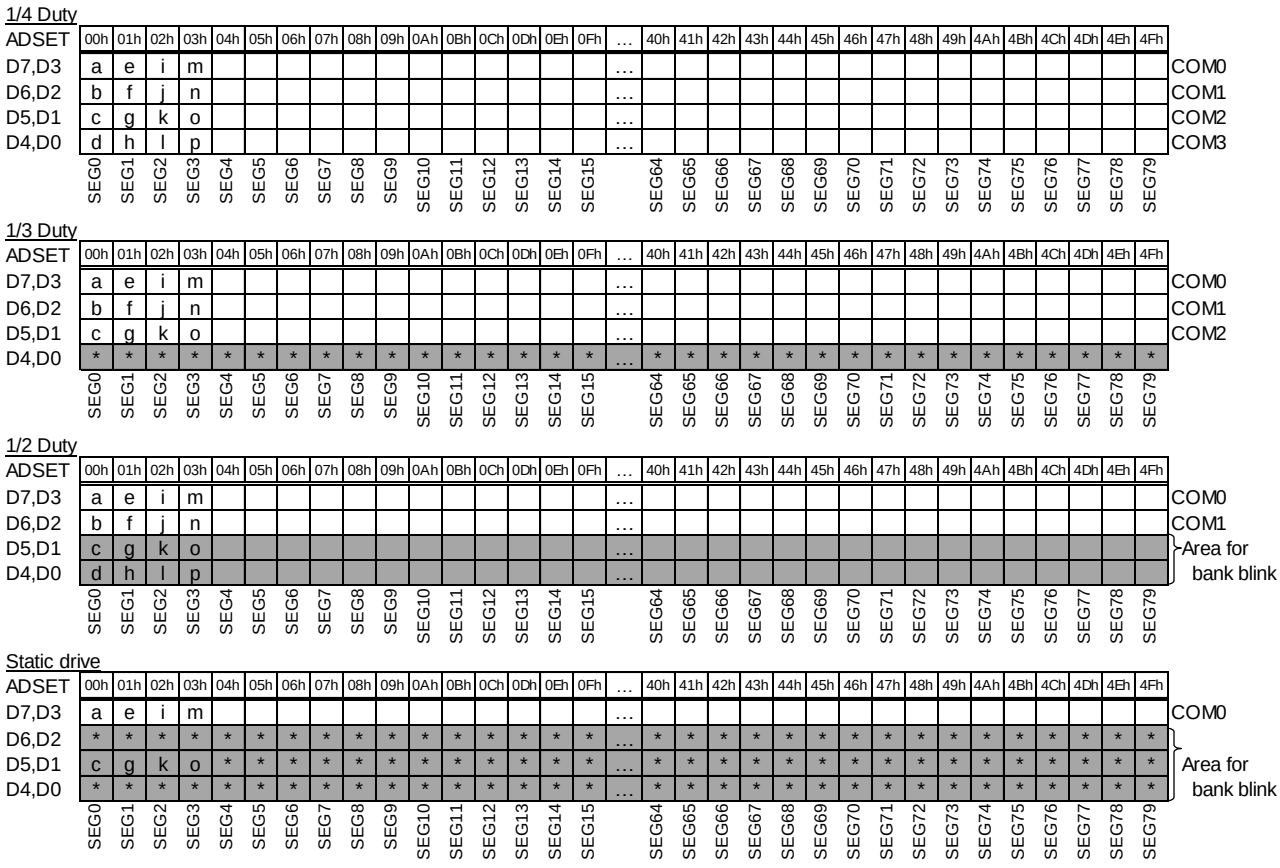



Figure 21. DDRAM Address Map in Read Mode


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

## MCU Interface - continued

### Command Registers Read-back Method (2-wire)

For Read Mode, set R/W bit in Slave Address bye to '1'. In advance, Read_data bit in RDCTL must be set to '0' for reading Command Registers. The Command Registers can be read during Read Mode. The sequence of the Command Registers read-back is shown below and is similar to the Display Data read sequence.

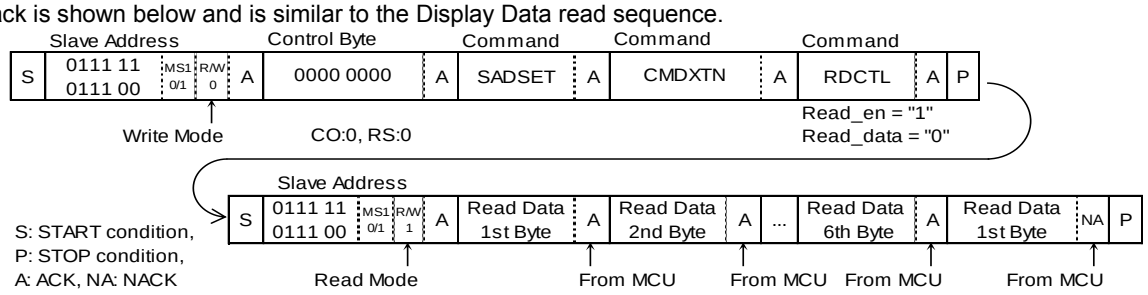



Figure 22. Command Registers Read-back Method in 2-wire

After the sixth byte data, the first byte data will be outputted again. Command Registers read-back mode can be released at NACK condition (Same as Read Display Data).

Table 5. Command Registers Map for Read-back

| Byte | Bit | Read Data | Remark |
|---|---|---|---|
| 1st Byte | D7 | Enable for Glass Breaking Detection | MODESET2 P3 |
| | D6 | Enable for Interface Checksum Detection | MODESET2 P2 |
| | D5 | Enable for Logic Error Detection | MODESET2 P1 |
| | D4 | Enable for SEG / COM Toggle Detection | MODESET2 P0 |
| | D3 | Status of Glass Breaking Detection | 1: Abnormal, 0: Normal |
| | D2 | Status of Interface Checksum Detection | 1: Abnormal, 0: Normal |
| | D1 | Status of Logic Error Detection | 1: Abnormal, 0: Normal |
| | D0 | Status of SEG / COM Toggle Detection | 1: Abnormal, 0: Normal |
| 2nd Byte | D7 | Display On | MODESET1 P3 |
| | D6 | Blink Mode | BLKCTL1 P2 |
| | D5 | 2x frequency in frame Inversion | MODESET3 P1 |
| | D4 | Inversion Mode | MODESET3 P2 |
| | D3 | Higher Frequency Mode | MODESET3 P0 |
| | D2 | Frame Rate Bit2 | FRSET P2 |
| | D1 | Frame Rate Bit1 | FRSET P1 |
| | D0 | Frame Rate Bit0 | FRSET P0 |
| 3rd Byte | D7 | Blink Freq. Bit1 | BLKCTL1 P1 |
| | D6 | Blink Freq. Bit0 | BLKCTL1 P0 |
| | D5 | Blink Area Select | BLKCTL2 P1 |
| | D4 | EVR Bit4 | COMSET P3 |
| | D3 | EVR Bit3 | CNTSET P3 |
| | D2 | EVR Bit2 | CNTSET P2 |
| | D1 | EVR Bit1 | CNTSET P1 |
| | D0 | EVR Bit0 | CNTSET P0 |
| 4th Byte | D7 | IFCHKSUM Bit3 | CHKSUM P3 |
| | D6 | IFCHKSUM Bit2 | CHKSUM P2 |
| | D5 | IFCHKSUM Bit1 | CHKSUM P1 |
| | D4 | IFCHKSUM Bit0 | CHKSUM P0 |
| | D3 | 0 | - |
| | D2 | COMSET Bit2 | COMSET P2 |
| | D1 | COMSET Bit1 | COMSET P1 |
| | D0 | COMSET Bit0 | COMSET P0 |
| 5th Byte | D7 | 0 | - |
| | D6 | 0 | - |
| | D5 | Sub Address Set Bit1 | SADSET P1 |
| | D4 | Sub Address Set Bit0 | SADSET P0 |
| | D3 | 0 | - |
| | D2 | 0 | - |
| | D1 | 0 | - |
| | D0 | 0 | - |
| 6th Byte | D7 | 0 | - |
| | D6 | Address Set Bit6 | ADSET P6 |
| | D5 | Address Set Bit5 | ADSET P5 |
| | D4 | Address Set Bit4 | ADSET P4 |
| | D3 | Address Set Bit3 | ADSET P3 |
| | D2 | Address Set Bit2 | ADSET P2 |
| | D1 | Address Set Bit1 | ADSET P1 |
| | D0 | Address Set Bit0 | ADSET P0 |


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## MCU Interface - continued

### Command / Display Data Transfer Method (3-SPI)

In IFSEL = VDD, BU91R64CH-M3BW is controlled by 3-wire signals (CSB, SCK, and SDI). First, Interface counter is initialized with CSB =high then CSB =low enables SDI and SCK input.
D7 to D0 follows continuously after CSB =low. Internal data is latched at the rising edge of SCK. Command is converted to 8-bit parallel data at the rising edge of the eighth SCK. Display Data is stored at the fourth and the eighth falling edge of SCK. The protocol of 3-SPI transfer is as follows.

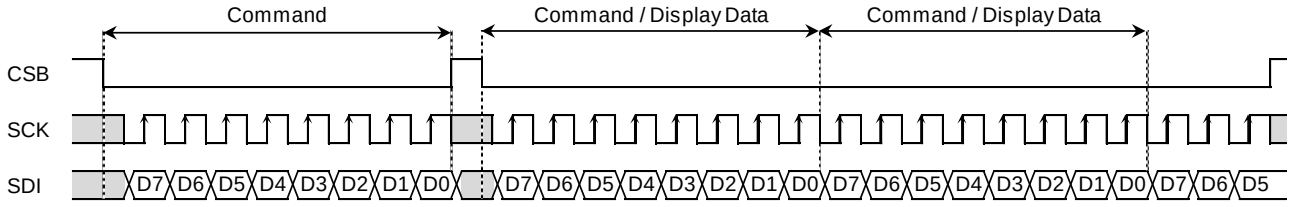



Figure 23. Command / Data Transfer in 3-SPI Command / Data Transfer in 3-SPI

### Command Transfer Method (3-SPI)

After CSB changes from high to low, the first byte is always a command input. To escape Display Data transfer condition or to send command again, CSB should be set from low to high then set to low.

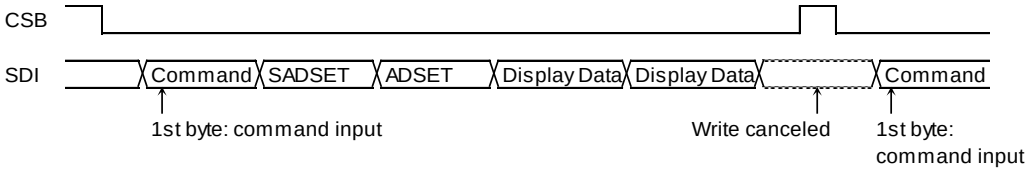



Figure 24. Escape from Data Transfer Condition in 3-SPI

Command transfer is done by 8-bit unit, so if CSB is set from low to high with less than 8-bit data transfer, command will be cancelled. It will be able to transfer command when CSB= low again.

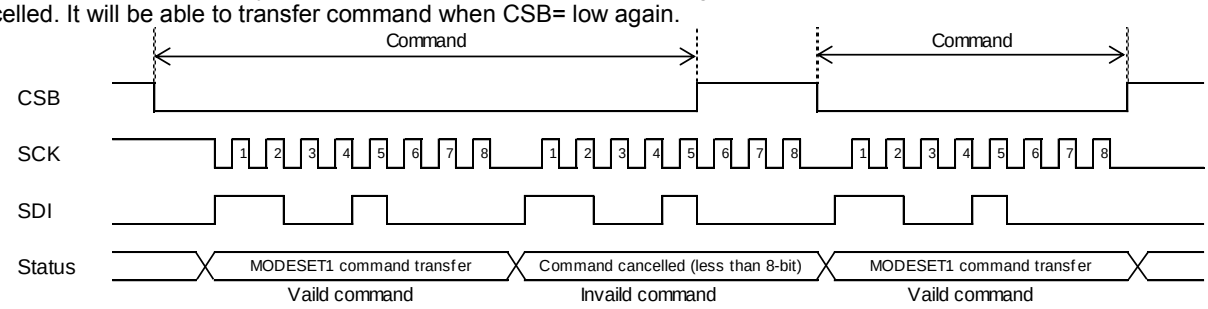



Figure 25. Case of Less Than 8-bit Data Transfer in 3-SPI


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## MCU Interface - continued

### Display Data Transfer Method (3-SPI)

In 3-SPI, BU91R64CH-M3BW enters to Display Data write state after receiving ADSET command. BU91R64CH-M3BW has a Display Data RAM (DDRAM) of 80×4 = 320-bit. SADSET and ADSET commands specify the address where the first Display Data Byte is written. The address is automatically incremented in every 4-bit data and the Display Data is written to DDRAM at the same timing. Smaller Display Data than 4-bit will be cancelled in the transfer.

Burst write into DDRAM is available by transferring data continuously. The address is returned to 00h by the auto-increment function after writing Display Data to the last address. BU91R64CH-M3BW escapes from the burst mode by setting CSB to high.

Ex) in 1/4 Duty Drive mode, the address is returned to 00h (for SEG0) after writing Display Data into address = 4Fh (for SEG79). In case of Static Drive Mode, maximum address is 13h (for SEG76 to SEG79).

The DDRAM address map is same as the one in 2-wire Serial Interface (Refer to **Figure 18. DDRAM Address Map in Write Mode**).

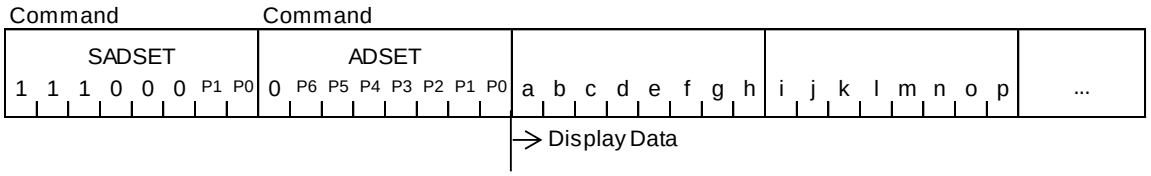



Figure 26. Display Data Transfer and Bit Assignment in 3-SPI

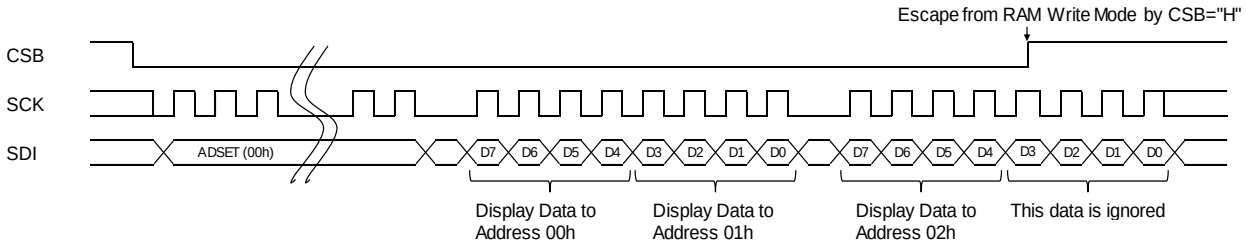



Figure 27. Case of Less Than 4-bit Write Data Transfer in 3-SPI


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## MCU Interface - continued

### Display Data Read-back Method (3-SPI)

Set Read_en = “1” and Read_data = “1” in RDCTL register to enter to Display Data Read Mode. The Display Data values can be read during this mode. The sequence of the Display Data read-back is shown below.

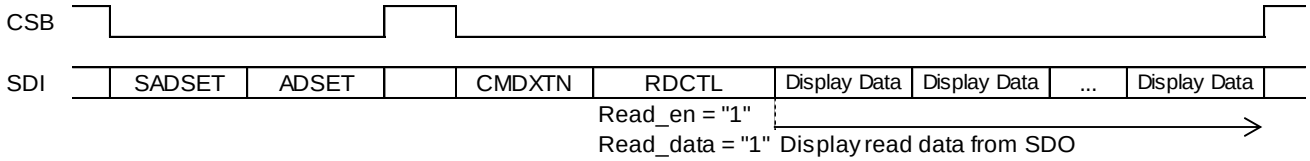



Figure 28. Display Data Read-back in 3-SPI

During Display Data Read Mode, the Display Data can be read from the DDRAM through the SDO line. The data will output synchronized with falling edge of SCK input.
SADSET and ADSET must be set first during Write Mode in advance. If DDRAM address is not specified before Display Data read, the current DDRAM address is used as the first read address. Address will be incremented automatically by +2 addresses after 8-bit data output. The Address will be set to 00h automatically after maximum address. Display Data Read Mode will be released by setting CSB to high (SDO output also be stopped).
The DDRAM address map is same as the one in 2-wire Serial Interface (Refer to **Figure 21. DDRAM Address Map in Read Mode**).

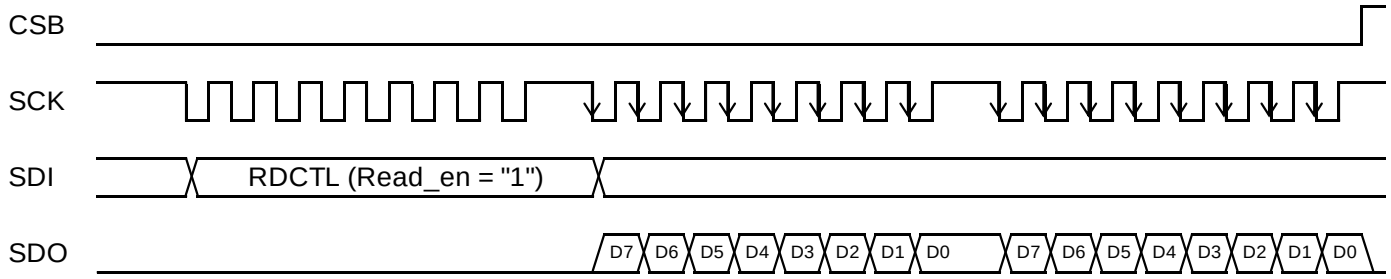



Figure 29. Display Data Read-back in 3-SPI

### Command Registers Read-back Method (3-SPI)

Set Read_en = “1” and Read_data = “0” in RDCTL register to enter Command Registers Read Mode. The Command Registers values can be read during this mode. The sequence of the Command Registers read-back is shown below.

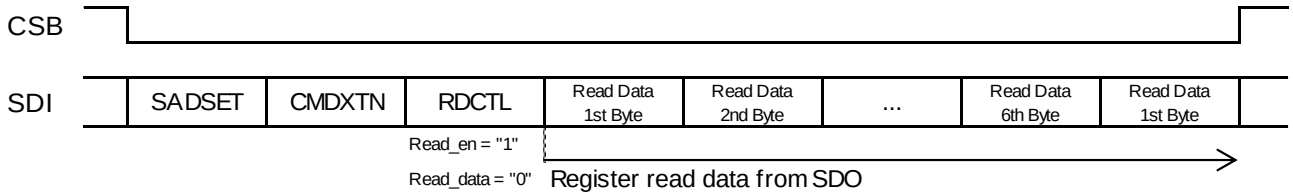



Figure 30. Command Registers Read-back in 3-SPI

After reading the 6th byte data, the first byte data will be output again. Command Registers Read Mode will be released after CSB change from low to high. (SDO stops).
The Command Registers Map is same as the one in 2-wire. Refer to **Table 5. Command Registers Map for Read-back**.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

### OSC (Oscillator)

In master chip (MS1 = VSS and MS2 = VSS), the clock mode can be selected by EXTCLK. The clock signals for logic and analog circuit can be generated in internal oscillator if EXTCLK = VSS or can be provided from external clock input if EXTCLK = VDD.

| Clock Mode | EXTCLK | OSCIO |
|---|---|---|
| Internal Clock Mode | VSS | To Output Internal Generated Clock Signal |
| External Clock Mode | VDD | To Input External Clock |

In cascaded connection, slave chip (MS1 = VDD or MS2 = VDD) is always in External Clock Mode regardless of EXTCLK.

In case of External Clock Mode, a clock signal should be always supplied to BU91R64CH-M3BW. Removing the clock may freeze the LCD in a DC state which is not suitable for the LCD.

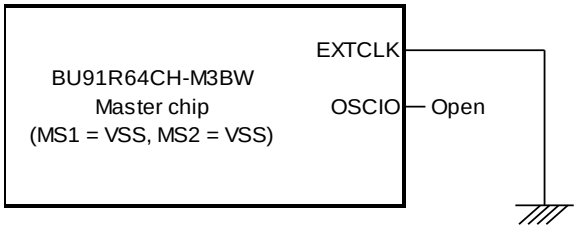



Figure 31. Internal Clock Mode

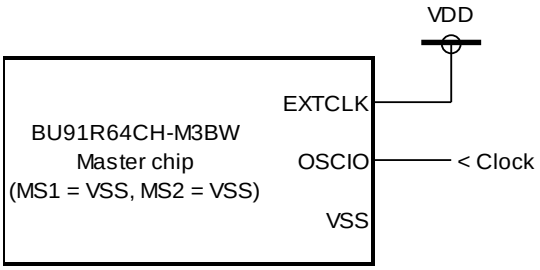



Figure 32. External Clock Mode


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## SYNC CTRL (Multi-chip Structure)

BU91R64CH-M3BW supports large display application by connecting up to four IC in cascade. BU91R64CH-M3BW can be combined with BU91R65CH-M3BW and BU91R66CH-M3BW.
The relationship of MS1 / MS2 setting, OSCIO, SYNCB and SADSET are shown below. To synchronize each IC, connect the synchronizing signal (SYNCB) and the synchronous clock (OSCIO) from the Master to Slave ICs.

In case of 2-wire Serial Interface

| MS2 | MS1 | Mode | Slave Address [7:1] | OSCIO | | | | SYNCB | | SADSET (P1,P0) |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | EXTCLK = VDD *(Note 1)* | | EXTCLK = VSS *(Note 2)* | | | | |
| | | | | I/O | Connected to | I/O | Connected to | I/O | Connected to | |
| VSS | VSS | Master | 0111 110 / 0111 000 | IN | MCU | OUT | Slave1 to Slave3 (OSCIO) | OUT | Slave1 to Slave3 (SYNCB) | (0,*) |
| VSS | VDD | Slave1 | 0111 111 / 0111 001 | IN | MCU | IN | Master (OSCIO) | IN | Master (SYNCB) | (0,*) |
| VDD | VSS | Slave2 | 0111 110 / 0111 000 | IN | MCU | IN | Master (OSCIO) | IN | Master (SYNCB) | (1,*) |
| VDD | VDD | Slave3 | 0111 111 / 0111 001 | IN | MCU | IN | Master (OSCIO) | IN | Master (SYNCB) | (1,*) |

(*: don't care)
*(Note 1)* Frame rate is fixed (24 clock / frame) regardless of FRSET and MODESET3.
*(Note 2)* Frame rate depends on FRSET and MODESET3. All of Master and Slave1 to Slave3 must be same setting in the registers.

In case of 3-wire Serial Interface

| MS2 | MS1 | Mode | OSCIO | | | | SYNCB | | SADSET (P1,P0) |
|---|---|---|---|---|---|---|---|---|---|
| | | | EXTCLK = VDD *(Note 1)* | | EXTCLK = VSS *(Note 2)* | | | | |
| | | | I/O | Connected to | I/O | Connected to | I/O | Connected to | |
| VSS | VSS | Master | IN | MCU | OUT | Slave1 to Slave3 (OSCIO) | OUT | Slave1 to Slave3 (SYNCB) | (0, 0) |
| VSS | VDD | Slave1 | IN | MCU | IN | Master (OSCIO) | IN | Master (SYNCB) | (0, 1) |
| VDD | VSS | Slave2 | IN | MCU | IN | Master (OSCIO) | IN | Master (SYNCB) | (1, 0) |
| VDD | VDD | Slave3 | IN | MCU | IN | Master (OSCIO) | IN | Master (SYNCB) | (1, 1) |

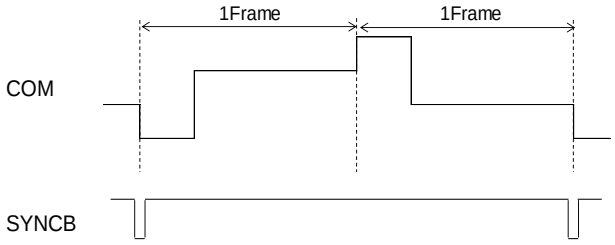
*(Note 1)* Frame rate is fixed (24 clock / frame) regardless of FRSET and MODESET3.
*(Note 2)* Frame rate depends on FRSET and MODESET3. All of Master and Slave1 to Slave3 must be same setting in the registers.


© 2016 ROHM Co., Ltd. All rights reserved.

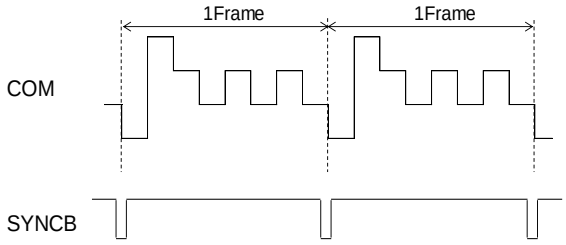
Downloaded from Arrow.com.

### SYNC CTRL (Multi-chip Structure) - continued

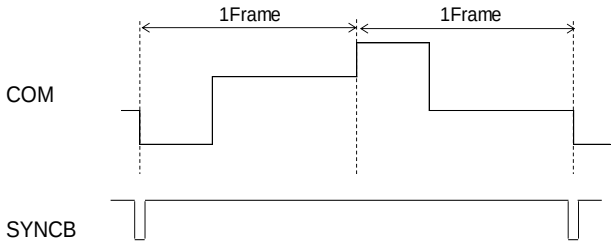
The relationship between COM and SYNCB timing is as follows.



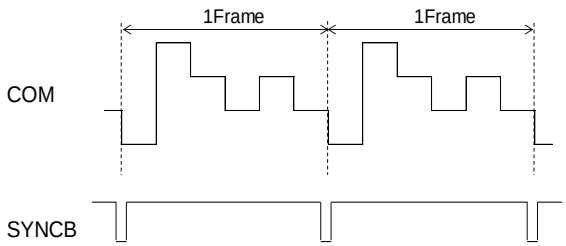

(a-1) 1/4 Duty Drive and Frame Inversion



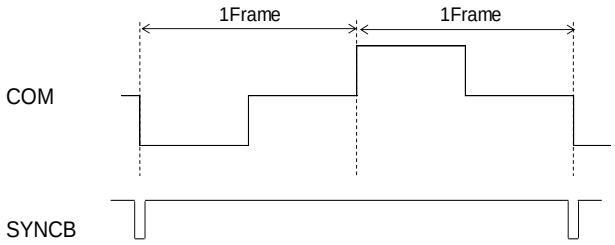

(a-2) 1/4 Duty Drive and Line Inversion



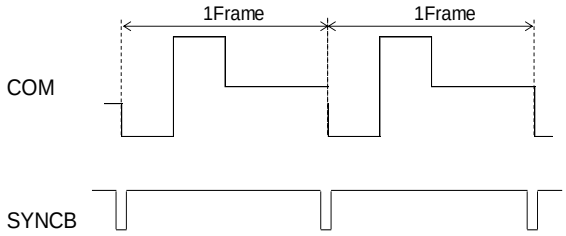

(b-1) 1/3 Duty Drive and Frame Inversion



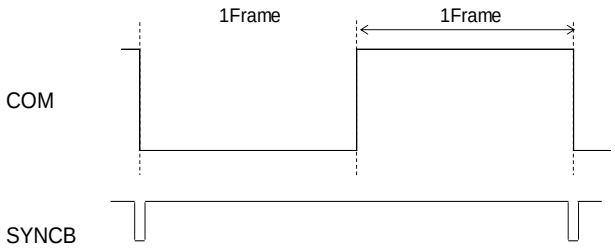

(b-2) 1/3 Duty Drive and Line Inversion



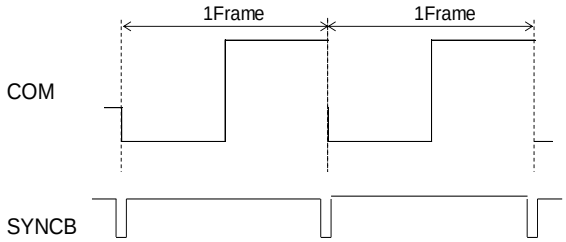

(c-1) 1/2 Duty Drive and Frame Inversion (1/2bias)



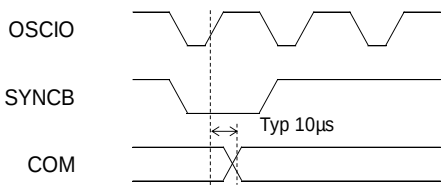

(c-2) 1/2 Duty Drive and Line Inversion (1/2bias)




(d-1) Static Drive and Frame Inversion




(d-2) Static Drive and Line Inversion




(e) Driver timing waveform

In Blink Mode,
SYNCB "L" pulse width will be twice longer
to synchronize normal and blink display .

Figure 33. Synchronization of Multi-chip Cascaded Connection

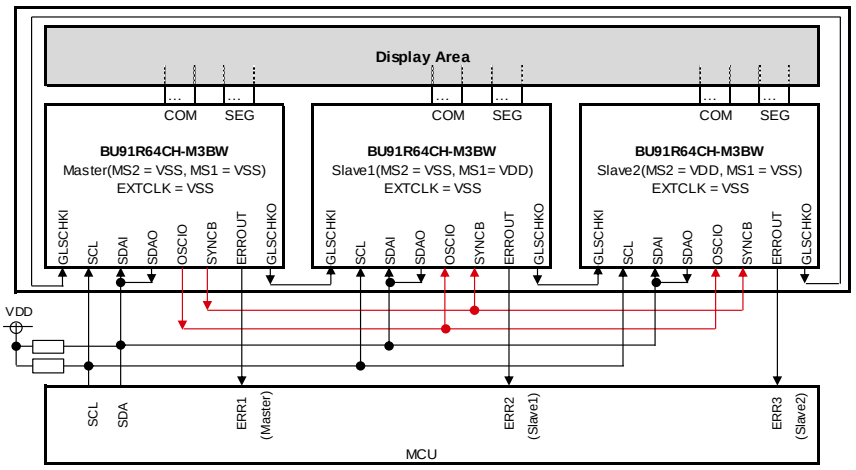

© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

## SYNC CTRL (Multi-chip Structure) - continued

The example of cascaded connection

<2-wire serial, Internal Clock Mode, Detection enable>




<3-wire serial, External Clock Mode, Detection disable>

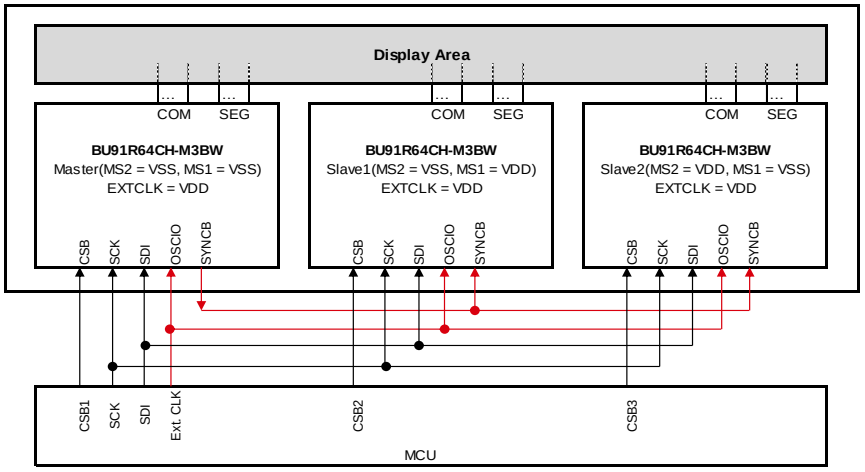



Figure 34. Example of Cascaded Connection

<Different Duty Panel Combination>

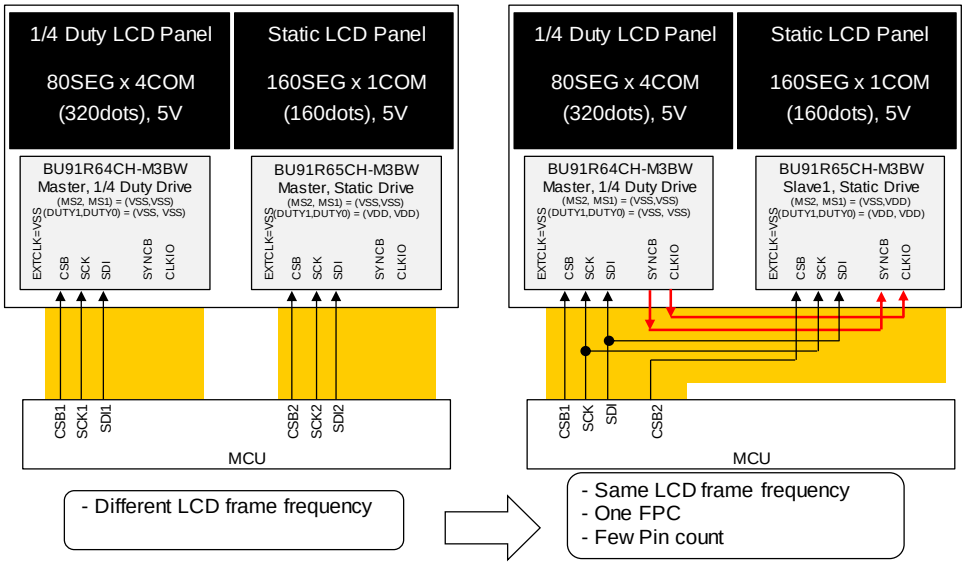



Figure 35. Example Different Duty Drive Panel Configuration


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## LCD Driver Voltage Generator / LCD Bias Selector

BU91R64CH-M3BW generates LCD driving voltage with on-chip Buffer AMP. 1/3 or 1/2 Bias Drive can be selected by external terminal (BIAS) setting. Line / frame inversion can be set by MODESET3 command. Refer to **LCD Driving Waveform**.

## POR and Reset Initialize Condition

BU91R64CH-M3BW has POR (Power On Reset) circuit. Keep Power On / Off specification and sequence described in **Cautions in Power On / Off**. Initial condition after executing Software Reset and POR is as follows.

- Display is off.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Each Command Registers are reset initialize condition. Refer to **Detailed Command Description**.

## Blink Control (Blink Timing Generator)

Blink function is asserted by Blink Control 1 command (BLKCTL1). In All Segments Blink Mode, all dots blink is available. In Bank Blink Mode, individual dot blink is available only in 1/2 Duty and Static Drive mode. Refer to **5. Blink Control1 (BLKCTL1)**. The Displayed RAM mapping is switched at blink frequency as following images.

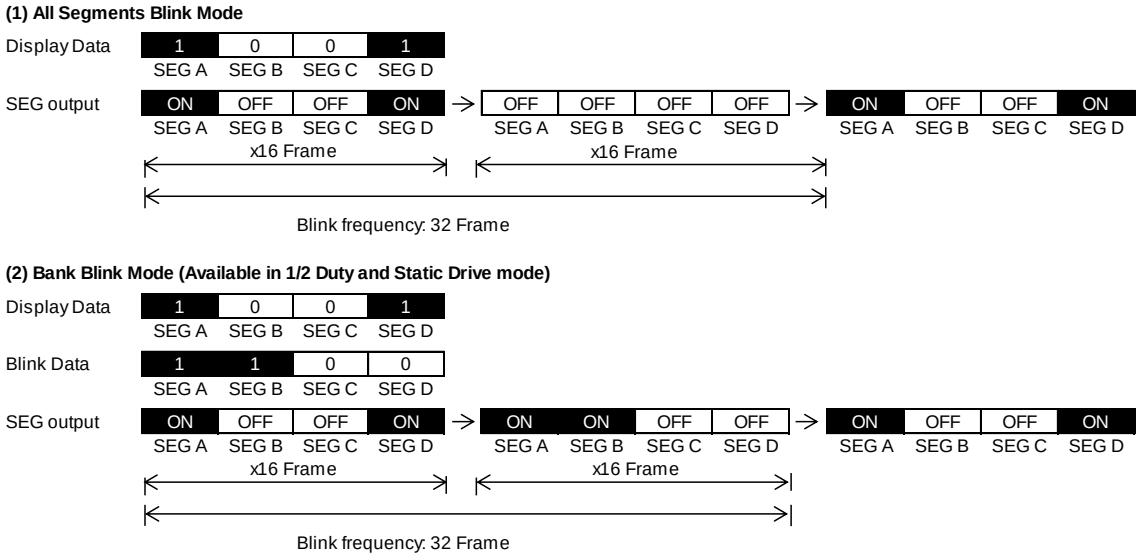



Figure 36. Bank Blink Mode Function (Blink Frequency as 32 Frame Case)

Blink data can be written in Blink Control 2 command (BLKCTL2) P1 = “1”. The command sequence and the relationship between data input and DDRAM Address Map are as follows.

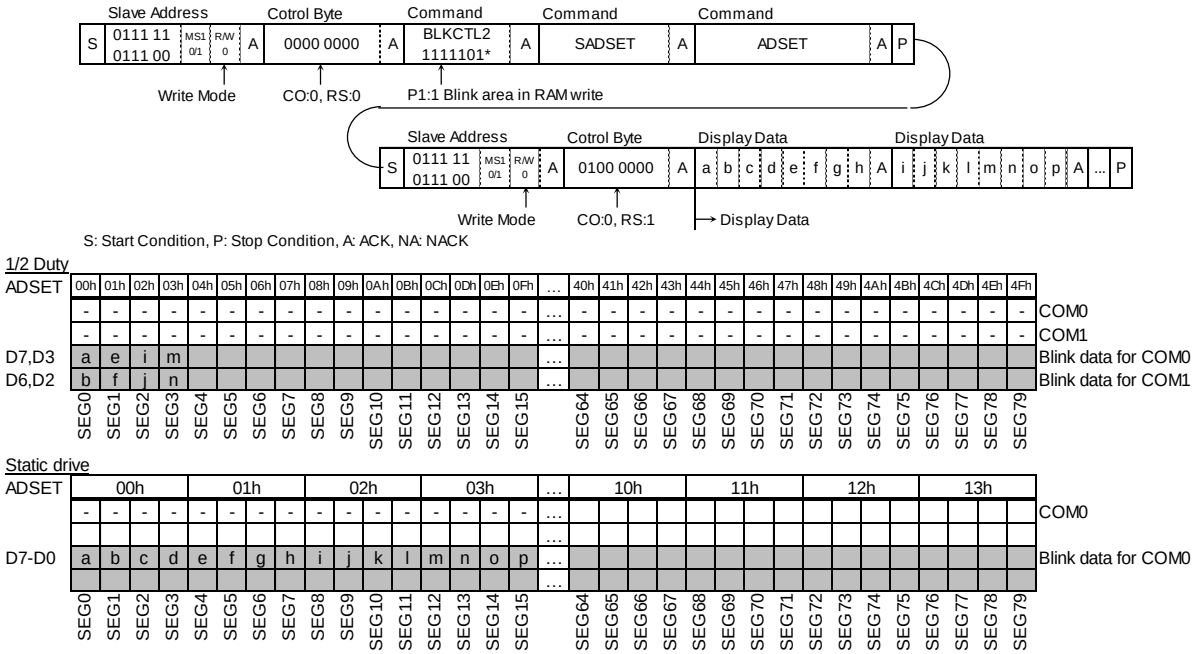



Figure 37. DDRAM Address Map of Blink Area (Bank Blink Mode)


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Error Detection

BU91R64CH-M3BW has the following Error Detection functions. When one of functions in a following table detects abnormal status, ERROUT terminal output high level. Then the item with abnormal status can be identified by reading Command Registers.
MCU can detect all events which cause abnormal display by these functions. MCU can take action ex) Stopping the display or displaying information about abnormal state when LCD module encountered problem.

Table 6. Detection Functions

| Item | Detected Error | Detection Function Availability | Detection Timing |
|---|---|---|---|
| Glass Breaking Detection | LCD Glass Breaking | During DISPON | By DISPON Command |
| Checksum Detection | I/F Communication Error | Always | By CHKSUM Command |
| Logic Error Detection | Logic DFF Malfunction | During DISPON | Always in DISPON |
| SEG / COM Toggle Detection | SEG / COM Output Level Error | During DISPON | Always in DISPON |
| Contact Resistance Check | COG Bonding Status | (No Power Applied) | (In LCD Module Assembly) |

Block diagram and data path of Detection block are shown below.

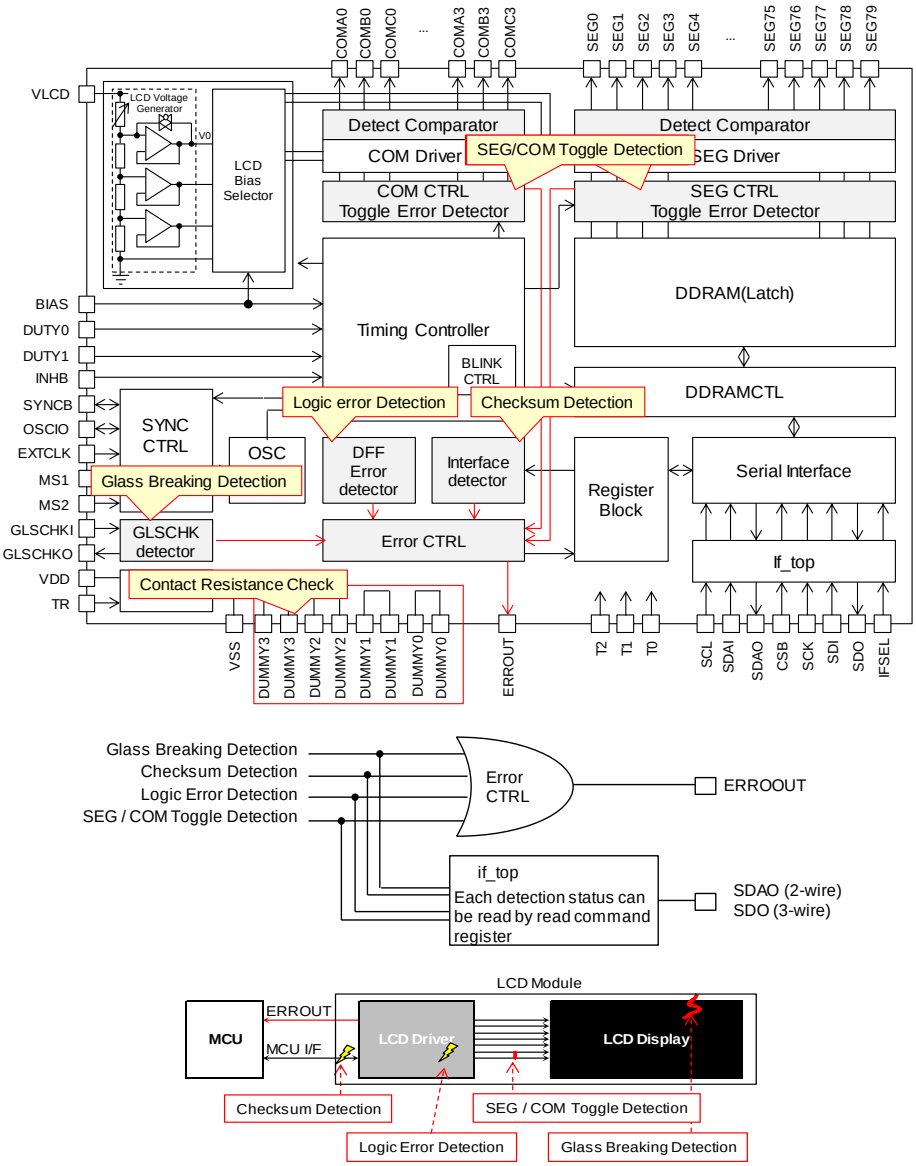



Figure 38. Detection Block and Data Path


© 2016 ROHM Co., Ltd. All rights reserved.

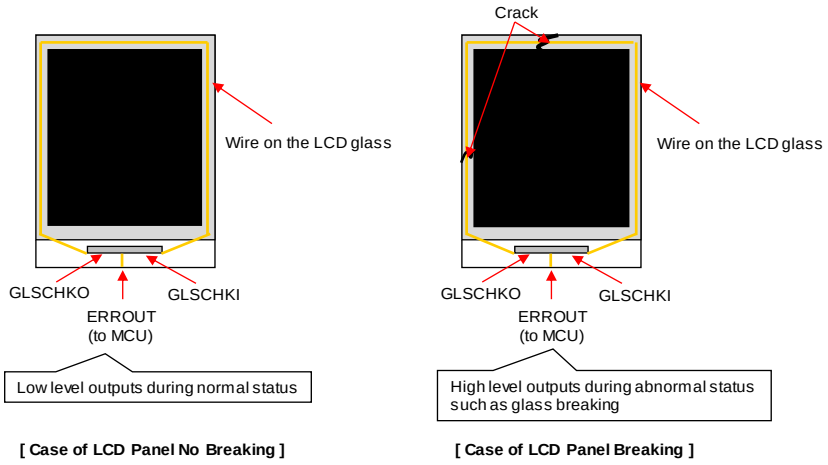
Downloaded from Arrow.com.

## Error Detection - continued

### Glass Breaking Detection

BU91R64CH-M3BW can detect LCD glass breaking status.

In Single-chip Use Case,




In Multi-chip Cascaded Use Case,

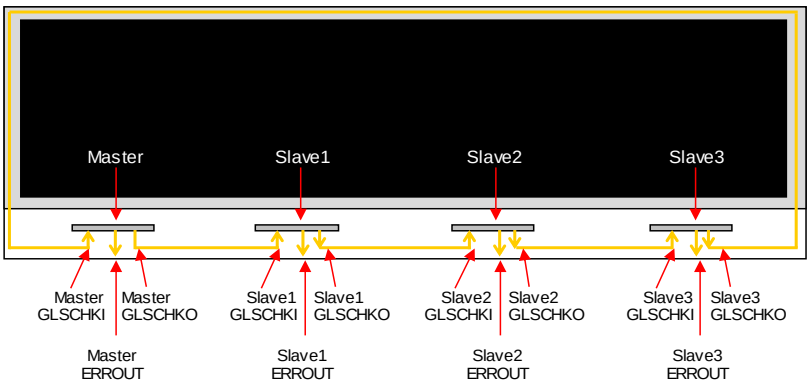



Figure 39. Glass Breaking Detection


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

**Glass Breaking Detection – continued**

Glass breaking detection will be judged after 4 frames from MODESET1 command (DISPON). High level will be judged at the end of the second frame after MODESET1 command (DISPON) and low level will be judged at the end of the fourth frame after the command. See following sequence.

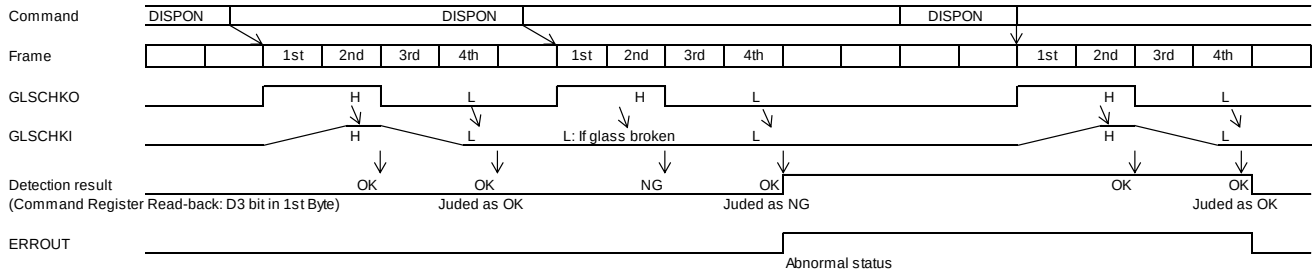



Figure 40. Sequence of Glass Breaking Detection

Thus, the detection period depends on the Frame Frequency setting. It is necessary to consider ITO wiring resistance and capacitance to keep the following calculation:

$$2 \times \tau < 2 \times \text{Frame Duty} \quad [\text{s}] \qquad \text{(A)}$$

where:
$\tau$ is the CR time constant. $\tau = C \times R$. $C$: ITO capacitance, $R$: ITO resistance.

< Calculation example >
When Frame rate = 200Hz, Wire length around LCD glass = 500 counts, ITO sheet count = 60Ω and ITO capacitance = 100pF

$$\text{ITO registance} = 60[\Omega] \times 500 \ [\text{count}] = 30{,}000 \qquad [\Omega]$$

$$2 \times \tau = 2 \times C \times R = 2 \times 100[\text{pF}] \times 30[\text{k}\Omega] = 6 \qquad [\mu\text{s}]$$

$$2 \times \text{Frame Duty} = 2 \times \frac{1}{200} = 10 \qquad [\text{ms}]$$

In this case, (A) is satisfied. So glass check function will work correctly.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Error Detection - continued

### Checksum Detection

This function detects the error due to command or Display Data alteration by electric noise during transfer from MCU. Checksum detection will be judged after every CHKSUM command. See following sequence.

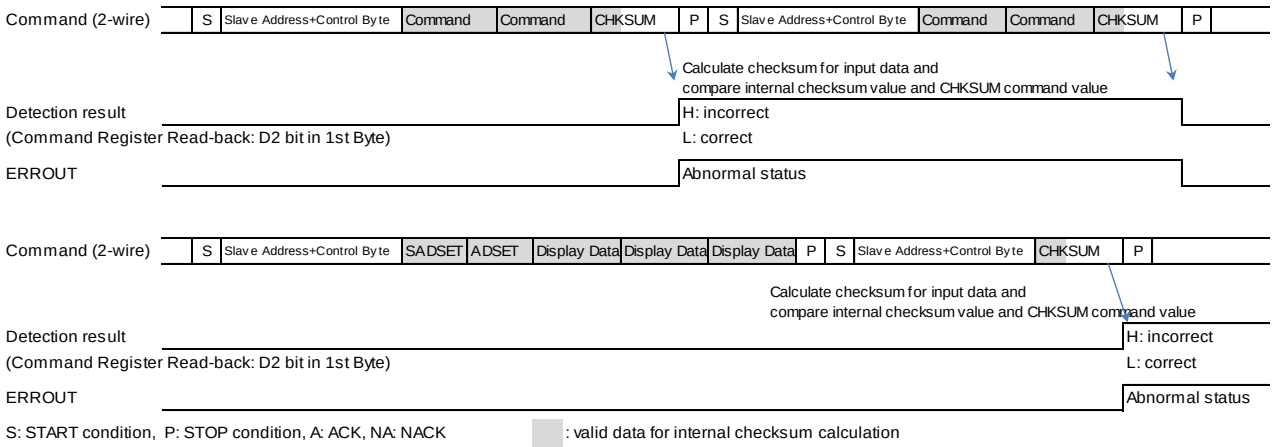
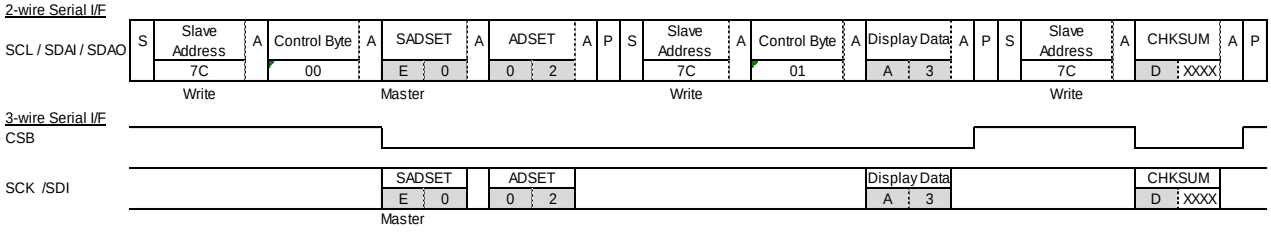


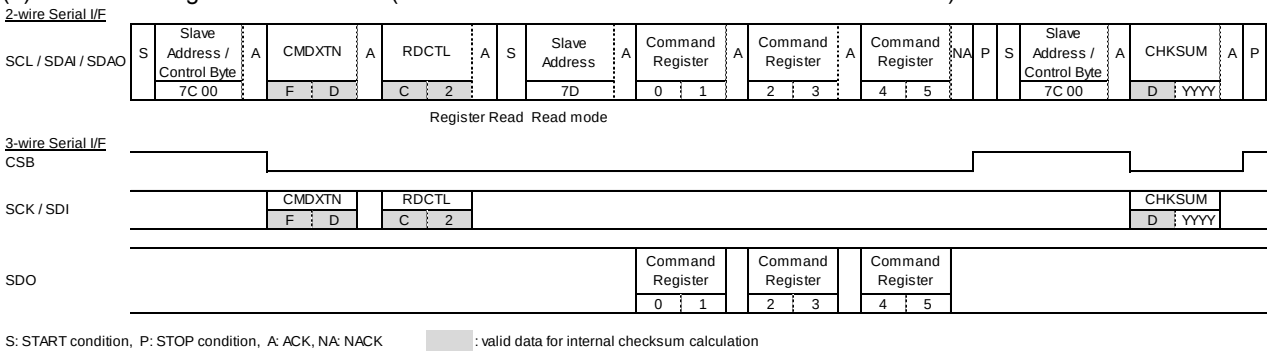

Figure 41. Sequence of Checksum Detection

Checksum calculation example:

(1) Display Data Write Case




(2) Command Registers Read Case (Read values are not used for checksum calculation.)




Calculation (1) RAM Write Case

| | Hex | Dec |
|---|---|---|
| SADSET upper 4-bit | E | 14 |
| SADSET lower 4-bit | 0 | 0 |
| ADSET upper 4-bit | 0 | 0 |
| ADSET lower 4-bit | 2 | 2 |
| Display Data upper 4-bit | A | 10 |
| Display Data lower 4-bit | 3 | 3 |
| CHKSUM upper 4-bit | D | 13 |
| Sum | 2A | 42 |

-> "XXXX" = "Ah"

Calculation (2) Read Case

| | Hex | Dec |
|---|---|---|
| CMDXTN upper 4-bit | F | 15 |
| CMDXTN lower 4-bit | D | 13 |
| RDCTL upper 4-bit | C | 12 |
| RDCTL lower 4-bit | 2 | 2 |
| CHKSUM upper 4-bit | D | 13 |
| Sum | 37 | 55 |

-> "YYYY" = "7h"

Figure 42. Example of Checksum Calculation

In 2-wire, the checksum calculation value will be same in ICs which use same Slave Address and different sub address.
In 3-wire, all IC's checksum values will be same.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Error Detection - continued

### Logic Error Detection

This function detects occurrence of registers (DFF) errors due to electric noise. DFFs for detection are placed around logic area. Judgement is always proceeding in DISPON status. Logic error detection will be judged after every 2 frames from DISPON command. See following sequence.

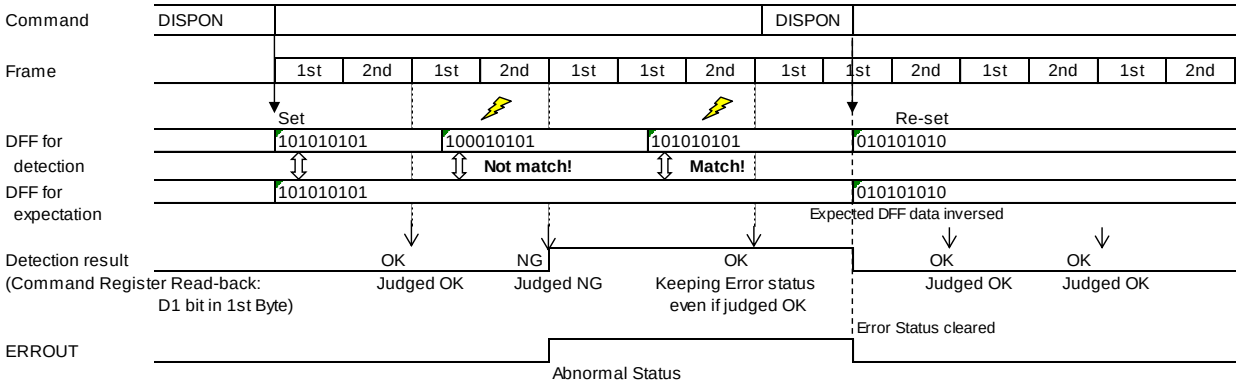



Figure 43. Sequence of Logic Error Detection

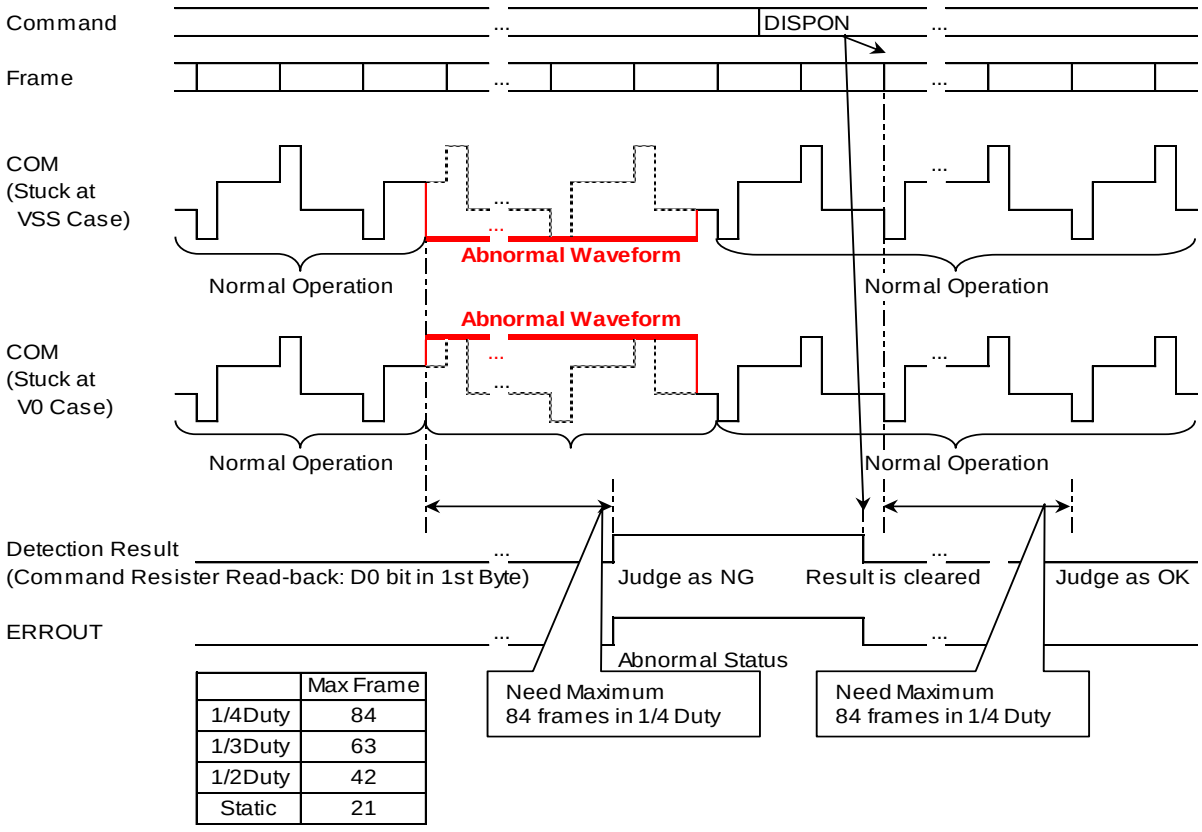

© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Error Detection - continued

### SEG / COM Toggle Detection

This function is to detect whether SEG / COM output toggle (AC inversion) in DDRAM data bit = 1.
Detectable status are considered as following conditions,
(1) SEG / COM waveform stuck at VSS level (SEG can detect in DDRAM data bit = 1 case only).
(a) LCD broken.
(b) ITO wiring connected to VSS line.
(c) SEG / COM output broken such as short with VSS level.
(2) SEG / COM waveform stuck at V0 level (SEG can detect in DDRAM data bit = 1 case only).
(a) LCD broken.
(b) ITO wiring connected to VLCD line.
(c) SEG / COM output broken such as short with VLCD / V0 level.




| | Max Frame |
|---|---|
| 1/4Duty | 84 |
| 1/3Duty | 63 |
| 1/2Duty | 42 |
| Static | 21 |

Figure 44. Sequence of SEG / COM Toggle Detection

### Contact Resistance Check

COG contact resistance can be inspected by measuring resistance in DUMMY0, DUMMY1, DUMMY2 and DUMMY3 terminals. Abnormal COG bonding status can be detected if the values are outliers.

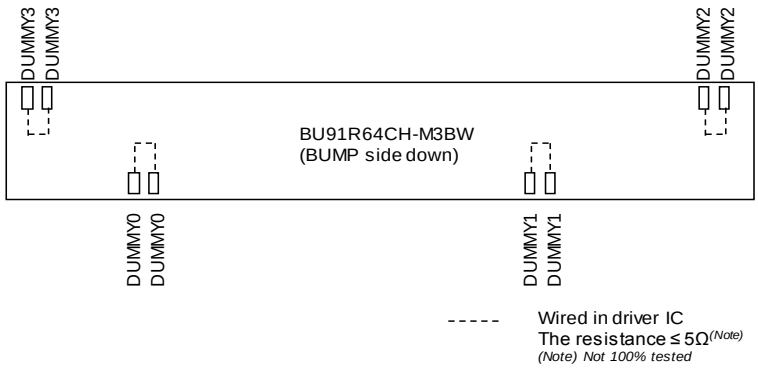



Figure 45. DUMMY PADs for the Contact Resistance Measurement


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Command / Function List

Description List of Command / Function

Table 7. Command / Function List

| No. | Command | Function | Identify Sub Address by SADSET | Available in CMDXTN Mode |
|---|---|---|---|---|
| Normal Command | | | | |
| 1 | Mode Set 1(MODESET1) | Display On / Off | - | No |
| 2 | Address Set (ADSET) | DDRAM Address Setting | - | No |
| 3 | Sub Address Set (SADSET) | IC Selecting | - | No |
| 4 | Frame Rate Set (FRSET) | Frame Frequency | - | No |
| 5 | Blink Control1 (BLKCTL1) | Blink Mode / Blink Frequency Setting | - | No |
| 6 | Blink Control2 (BLKCTL2) | Blink Area Setting | - | No |
| 7 | Command Extension (CMDXTN) | Access enable for extended commands | - | - |
| Extension Command | | | | |
| 8 | Software Reset (SWRST) | Software Reset | - | Yes |
| 9 | Mode Set 2(MODESET2) | Error Detection Control | - | Yes |
| 10 | Mode Set 3(MODESET3) | Line / Frame Inversion, Frame Frequency | - | Yes |
| 11 | Contrast Setting (CNTSET) | Contrast adjustment | Yes | Yes |
| 12 | Read Control (RDCTL) | Read Control | - | Yes |
| 13 | Checksum(CHKSUM) | Checksum Trigger and Expected Value | - | Yes |
| 14 | COM Set (COMSET) | COM driving order select, Contrast adjustment | Yes | Yes |

## Detailed Command Description

### 1. Mode Set 1 (MODESET1)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 0 | 0 | P3 | * | * | * |

(*: don’t care)

Set Display On and Off

| P3 | Setup | Reset Initialize Condition |
|---|---|---|
| 0 | Display Off (DISPOFF) | ○ |
| 1 | Display On (DISPON) | - |

Display Off: Regardless of DDRAM data, all Segment and Common output will be stopped (VSS level).
Display On: Segment and Common output will be active and will start to read the Display Data from DDRAM.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 2. Address Set (ADSET)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Set address. (P6 to P0 = “0000000” in reset initialize condition)
Don’t set out of range address, otherwise address will be set to “0000000”.
In 3-SPI case, next transferred data will be recognized as Display Data.

The range of address (7-bit) is shown as bellow.
1/4, 1/3 and 1/2 Duty Drive mode: 00h to 4Fh
Static Drive Mode: 00h to 13h

### 3. Sub Address Set (SADSET)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 0 | 0 | 0 | P1 | P0 |

Set sub address to define one of BU91R6xCH sub address.
The following command can be set independently after SADSET command.
- Display Data write
- Display Data read
- Command Registers read
- Contrast Setting (CNTSET)
- COM set (COMSET)

In 2-wire Serial Interface mode

| P1 | P0 | Available IC | Reset Initialize Condition |
|---|---|---|---|
| 0 | * | Master or Slave1 *(Note 1)*(MS2 = VSS) | ○ |
| 1 | * | Slave2 or Slave3 *(Note 1)*(MS2 = VDD) | - |

*(Note 1)*: Bit1 of Slave Address selects one of “Master / Slave1” or one of “Slave2 / Slave3”.
(*: don’t care)

In 3-wire Serial Interface mode

| P1 | P0 | Available IC | Reset Initialize Condition |
|---|---|---|---|
| 0 | 0 | Master (MS2 = VSS, MS1 = VSS) | ○ |
| 0 | 1 | Slave1 (MS2 = VSS, MS1 = VDD) | - |
| 1 | 0 | Slave2 (MS2 = VDD, MS1 = VSS) | - |
| 1 | 1 | Slave3 (MS2 = VDD, MS1 = VDD) | - |


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 4. Frame Rate Set (FRSET)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 0 | 1 | P2 | P1 | P0 |

Set Frame Frequency
In Internal Clock Mode, Frame Frequency is calculated as shown in the following table.

Table 8. Frame Frequency (Internal Clock Mode)

| MODESET3 | | FRSET | | | Frame Fregency [Hz] (Number of Clock Pulses) | | Reset Initilaze Condition |
|---|---|---|---|---|---|---|---|
| P1 | P0 | P2 | P1 | P0 | Line Inversion | Frame Inversion | |
| 0 | 0 | 0 | 0 | 0 | 65.7 (624) | | - |
| 0 | 0 | 0 | 0 | 1 | 74.3 (552) | | - |
| 0 | 0 | 0 | 1 | 0 | 85.4 (480) | | - |
| 0 | 0 | 0 | 1 | 1 | 122.0 (336) | | - |
| 0 | 0 | 1 | 0 | 0 | 131.4 (312) | | - |
| 0 | 0 | 1 | 0 | 1 | 142.4 (288) | | - |
| 0 | 0 | 1 | 1 | 0 | 155.3 (264) | | o |
| 0 | 0 | 1 | 1 | 1 | 170.8 (240) | | - |
| 0 | 1 | 0 | 0 | 0 | 189.8 (216) | | - |
| 0 | 1 | 0 | 0 | 1 | 213.5 (192) | | - |
| 0 | 1 | 0 | 1 | 0 | 244.0 (168) | | - |
| 0 | 1 | 0 | 1 | 1 | 284.7 (144) | | - |
| 0 | 1 | 1 | 0 | 0 | 427.1 ( 96) | | - |
| 0 | 1 | 1 | 0 | 1 | 569.4 ( 72) (Prohibited) | | - |
| 0 | 1 | 1 | 1 | 0 | 854.2 ( 48) (Prohibited) | | - |
| 0 | 1 | 1 | 1 | 1 | 1708.3 ( 24) (Prohibited) | | - |
| 1 | 0 | 0 | 0 | 0 | 65.7 (624) | 131.4 (312) | - |
| 1 | 0 | 0 | 0 | 1 | 74.3 (552) | 148.6 (276) | - |
| 1 | 0 | 0 | 1 | 0 | 85.4 (480) | 170.8 (240) | - |
| 1 | 0 | 0 | 1 | 1 | 122.0 (336) | 244.0 (168) | - |
| 1 | 0 | 1 | 0 | 0 | 131.4 (312) | 262.8 (156) | - |
| 1 | 0 | 1 | 0 | 1 | 142.4 (288) | 284.7 (144) | - |
| 1 | 0 | 1 | 1 | 0 | 155.3 (264) | 310.6 (132) | - |
| 1 | 0 | 1 | 1 | 1 | 170.8 (240) | 341.7 (120) | - |
| 1 | 1 | 0 | 0 | 0 | 189.8 (216) | 379.6 (108) | - |
| 1 | 1 | 0 | 0 | 1 | 213.5 (192) | 427.1 ( 96) | - |
| 1 | 1 | 0 | 1 | 0 | 244.0 (168) | 488.1 ( 84) | - |
| 1 | 1 | 0 | 1 | 1 | 284.7 (144) | 569.4 ( 72) (Prohibited) | - |
| 1 | 1 | 1 | 0 | 0 | 427.1 ( 96) | 854.2 ( 48) (Prohibited) | - |
| 1 | 1 | 1 | 0 | 1 | 569.4 ( 72) (Prohibited) | 1138.9 ( 36) (Prohibited) | - |
| 1 | 1 | 1 | 1 | 0 | 854.2 ( 48) (Prohibited) | 1708.3 ( 24) (Prohibited) | - |
| 1 | 1 | 1 | 1 | 1 | 1708.3 ( 24) (Prohibited) | 3416.7 ( 12) (Prohibited) | - |

In External Clock Mode, Frame Frequency is calculated as shown in following table,

Table 9. Frame Frequency (External Clock Mode)

| MODESET3 | | FRSET | | | Frame Fregency [Hz] | | Reset Initilaze Condition |
|---|---|---|---|---|---|---|---|
| P1 | P0 | P2 | P1 | P0 | Line Inversion | Frame Inversion | |
| 0 | * | * | * | * | External Clock / 24 | | o |
| 1 | * | * | * | * | External Clock / 24 | External Clock / 12 | - |

(*: don't care)

(Example 1)
EXTCLK = VDD
External Clock: 1800Hz
MODESET3 P1: 0
Frame Frequency = External Clock / 24 = 1800 / 24 = 75Hz @Line / Frame Inversion

(Example 2)
EXTCLK = VDD
External Clock: 3500Hz
MODESET3 P1: 1
Frame Frequency = External Clock / 24 = 3500 / 24 = 145.8Hz @Line Inversion
Frame Frequency = External Clock / 12 = 3500 / 12 = 291.7Hz @Frame Inversion


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 5. Blink Control1 (BLKCTL1)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 0 | P2 | P1 | P0 |

Set Blink Mode

| P2 | Blink Mode | Reset Initialize Condition |
|---|---|---|
| 0 | All Segments Blink Mode | ○ |
| 1 | Bank Blink Mode | - |

Bank Blink Mode is available in 1/2 Duty Drive and Static Drive.

Set Blink Frequency

| P1 | P0 | Blink Frequency | Reset Initialize Condition |
|---|---|---|---|
| 0 | 0 | Off | ○ |
| 0 | 1 | 32 Frames | - |
| 1 | 0 | 64 Frames | - |
| 1 | 1 | 128 Frames | - |

About Frame Frequency calculation, refer to **4. Frame Rate Set (FRSET)**.
About Bank Blink Mode, refer to **Blink Control (Blink Timing Generator)**.

### 6. Blink Control2 (BLKCTL2)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 1 | 0 | P1 | * |

(*: don't care)

Set Blink Area in 1/2 Duty Drive and Static Drive in Bank Blink Mode

| P1 | DDRAM Write Area | Reset Initialize Condition |
|---|---|---|
| 0 | Normal Display Area | ○ |
| 1 | Blink Area | - |

This register is available only in 1/2 Duty Drive and Static Drive.
About data writing to blink area, refer to **Blink Control (Blink Timing Generator)**.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 7. Command Extension (CMDXTN)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | P0 |

Set CMDXTN Mode Effective

| P0 | Mode | Reset Initialize Condition |
|---|---|---|
| 0 | Ineffective CMDXTN Mode (Normal Mode) | ○ |
| 1 | CMDXTN Mode (Extension Mode) | - |

The following extension commands are accessible only in CMDXTN mode,

1. SWRST
2. MODESET2
3. MODESET3
4. CNTSET
5. RDCTL
6. CHKSUM
7. COMSET

To access normal command such as DISPON etc., set P0 = “0” (ineffective CMDXTN mode).
Refer to **Command / Function List**.

### 8. Software Reset (SWRST)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | * | * | * | P0 |

(*: don’t care)

This register can be accessed in CMDXTN mode only.

Set software reset effective

| P0 | Operation | Reset Initialize Condition |
|---|---|---|
| 0 | No Operation | ○ |
| 1 | Software Reset Execute | - |

When “Software Reset” is executed, BU91R64CH-M3BW will be reset to initial condition.
Refer to **POR and Reset Initialize Condition**.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 9. Mode Set 2 (MODESET2)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 1 | P3 | P2 | P1 | P0 |

This register can be accessed in CMDXTN mode only.

Set Glass breaking detection to enable

| P3 | Setup | Reset Initialize Condition |
|---|---|---|
| 0 | Disable | ○ |
| 1 | Enable | - |

Set Checksum detection to enable

| P2 | Setup | Reset Initialize Condition |
|---|---|---|
| 0 | Disable | ○ |
| 1 | Enable | - |

Set Logic error detection to enable

| P1 | Setup | Reset Initialize Condition |
|---|---|---|
| 0 | Disable | ○ |
| 1 | Enable | - |

Set SEG / COM toggle detection to enable

| P0 | Setup | Reset Initialize Condition |
|---|---|---|
| 0 | Disable | ○ |
| 1 | Enable | - |

ERROUT output function will be effective when any bit of P3 to P0 is set to enable, refer to **Detailed Command Description**.

### 10. Mode Set 3 (MODESET3)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 1 | 0 | 0 | P2 | P1 | P0 |

This register can be accessed in CMDXTN mode only.

Set LCD Driving Mode

| P2 | Driving Mode | Reset Initialize Condition |
|---|---|---|
| 0 | Line Inversion Mode | ○ |
| 1 | Frame Inversion Mode | - |

Power consumption is reduced in the following order: Line inversion > Frame inversion
Typically, when driving large capacitance LCD, Line inversion will increase the influence of crosstalk.
Regarding driving waveform, refer to **LCD Driving Waveform**.

Set x2 Frame frequency in Frame inversion mode

| P1 | Mode | Reset Initialize Condition |
|---|---|---|
| 0 | Normal Frequency Mode | ○ |
| 1 | x2 Frequency in Frame Inversion | - |

This command is only effective in Frame inversion mode.
In detail, refer to **4. Frame Rate Set (FRSET)**.

Set Frame Frequency Mode

| P0 | Frame Frequency Mode | Reset Initialize Condition |
|---|---|---|
| 0 | Normal Frequency Mode | ○ |
| 1 | High Frequency Mode | - |

In detail, refer to **4. Frame Rate Set (FRSET)**.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 11. Contrast Setting (CNTSET)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 1 | 1 | P3 | P2 | P1 | P0 |

This register can be accessed in CMDXTN mode only.
This command can set sub address individually by SADSET command.

Set EVR for Contrast adjustment.
BU91R64CH-M3BW is able to control V0 voltage level (the maximum level voltage of LCD driving) by a 32-step electrical volume register (EVR).

Table 10. V0 Voltage Setting

Unit: V

| COMSET | CNTSET | | | | Formula | VLCD [V] | | | | | | | Reset Initialize Condition |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| P3 | P3 | P2 | P1 | P0 | | 6.0 | 5.5 | 5.0 | 4.0 | 3.5 | 3.0 | 2.5 | |
| 0 | 0 | 0 | 0 | 0 | 1.000 * VLCD | 6.000 | 5.500 | 5.000 | 4.000 | 3.500 | 3.000 | 2.500 | O |
| 0 | 0 | 0 | 0 | 1 | 0.967 * VLCD | 5.802 | 5.323 | 4.839 | 3.871 | 3.387 | 2.903 | 2.419 | - |
| 0 | 0 | 0 | 1 | 0 | 0.937 * VLCD | 5.622 | 5.156 | 4.688 | 3.750 | 3.281 | 2.813 | 2.344 | - |
| 0 | 0 | 0 | 1 | 1 | 0.909 * VLCD | 5.454 | 5.000 | 4.545 | 3.636 | 3.182 | 2.727 | 2.273 | - |
| 0 | 0 | 1 | 0 | 0 | 0.882 * VLCD | 5.292 | 4.853 | 4.412 | 3.529 | 3.088 | 2.647 | 2.206 | - |
| 0 | 0 | 1 | 0 | 1 | 0.857 * VLCD | 5.142 | 4.714 | 4.286 | 3.429 | 3.000 | 2.571 | 2.143 | - |
| 0 | 0 | 1 | 1 | 0 | 0.833 * VLCD | 4.998 | 4.583 | 4.167 | 3.333 | 2.917 | 2.500 | 2.083 | - |
| 0 | 0 | 1 | 1 | 1 | 0.810 * VLCD | 4.860 | 4.459 | 4.054 | 3.243 | 2.838 | 2.432 | 2.027 | - |
| 0 | 1 | 0 | 0 | 0 | 0.789 * VLCD | 4.734 | 4.342 | 3.947 | 3.158 | 2.763 | 2.368 | 1.974 | - |
| 0 | 1 | 0 | 0 | 1 | 0.769 * VLCD | 4.614 | 4.231 | 3.846 | 3.077 | 2.692 | 2.308 | 1.923 | - |
| 0 | 1 | 0 | 1 | 0 | 0.750 * VLCD | 4.500 | 4.125 | 3.750 | 3.000 | 2.625 | 2.250 | 1.875 | - |
| 0 | 1 | 0 | 1 | 1 | 0.731 * VLCD | 4.386 | 4.024 | 3.659 | 2.927 | 2.561 | 2.195 | 1.829 | - |
| 0 | 1 | 1 | 0 | 0 | 0.714 * VLCD | 4.284 | 3.929 | 3.571 | 2.857 | 2.500 | 2.143 | 1.786 | - |
| 0 | 1 | 1 | 0 | 1 | 0.697 * VLCD | 4.182 | 3.837 | 3.488 | 2.791 | 2.442 | 2.093 | 1.744 | - |
| 0 | 1 | 1 | 1 | 0 | 0.681 * VLCD | 4.086 | 3.750 | 3.409 | 2.727 | 2.386 | 2.045 | 1.705 | - |
| 0 | 1 | 1 | 1 | 1 | 0.666 * VLCD | 3.996 | 3.667 | 3.333 | 2.667 | 2.333 | 2.000 | 1.667 | - |
| 1 | 0 | 0 | 0 | 0 | 0.652 * VLCD | 3.912 | 3.587 | 3.261 | 2.609 | 2.283 | 1.957 | 1.630 | - |
| 1 | 0 | 0 | 0 | 1 | 0.638 * VLCD | 3.828 | 3.511 | 3.191 | 2.553 | 2.234 | 1.915 | 1.596 | - |
| 1 | 0 | 0 | 1 | 0 | 0.625 * VLCD | 3.750 | 3.438 | 3.125 | 2.500 | 2.188 | 1.875 | 1.563 | - |
| 1 | 0 | 0 | 1 | 1 | 0.612 * VLCD | 3.672 | 3.367 | 3.061 | 2.449 | 2.143 | 1.837 | 1.531 | - |
| 1 | 0 | 1 | 0 | 0 | 0.600 * VLCD | 3.600 | 3.300 | 3.000 | 2.400 | 2.100 | 1.800 | 1.500 | - |
| 1 | 0 | 1 | 0 | 1 | 0.588 * VLCD | 3.528 | 3.235 | 2.941 | 2.353 | 2.059 | 1.765 | 1.471 | - |
| 1 | 0 | 1 | 1 | 0 | 0.576 * VLCD | 3.456 | 3.173 | 2.885 | 2.308 | 2.019 | 1.731 | 1.442 | - |
| 1 | 0 | 1 | 1 | 1 | 0.566 * VLCD | 3.396 | 3.113 | 2.830 | 2.264 | 1.981 | 1.698 | 1.415 | - |
| 1 | 1 | 0 | 0 | 0 | 0.555 * VLCD | 3.330 | 3.056 | 2.778 | 2.222 | 1.944 | 1.667 | 1.389 | - |
| 1 | 1 | 0 | 0 | 1 | 0.545 * VLCD | 3.270 | 3.000 | 2.727 | 2.182 | 1.909 | 1.636 | 1.364 | - |
| 1 | 1 | 0 | 1 | 0 | 0.535 * VLCD | 3.210 | 2.946 | 2.679 | 2.143 | 1.875 | 1.607 | 1.339 | - |
| 1 | 1 | 0 | 1 | 1 | 0.526 * VLCD | 3.156 | 2.895 | 2.632 | 2.105 | 1.842 | 1.579 | 1.316 | - |
| 1 | 1 | 1 | 0 | 0 | 0.517 * VLCD | 3.102 | 2.845 | 2.586 | 2.069 | 1.810 | 1.552 | 1.293 | - |
| 1 | 1 | 1 | 0 | 1 | 0.508 * VLCD | 3.048 | 2.797 | 2.542 | 2.034 | 1.780 | 1.525 | 1.271 | - |
| 1 | 1 | 1 | 1 | 0 | 0.500 * VLCD | 3.000 | 2.750 | 2.500 | 2.000 | 1.750 | 1.500 | 1.250 | - |
| 1 | 1 | 1 | 1 | 1 | 0.491 * VLCD | 2.946 | 2.705 | 2.459 | 1.967 | 1.721 | 1.475 | 1.230 | - |

Prohibited Setting

Avoid setting EVR of “V0 < 2.5V” and “V0 > VLCD – 0.6V” condition. BU91R64CH-M3BW output voltage will be unstable in such conditions.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 12. Read Control (RDCTL)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 0 | 0 | * | * | P1 | P0 |

(*: don't care)

This register can be accessed in CMDXTN mode only.

Set Read enable (This bit is available in 3SPI mode only. In 2-wire, this bit is undefined.)

| P1 | Read_en | Reset Initialize Condition |
|---|---|---|
| 0 | Read disable (Write Mode) | ○ |
| 1 | Read enable (Read Mode) | - |

Set Read data

| P0 | Read_mode | Reset Initialize Condition |
|---|---|---|
| 0 | Command Registers Read | ○ |
| 1 | DDRAM Data Read | - |

### 13. Checksum (CHKSUM)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 0 | 1 | P3 | P2 | P1 | P0 |

This register can be accessed in CMDXTN mode only.

P3 to P0: The sum of all Command Registers value for interface checksum function. Set this value after calculating the sum of each Command Registers value. In detail, refer to **Checksum Detection**.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Detailed Command Description – continued

### 14. COM Set (COMSET)

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 1 | 1 | 0 | P3 | P2 | P1 | P0 |

This register can be accessed in CMDXTN mode only.
This command can set sub address individually by SADSET command.

P3: Set MSB of CNTSET
Refer to Contrast Setting command (CNTSET).

P2 to P0: Set COM scanning order of COMA, COMB and COMC individually.
P2: Set COMC Scanning Order
P1: Set COMB Scanning Order
P0: Set COMA Scanning Order

| P2 (COMC) | P1 (COMB) | P0 (COMA) | Duty Drive | Toggle Order of COM*0 to COM*3 | Reset Initialize Condition |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1/4 Duty | COM*0→COM*1→COM*2→COM*3 | ○ |
| | | | 1/3 Duty | COM*0→COM*1→COM*2 (*Note 1*) | |
| | | | 1/2 Duty | COM*0→COM*1 (*Note 2*) | |
| | | | Static | COM*0 (*Note 3*) | |
| 1 | 1 | 1 | 1/4 Duty | COM*3→COM*2→COM*1→COM*0 | - |
| | | | 1/3 Duty | COM*3→COM*2→COM*1 (*Note 1*) | |
| | | | 1/2 Duty | COM*1→COM*0 (*Note 2*) | |
| | | | Static | COM*0 (*Note 3*) | |

(*: A for P0, or B for P1, or C for P3)
(*Note 1*) COMA3 = COMA0
(*Note 2*) COMA2 = COMA0, COMA3 = COMA1
(*Note 3*) COMA1 / 2 / 3 = COMA0

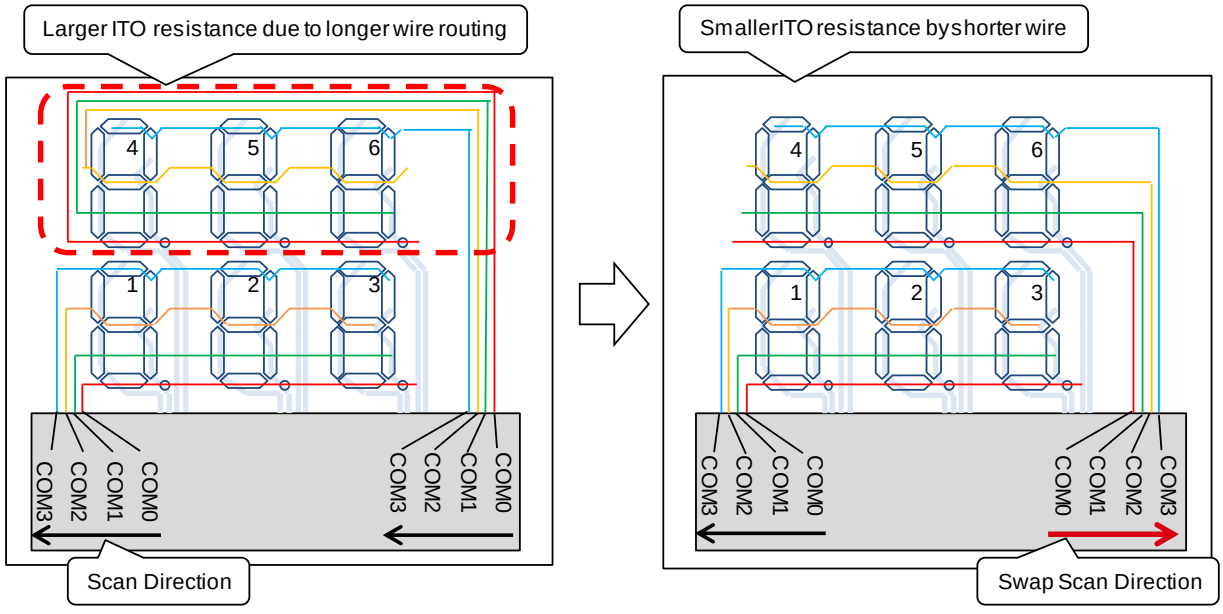


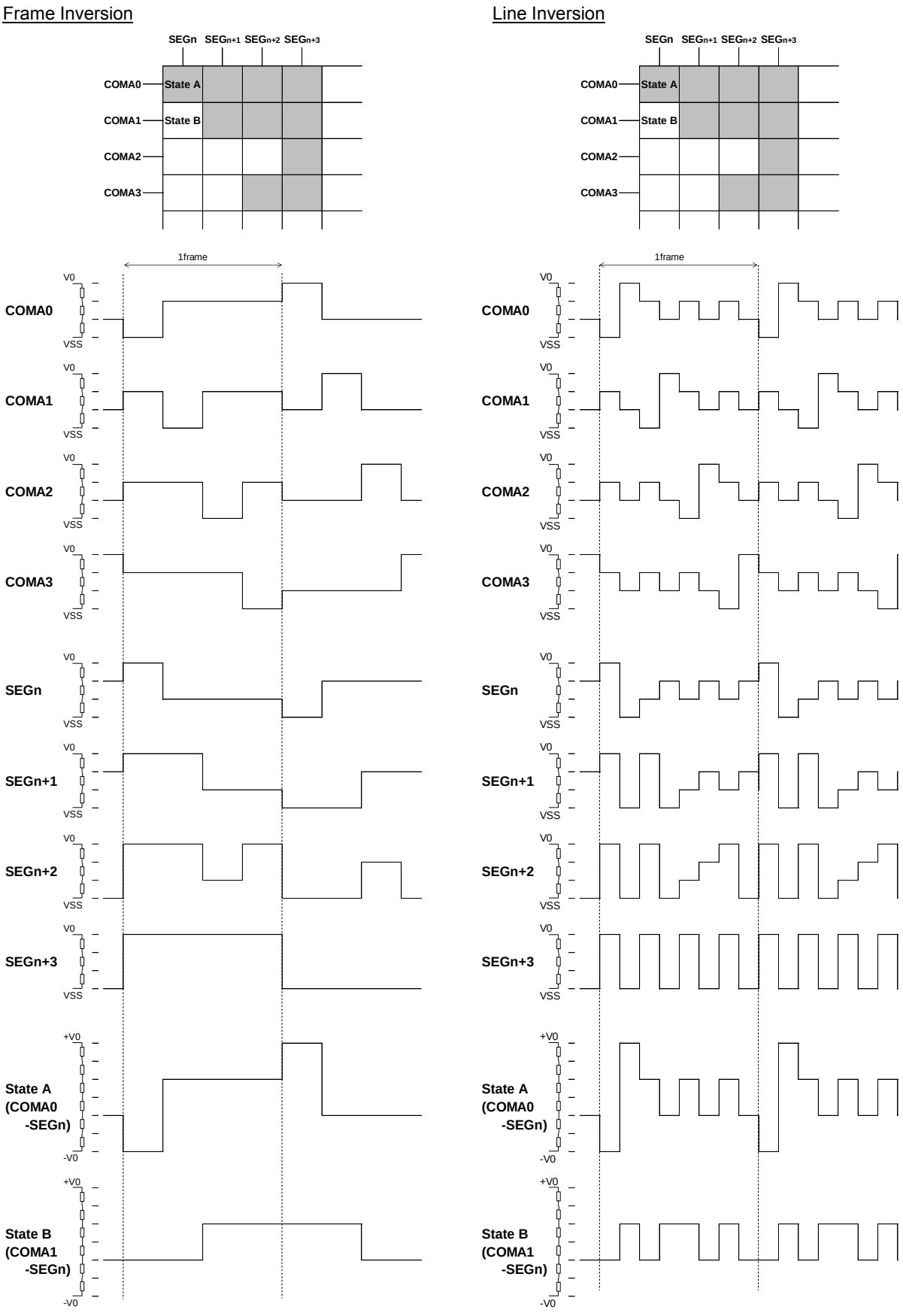

Figure 46. COM Scan Direction Image


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## LCD Driving Waveform

### 1/3 Bias, 1/4 Duty Drive




COMSET P2 = “0”, Normally white type LCD case

Figure 47. LCD Waveform (1/3 Bias, 1/4 Duty Drive)

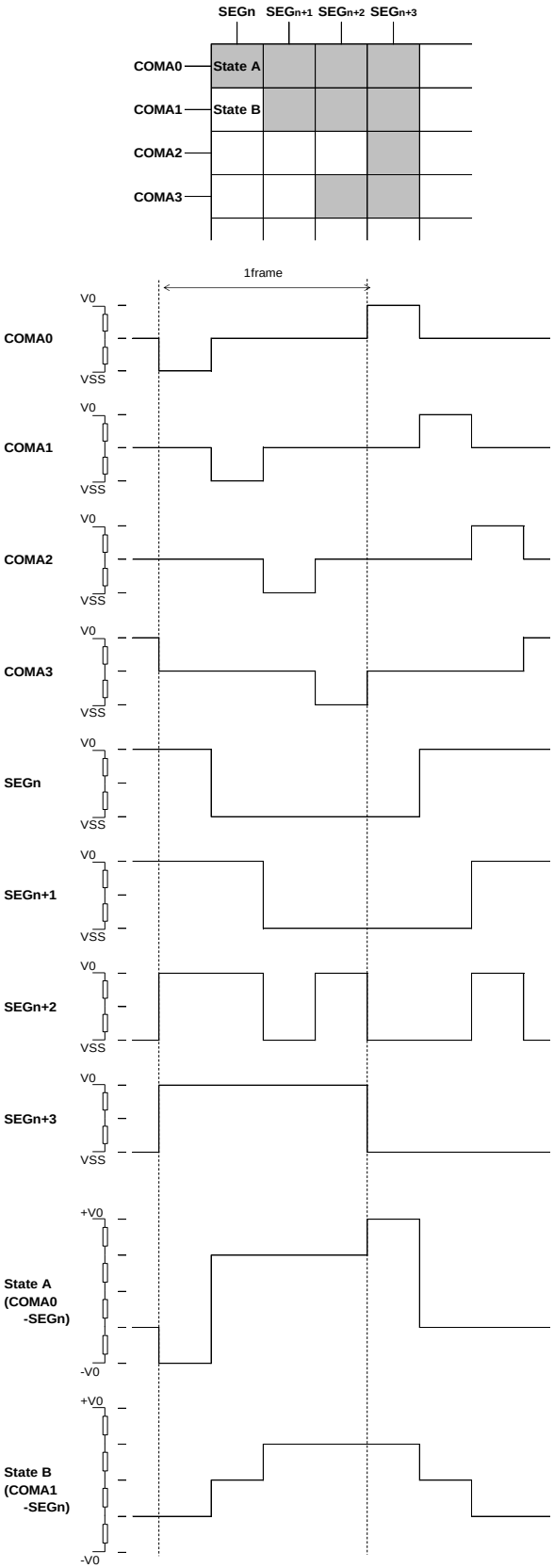

© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

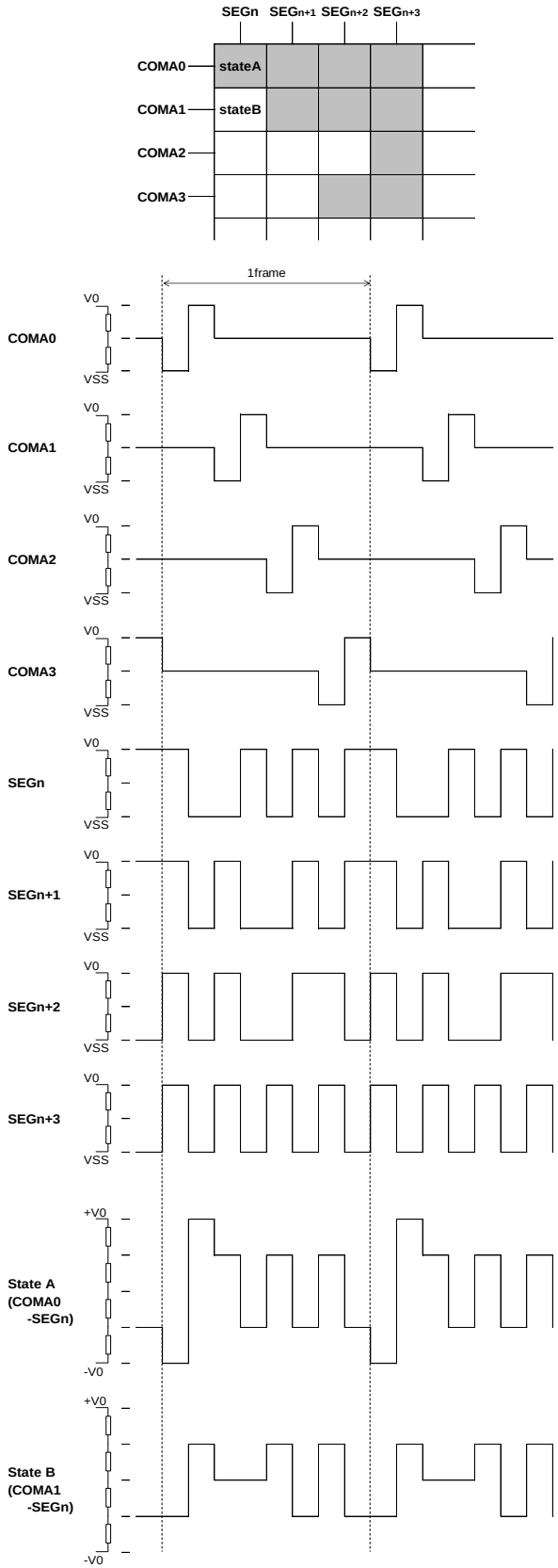
## LCD Driving Waveform - continued

### 1/2 Bias, 1/4 Duty Drive

Frame Inversion




Line Inversion




COMSET P2 = “0”, Normally white type LCD case

Figure 48. LCD Waveform (1/2 Bias, 1/4 Duty Drive)

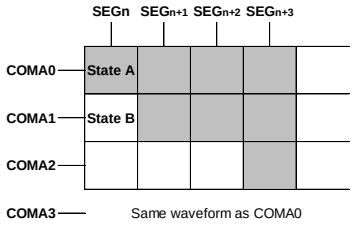

© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

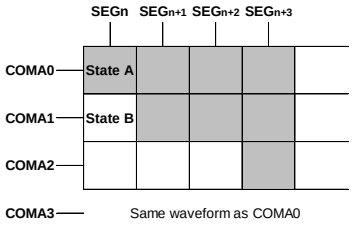
## LCD Driving Waveform - continued

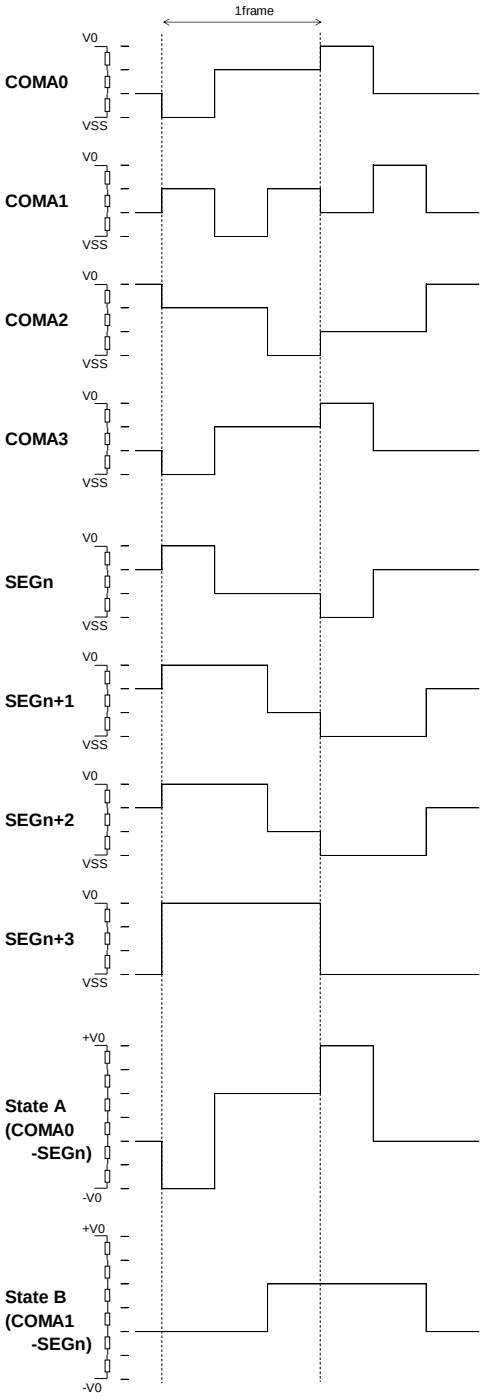
### 1/3 Bias, 1/3 Duty Drive

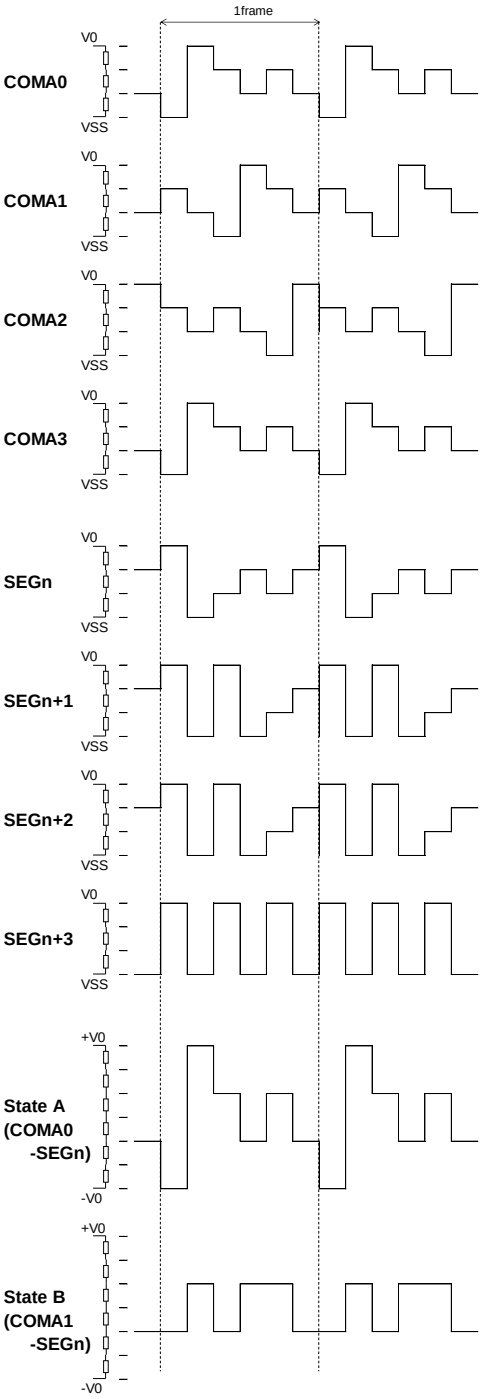
Frame Inversion




Line Inversion




COMSET P2 = “0”, Normally white type LCD case

Figure 49. LCD Waveform (1/3 Bias, 1/3 Duty Drive)

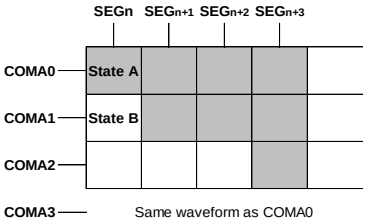

© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

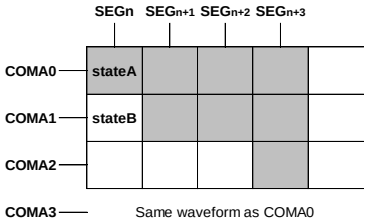
## LCD Driving Waveform - continued

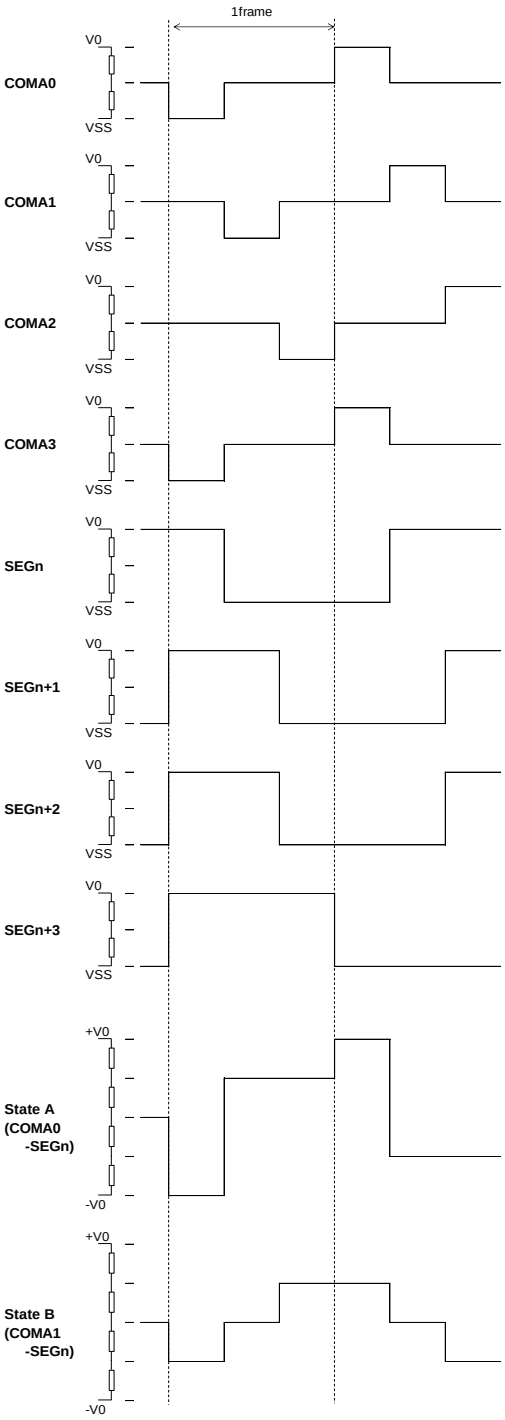
### 1/2 Bias, 1/3 Duty Drive

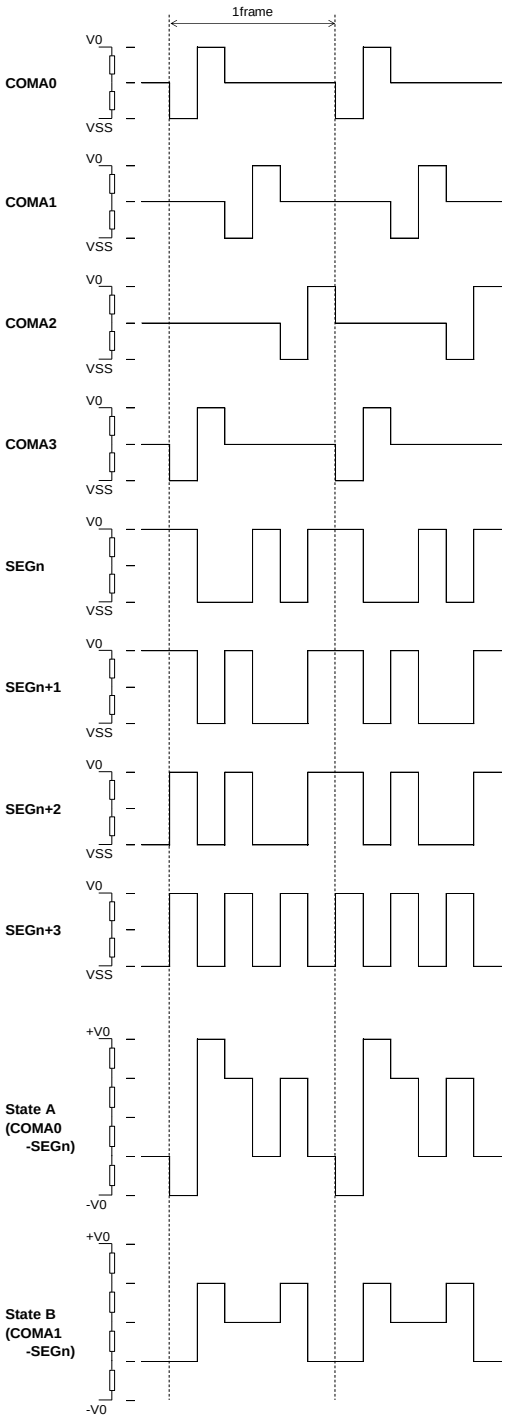
Frame Inversion




Line Inversion




COMSET P2 = “0”, Normally white type LCD case

Figure 50. LCD Waveform (1/2 Bias, 1/3 Duty Drive)

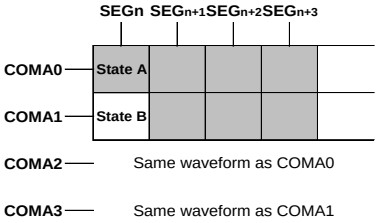

© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

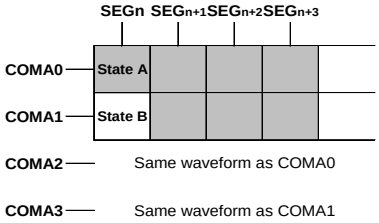
## LCD Driving Waveform - continued

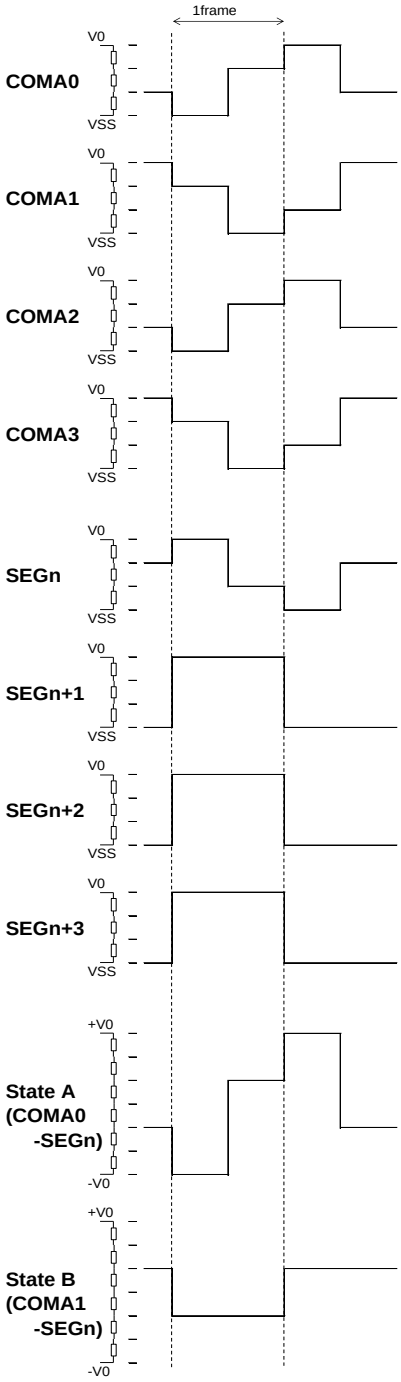
### 1/3 Bias, 1/2 Duty Drive

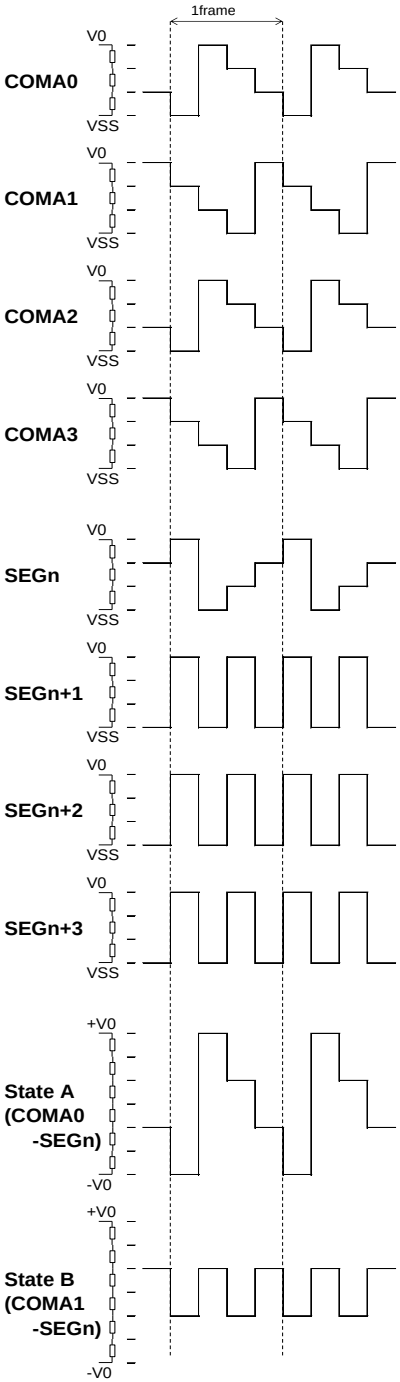
Frame Inversion




Line Inversion




COMSET P2 = “0”, Normally white type LCD case

Figure 51. LCD Waveform (1/3 Bias, 1/2 Duty Drive)

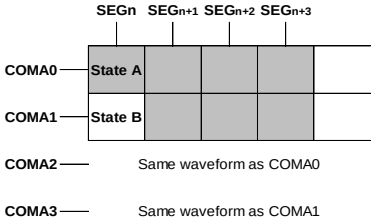

© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

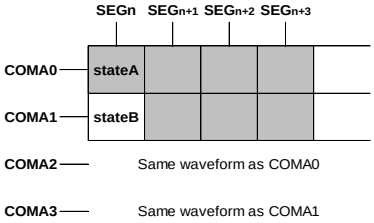
## LCD Driving Waveform - continued

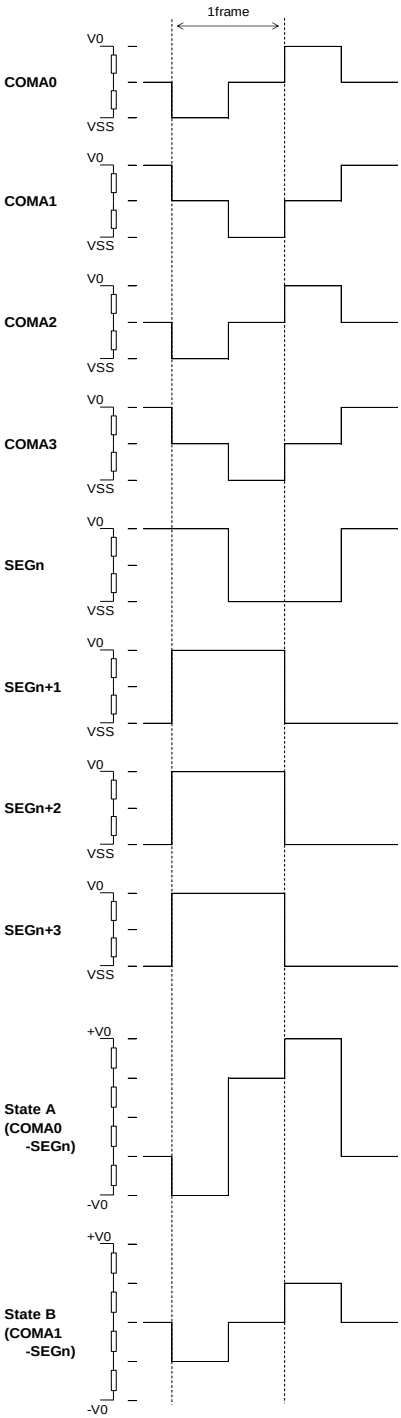
### 1/2 Bias, 1/2 Duty Drive

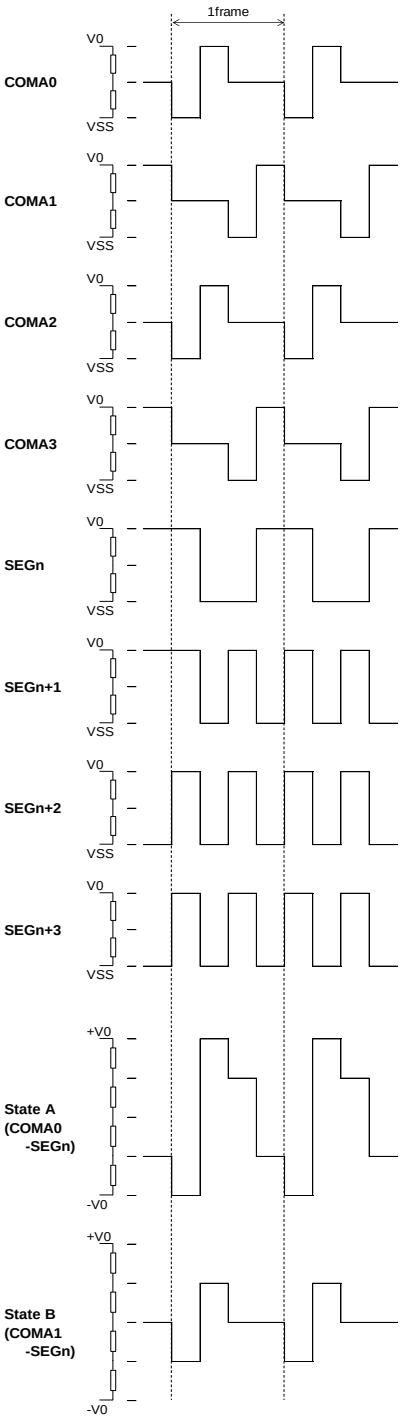
Frame Inversion




Line Inversion




COMSET P2 = “0”, Normally white type LCD case

Figure 52. LCD Waveform (1/2 Bias, 1/2 Duty Drive)

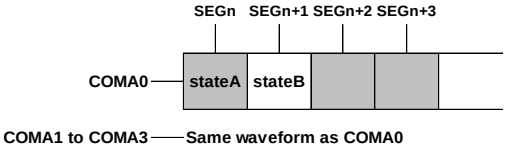

© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

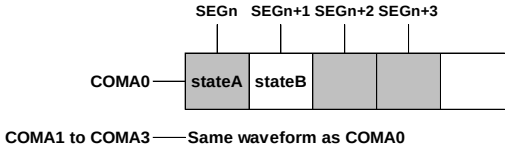
## LCD Driving Waveform - continued

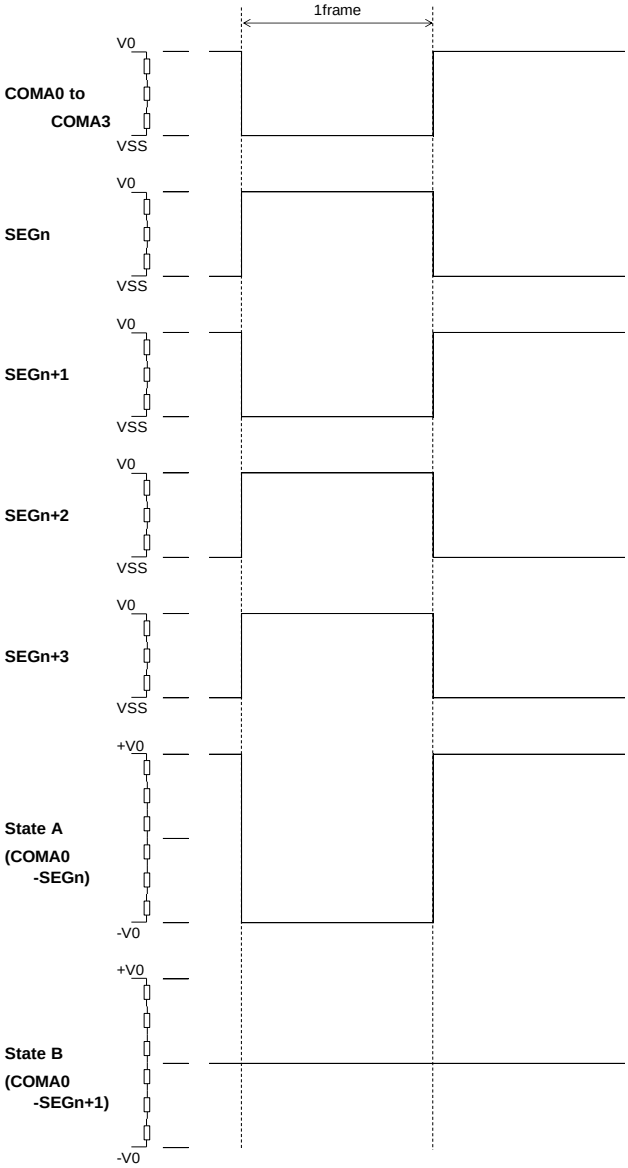
### Static Drive

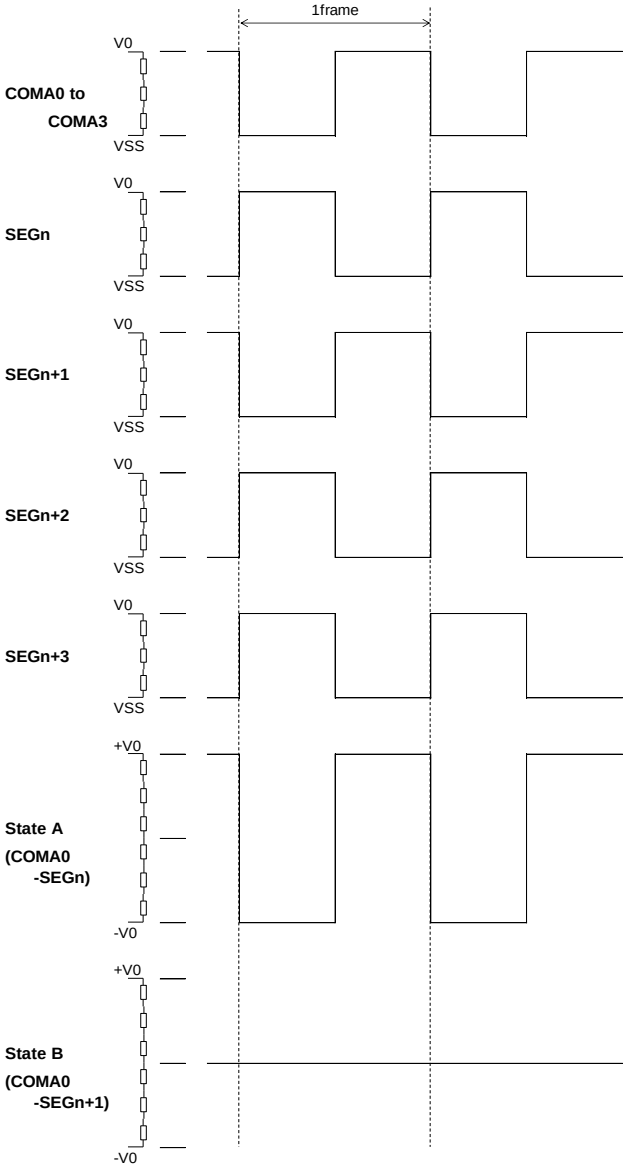
Frame Inversion




Line Inversion




Normally white type LCD case

Figure 53. LCD Waveform (Static Drive)


© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

### Example of Display Data

In case of LCD layout pattern shown in Figure 54. Example COM Line Pattern and Figure 55. Example SEG Line Pattern and DDRAM data shown in Table 11. DDRAM Data Example, display pattern will be shown as in Figure 56. Example Display Pattern.

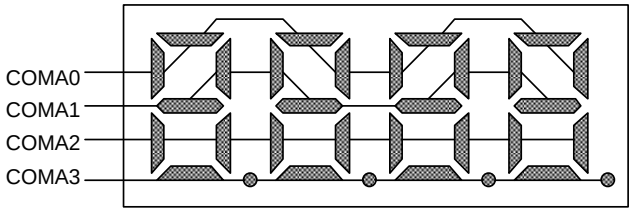



Figure 54. Example COM Line Pattern

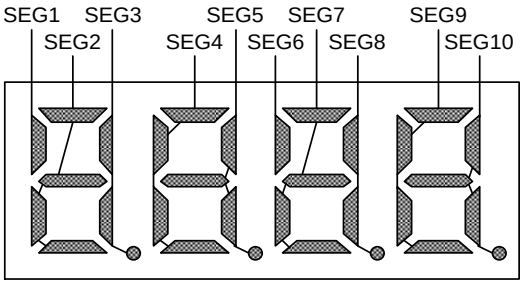



Figure 55. Example SEG Line Pattern

Table 11. DDRAM Data Example

| | SEG0 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 | SEG16 | SEG17 | SEG18 | SEG19 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| COMA0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COMA1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COMA2 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| COMA3 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Address | 00h | 01h | 02h | 03h | 04h | 05h | 06h | 07h | 08h | 09h | 0Ah | 0Bh | 0Ch | 0Dh | 0Eh | 0Fh | 10h | 11h | 12h | 13h |

(The COM scan order: COMSET P0 = "0")

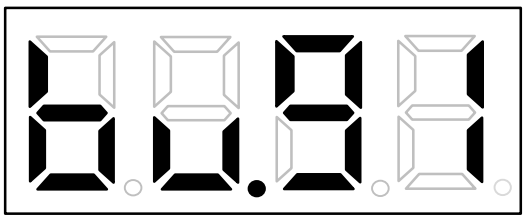


Figure 56. Example Display Pattern


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

### Initialize Sequence

Follow the Power On sequence below to set IC to initial reset condition.

Power On
↓
START condition
↓
9 clock pulses in SCL with SDA = High level
↓
STOP condition
↓
START condition
↓
9 clock pulses in SCL with SDA = High level
↓
STOP condition
↓
START condition
↓
Issue Slave Address
↓
Issue Control Byte
↓
Issue CMDXTN (Enter to Extension Mode)
↓
Issue SWRST (Execute Software Reset).

After Power On and before sending initialize sequence, each register value, DDRAM address and DDRAM data are random if POR is disabled by TR=VDD or power-on sequence cannot keep the conditions in **Figure 58. Power On / Off Waveform**.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Start Sequence

### Start Sequence Example1

| No. | Input | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Descriptions |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Power On | - | - | - | - | - | - | - | - | VDD = 0V→3.3V ($t_R$ = 1ms), VLCD = 0V→5.0V |
| 2 | Wait 100µs | - | - | - | - | - | - | - | - | Initialize BU91R64CH-M3BW |
| 3 | START | - | - | - | - | - | - | - | - | START condition |
| 4 | Dummy Byte | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 9 clock pulses in SCL with SDA = High level |
| 5 | STOP | - | - | - | - | - | - | - | - | STOP condition |
| 6 | START | - | - | - | - | - | - | - | - | START condition |
| 7 | Dummy Byte | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 9 clock pulses in SCL with SDA = High level |
| 8 | STOP | - | - | - | - | - | - | - | - | STOP condition |
| 9 | START | - | - | - | - | - | - | - | - | START condition |
| 10 | Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Issue Slave Address |
| 11 | Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Issue Control Byte |
| 12 | CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Enter to Extension Mode |
| 13 | SWRST | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Software Reset |
| 14 | STOP | - | - | - | - | - | - | - | - | STOP condition |
| 15 | START | - | - | - | - | - | - | - | - | START condition |
| 16 | Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Issue Slave Address |
| 17 | Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Issue Control Byte |
| 18 | MODESET1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Display Off |
| 19 | CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Enter to Extension Mode |
| 20 | MODESET2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | All detections: disabled |
| 21 | MODESET3 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Line Inversion, Normal Frequency Mode |
| 22 | CNTSET | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | V0 = 1.000 x VLCD level |
| 23 | RDCTL | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Read setting (disabled) |
| 24 | COMSET | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | COM Set |
| 25 | CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Enter to Normal Mode |
| 26 | FRSET | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Frame frequency = 155.3Hz |
| 27 | BLKCTL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Blink off |
| 28 | BLKCTL2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Data write access to Normal Display Area |
| 29 | SADSET | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Sub Address Set |
| 30 | ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Address Set |
| 31 | STOP | - | - | - | - | - | - | - | - | STOP condition |
| 32 | START | - | - | - | - | - | - | - | - | START condition |
| 33 | Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Issue Slave Address |
| 34 | Control Byte | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Issue Control Byte |
| 35 | Display Data | * | * | * | * | * | * | * | * | Address 00h to 01h |
| | Display Data | * | * | * | * | * | * | * | * | Address 02h to 03h |
| | : | : | : | : | : | : | : | : | : | : |
| | Display Data | * | * | * | * | * | * | * | * | Address 4Eh to 4Fh |
| 36 | STOP | - | - | - | - | - | - | - | - | STOP condition |
| 37 | START | - | - | - | - | - | - | - | - | START condition |
| 38 | Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Issue Slave Address |
| 39 | Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Issue Control Byte |
| 40 | MODESET1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Display On |
| 41 | STOP | - | - | - | - | - | - | - | - | STOP condition |

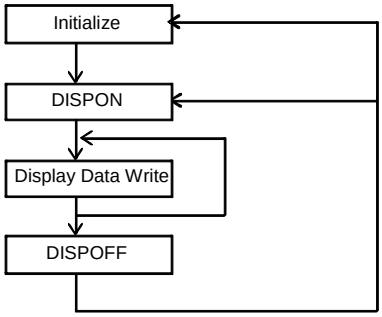
(*: don't care)


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Start Sequence – continued

### Start Sequence Example2




Initialize Sequence

DISPON Sequence

Display Data Write Sequence

DISPOFF Sequence

BU91R64CH-M3BW is initialized with “Initialize Sequence”, starts to display with “DISPON Sequence”, updates Display Data with “Display Data Write Sequence” and stops the display with “DISPOFF Sequence”.
Execute “DISPON Sequence” when MCU starts display again.

Initialize Sequence

| Input | Data | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| VDD on | | | | | | | | | |
| VLCD on | | | | | | | | | |
| Wait for 100µs | | | | | | | | | |
| START | | | | | | | | | |
| Dummy Byte | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Keep high in ACK bit |
| STOP | | | | | | | | | |
| START | | | | | | | | | |
| Dummy Byte | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Keep high in ACK bit |
| STOP | | | | | | | | | |
| START | | | | | | | | | |
| Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Enter to Extension Mode |
| SWRST | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Software Reset |
| STOP | | | | | | | | | |
| START | | | | | | | | | |
| Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| MODESET1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Display Off |
| CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Enter to Extension Mode |
| MODESET2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | All detections: disabled |
| MODESET3 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Inversion / FR setting |
| CNTSET | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Contrast Set |
| RDCTL | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Read setting |
| COMSET | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | COM Set |
| CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Enter to Normal Mode |
| FRSET | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Frame Frequency |
| BLKCTL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Blink setting |
| BLKCTL2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Data write setting |
| SADSET | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Sub Address Set |
| ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Address Set |
| STOP | | | | | | | | | |
| START | | | | | | | | | |
| Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| Control Byte | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Display Data | * | * | * | * | * | * | * | * | |
| : | | | | | | | | | |
| STOP | | | | | | | | | |

DISPON Sequence

| Input | Data | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| START | | | | | | | | | |
| Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Enter to Extension Mode |
| MODESET2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | All detections: disabled |
| MODESET3 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Inversion / FR setting |
| CNTSET | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Contrast Set |
| RDCTL | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Read setting |
| COMSET | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | COM Set |
| CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Enter to Normal Mode |
| FRSET | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Frame Frequency |
| BLKCTL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Blink setting |
| BLKCTL2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Data write setting |
| MODESET1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Display On |
| STOP | | | | | | | | | |

Display Data Write Sequence

| Input | Data | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| START | | | | | | | | | |
| Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| MODESET1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | Display On |
| CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | Enter to Extension Mode |
| MODESET2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | All detections: disabled |
| MODESET3 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Inversion / FR setting |
| CNTSET | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Contrast Set |
| RDCTL | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Read setting |
| COMSET | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | COM Set |
| CMDXTN | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | Enter to Normal Mode |
| FRSET | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Frame Frequency |
| BLKCTL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Blink setting |
| BLKCTL2 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | Data write setting |
| SADSET | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Sub Address Set |
| ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Address Set |
| STOP | | | | | | | | | |
| START | | | | | | | | | |
| Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| Control Byte | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Display Data | * | * | * | * | * | * | * | * | |
| : | | | | | | | | | |
| STOP | | | | | | | | | |

DISPOFF Sequence

| Input | Data | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| START | | | | | | | | | |
| Slave Address | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| Control Byte | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| MODESET1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Display Off |
| STOP | | | | | | | | | |

(*: don’t care)

Abnormal operation may occur in BU91R64CH-M3BW due to the effect of noise or other external factor. To avoid this phenomenon, it is highly recommended to input command according to sequence described above during initialization, Display On / Off and refresh of Display Data.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

### Cautions in Power On / Off

Please keep Power On / Off sequence as below waveform. To prevent incorrect display, malfunction and abnormal current, VDD must be turned on before VLCD In power up sequence. VDD must be turned off after VLCD In power down sequence. Please satisfies t1>0ns, t2>0ns.
To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

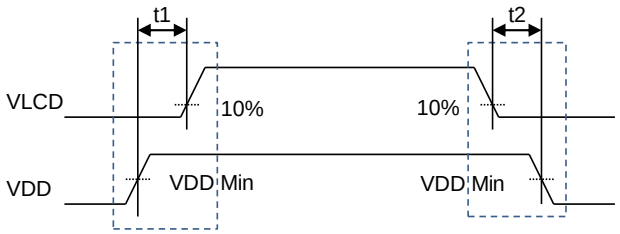



Figure 57. Recommended Power On / Off Sequence

BU91R64CH-M3BW has “POR” (Power On Reset) circuit and Software Reset function. Keep the following recommended Power On conditions in order to power up properly.
Set power up conditions to meet the recommended $t_R$, $t_F$, $t_{OFF}$, and $V_{BOT}$ specification below in order to ensure POR operation. Set terminal TR = VSS to enable POR circuit.

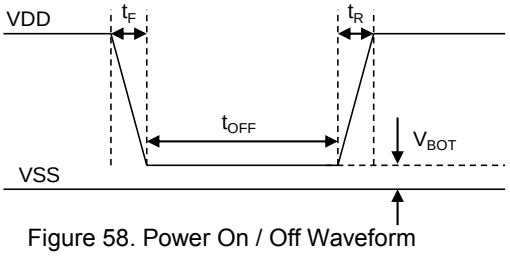


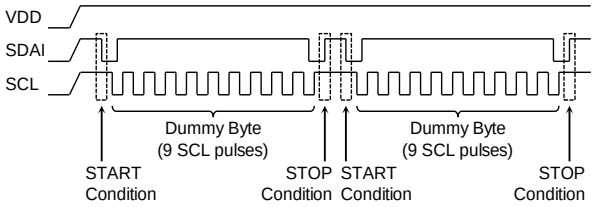
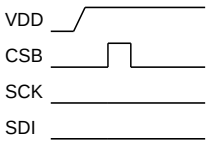

Figure 58. Power On / Off Waveform

Recommended condition of $t_R$, $t_F$, $t_{OFF}$, $V_{BOT}$ (Ta = 25°C)

| $t_R$(Note) | $t_F$(Note) | $t_{OFF}$(Note) | $V_{BOT}$(Note) |
|---|---|---|---|
| 1ms to 500ms | 1ms to 500ms | Min 20ms | Less than 0.1V |

*(Note)* This function is guaranteed by design, not tested in production process.

If it is difficult to keep above conditions, execute the following sequence as quickly as possible after Power On. Setting TR = VDD disables the POR circuit, in such case, execute the following sequence. Note that however it cannot accept command while supply is unstable or below the minimum supply range. Note also that software reset is not a complete alternative to POR function.

| 2-wire Serial Interface | 3-wire Serial Interface |
|---|---|
| 1. Generate two dummy bytes with START and STOP Conditions SDAI must be “1” as data.<br><br><br>Figure 59. Dummy Clock / STOP / START Condition<br><br>2. Execute Software Reset as follows<br>Send START Condition<br>Send Slave Address (7Ch, 7Eh, 70h or 72h)<br>Send Control Byte (00h)<br>Send CMDXTN command (FDh)<br>Send SWRST command (81h) | 1. Set CSB to High level.<br><br><br>Figure 60. CSB Timing<br><br>2. Set CSB to low level, then execute Software Reset as follows:<br>Send CMDXTN command (FDh)<br>Send SWRST command (81h) |


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Display Off Operation in External Clock Mode

Clock stop timing in Display Off

After receiving MODESET1 Display Off (DISPOFF), BU91R64CH-M3BW enters to DISPOFF sequence synchronized with frame then Segment and Common terminals output VSS level.
Therefore, in External Clock Mode, it is necessary to input the external clock (minimum 26 clock pulses) based on each Frame Frequency setting after sending MODESET1 DISPOFF command.

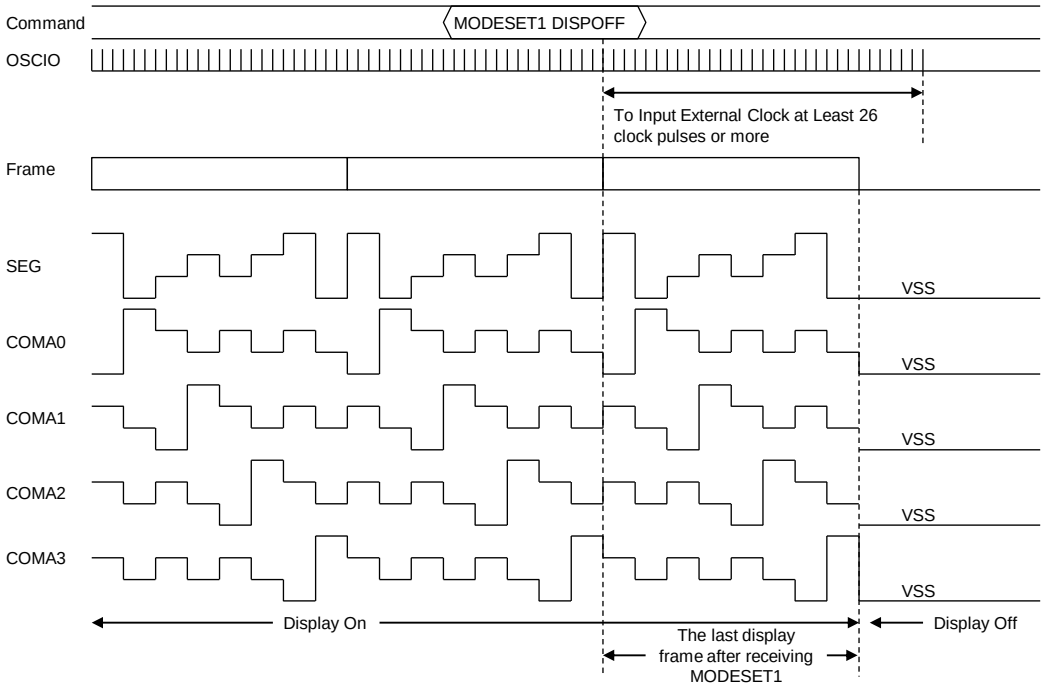



Figure 61. External Clock Stop Timing

In case of External Clock Mode, a clock signal shall be always supplied to BU91R64CH-M3BW. Removing the clock may freeze the LCD in a DC state which is not suitable for the LCD.

### In Multi-chip Structure in Internal Clock Mode

In multi-chip structure and in internal clock mode, clock signal for Slave 1 to Slave 3 display are provided by Master IC. So if Master IC receives Display off before Slave ICs, the clock from Master IC will stop and Slave ICs hold the SEG and COM level not VSS level, then causes abnormal display. To prevent this issue, DISPOFF must be sent to Slave ICs earlier than to Master IC.

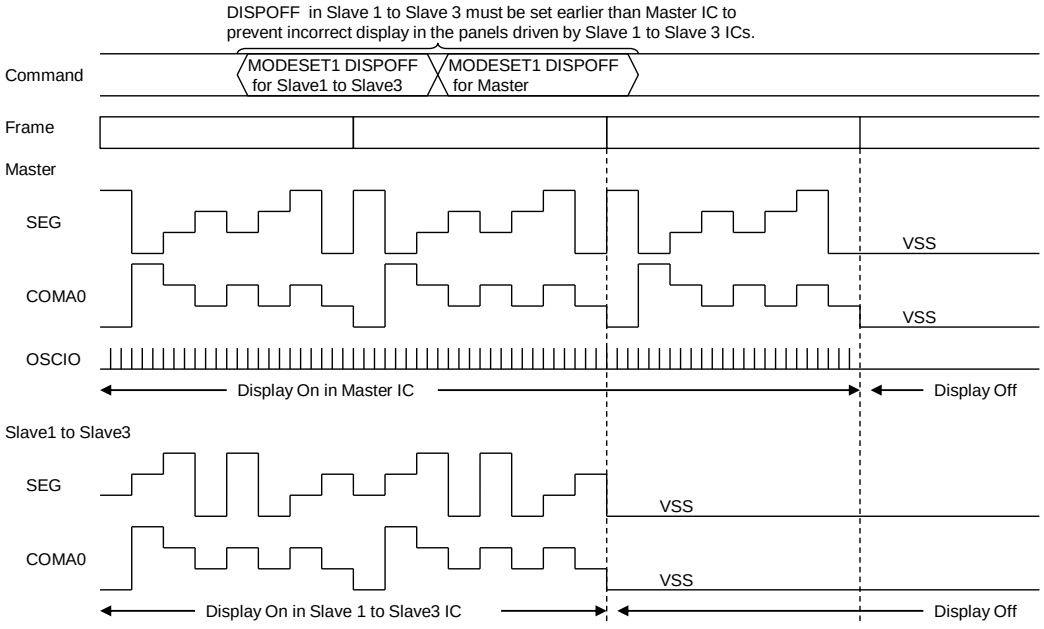



Figure 62. DISPOFF Sequence in Multi-chip Structure


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

**Note on The Multiple Device Connection to 2-wire Serial Interface.**

Do not access the other device without power supply (VDD) to the BU91R64CH-M3BW.

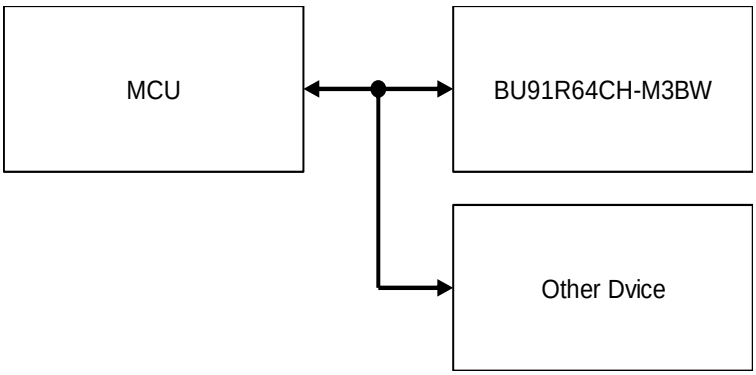



Figure 63. Example of BUS Connection

To control the slope of the falling edge, a capacitor is connected between gate and drain of a NMOS transistor as shown in the following figure. The gate is in a high-impedance state when the power supply (VDD) is not supplied.

In this condition, the gate voltage is pulled up by the current flow through the capacitance as a result of the SDAO signal's transition from low to high.

The NMOS transistor turns on and draws some current (Ids) from the SDAO if the gate voltage (Vg) is higher than the threshold voltage (Vth).

An external resistor (R) is connected between the power line and SDAO line to keep the SDA line as logic high.
But the line cannot be kept as logic high if the voltage drop (R*Ids) is large.

Apply power supply (VDD) to BU91R64CH-M3BW when the multiple devices are on the same bus.

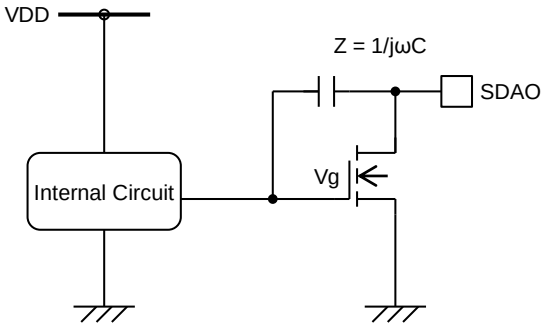



Figure 64. SDA Output Cell Structure

**Note in Case that the SDA is Stuck at LOW**

Normally, BU91R64CH-M3BW SDA status is controlled by MCU, so it set SDA to VSS level only in ACK timing and output “0” case during read-back state.
If the data line (SDAO) is stuck at LOW by BU91R64CH-M3BW unexpectedly, MCU should send two dummy bytes with START and STOP Conditions with SDAI = High. BU91R64CH-M3BW will release SDAO stuck within this sequence.

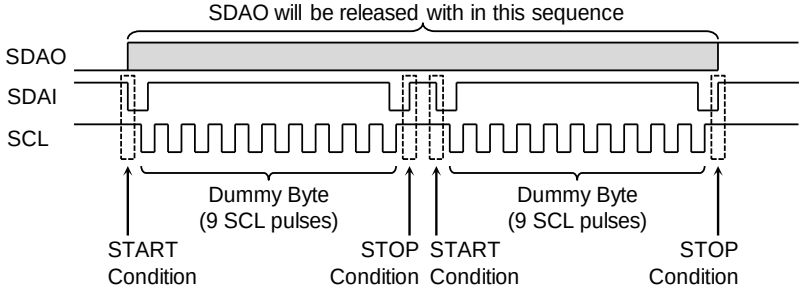



Figure 65. Recovery Sequence from SDA Stuck


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

12. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Operational Notes – continued

**13. Disturbance Light**

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Ordering Information

B U 9 1 R 6 4 C H - M 3 B W

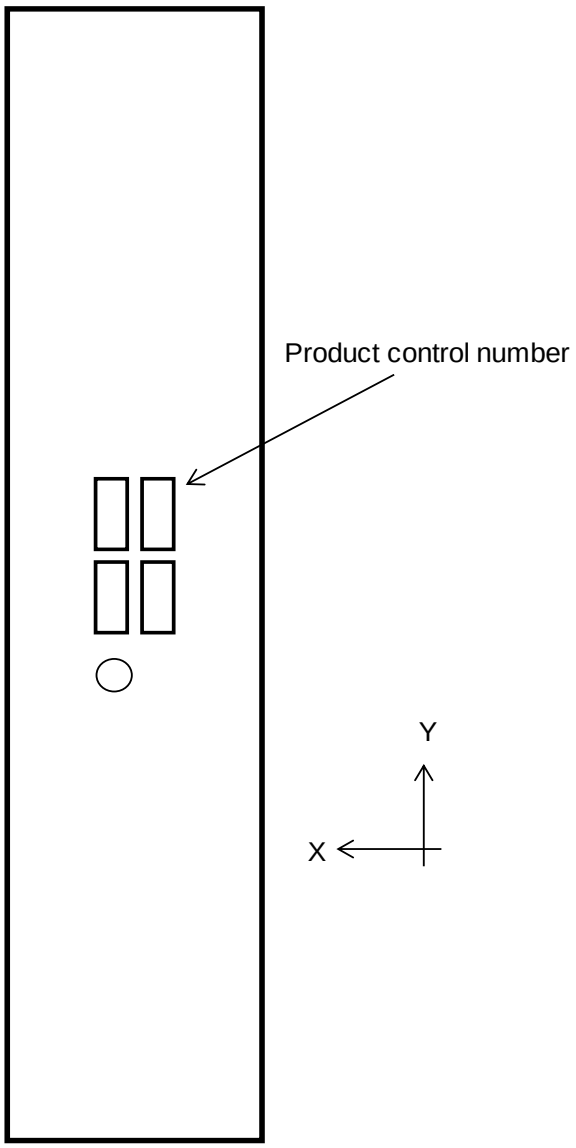
Part Number

Product Rank
M: for Automotive

## Lineup

| Package | | Orderable Part Number |
|---|---|---|
| Au Bump with Tray | MOQ: 10,800pcs | BU91R64CH-M3BW |

## Marking Diagram




(Bottom View)

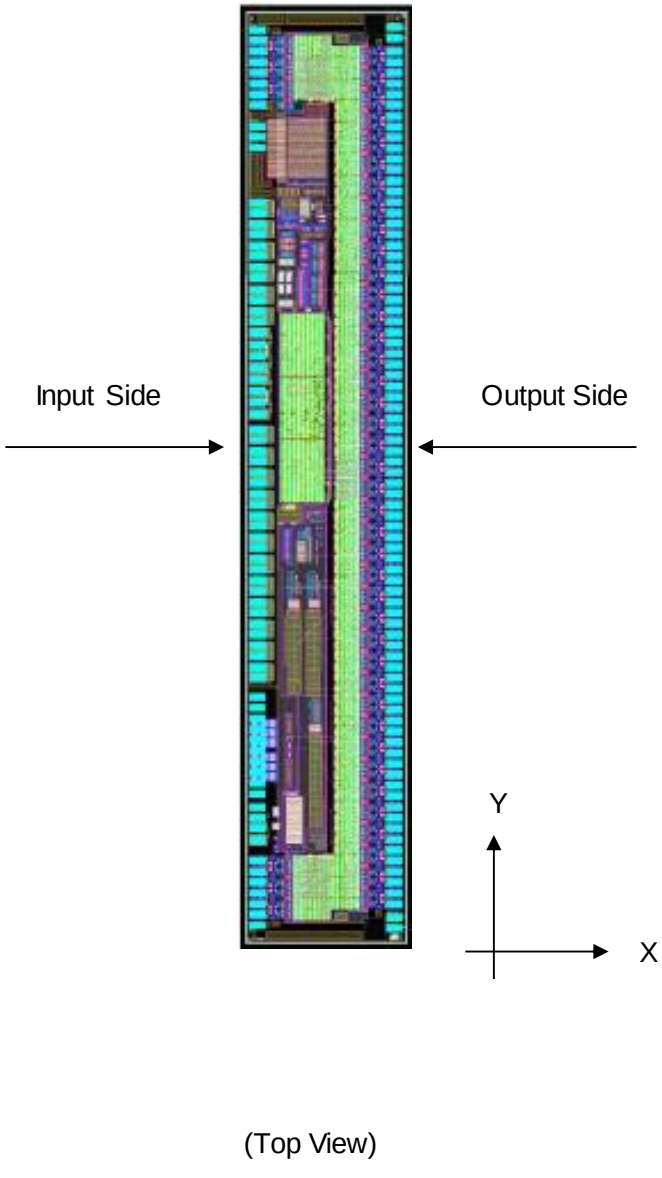

© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Packing Quantity

| | | | |
|---|---|---|---|
| Packing QTY. (Standard QTY) | Tray: | 90 | pcs / Tray |
| | Block: | 450 | pcs / Block (1 block = 5 trays) |
| | Vacuum Pack: | 5,400 | pcs / Vacuum pack (1 vacuum pack = 12 blocks) |
| Packing QTY. (Standard QTY) | | 10,800 | pcs / inner Box (1 inner box = 2 vacuum packs) |
| | | 21,600 | pcs / outer Box (1 outer box = 2 inner boxes) |

## Pallet Drawing



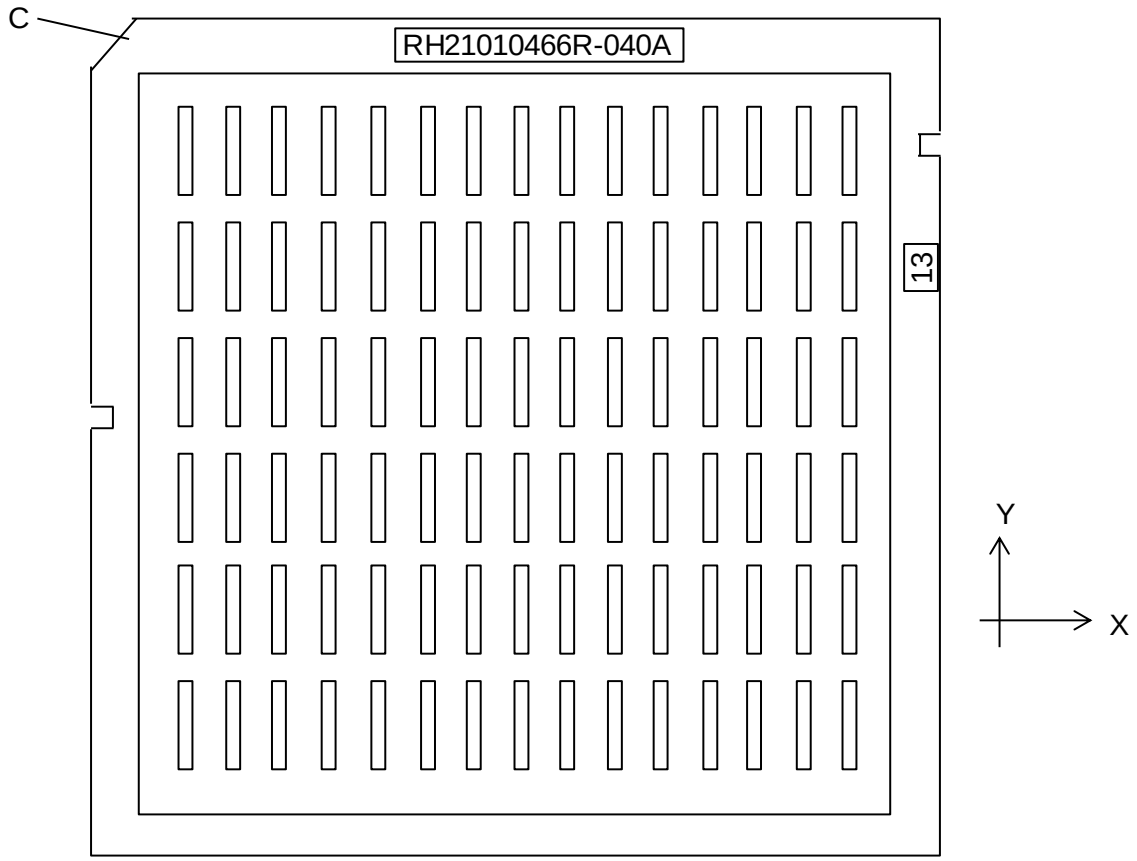

(Top View)


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

**Package Condition**

Products should be aligned to the same direction.
The alignment is based on “Chamfering” side as shown in the following drawing.



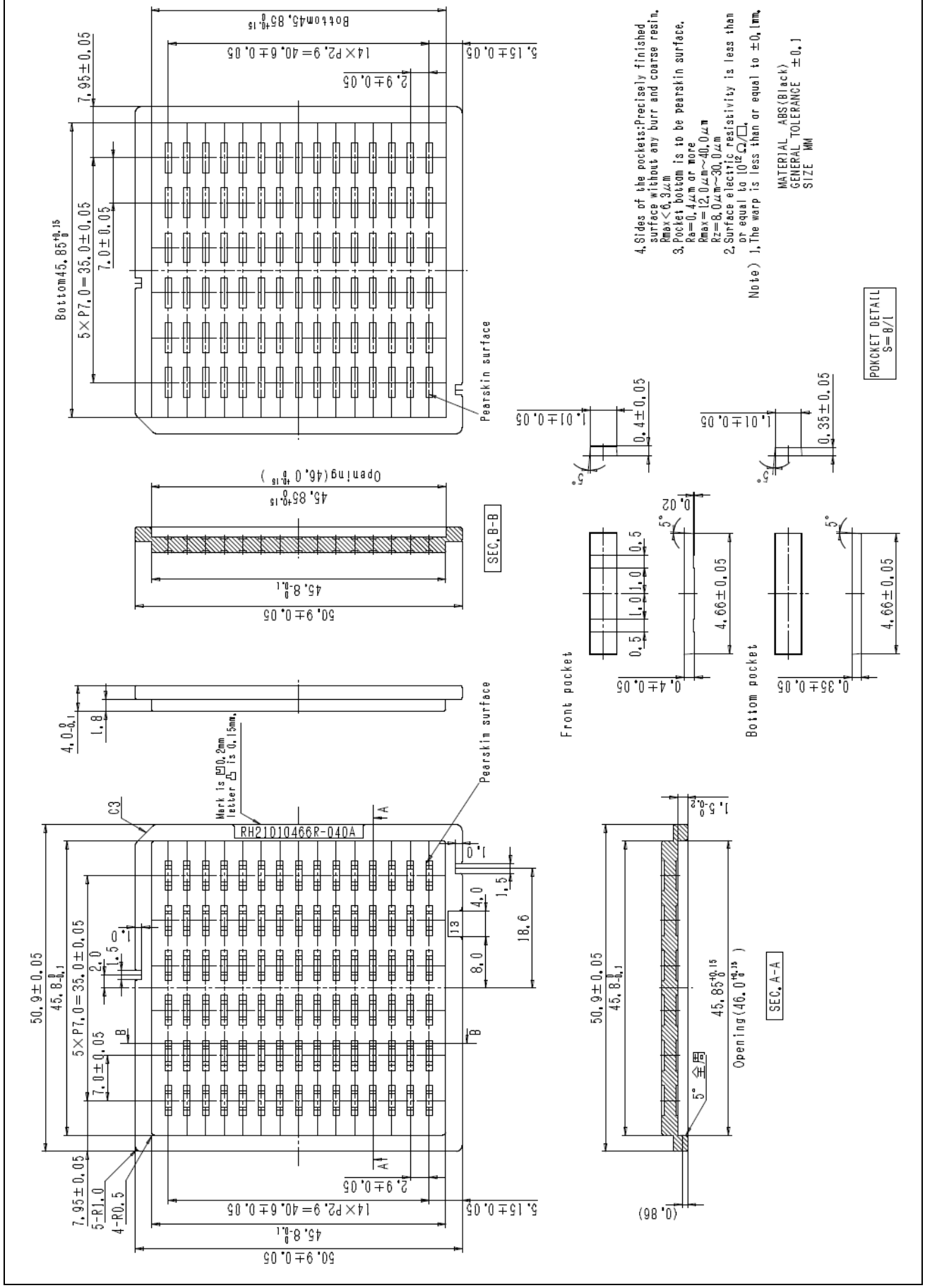


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

**Physical Dimension Tray Information**

| Package Name | Au Bump with Tray |
|---|---|





© 2016 ROHM Co., Ltd. All rights reserved.


Downloaded from Arrow.com.

## Revision History

| Data | Revision | Changes |
|---|---|---|
| 18.May. 2018 | 001 | New Release |


© 2016 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

# Notice

## Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|---|---|---|---|
| CLASSⅢ | CLASSⅢ | CLASSⅡb | CLASSⅢ |
| CLASSⅣ | | CLASSⅢ | |

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including $Cl_2$, $H_2S$, $NH_3$, $SO_2$, and $NO_2$
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification


© 2015 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

## Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

## Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

## Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

## Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

## Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

## Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

## Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.


© 2015 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.

## General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.


© 2015 ROHM Co., Ltd. All rights reserved.

Downloaded from Arrow.com.