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3.5 MHz, Wide Supply, Operational Amplifier Rail-to-Rail Output

NCS2004, NCS2004A

The NCS2004 operational amplifier provides rail-to-rail output operation. The output can swing within 70 mV to the positive rail and 30 mV to the negative rail. This rail-to-rail operation enables the user to make optimal use of the entire supply voltage range while taking advantage of 3.5 MHz bandwidth. The NCS2004 can operate on supply voltage as low as 2.5 V over the temperature range of −40 °C to 125 °C. The high bandwidth provides a slew rate of 2.4 V/μs while only consuming a typical 390 μA of quiescent current. Likewise the NCS2004 can run on a supply voltage as high as 16 V making it ideal for a broad range of battery operated applications. Since this is a CMOS device it has high input impedance and low bias currents making it ideal for interfacing to a wide variety of signal sensors. In addition it comes in either a small SC-88A or UDFN package allowing for use in high density PCB’s.

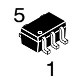
Features

- Rail-To-Rail Output
- Wide Bandwidth: 3.5 MHz
- High Slew Rate: 2.4 V/μs
- Wide Power Supply Range: 2.5 V to 16 V
- Low Supply Current: 390 μA
- Low Input Bias Current: 45 pA
- Wide Temperature Range: −40 °C to 125 °C
- Small Packages: 5-Pin SC-88A and UDFN6 1.6x1.6
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

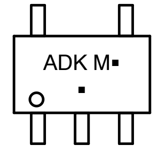
Applications

- Notebook Computers
- Portable Instruments

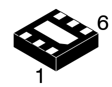
MARKING DIAGRAMS



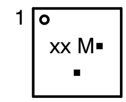
SC-88A (SC-70-5) SN SUFFIX CASE 419A



ADK = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

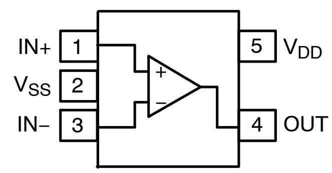


UDFN6 CASE 517AP

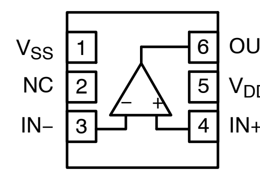


xx = Specific Device Code
AA for NCS2004
AC for NCS2004A
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PIN CONNECTIONS



SC-88A (Top View)



UDFN (Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCS2004MUTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 1)

NCS2004SQ3T2G	SC-88A (Pb-Free)	3000 / Tape & Reel
NCS2004AMUTAG	UDFN6 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

1. **DISCONTINUED:** These devices are not available. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage	16.5	V
V_{ID}	Input Differential Voltage	± Supply Voltage	V
V_I	Input Common Mode Voltage Range	−0.2 V to (V_{DD} + 0.2 V)	V
I_I	Maximum Input Current	± 10	mA
I_O	Output Current Range	± 100	mA
	Continuous Total Power Dissipation (Note 2)	200	mW
T_J	Maximum Junction Temperature	150	°C
θ_{JA}	Thermal Resistance	333	°C/W
T_{stg}	Operating Temperature Range (free-air)	−40 to 125	°C
T_{stg}	Storage Temperature	−65 to 150	°C
	Mounting Temperature (Infrared or Convection - 20 sec)	260	°C
V_{ESD}	Machine Model Human Body Model	300 2000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Continuous short circuit operation to ground at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 °C. Output currents in excess of 45 mA over long term may adversely affect reliability. Shorting output to either V+ or V- will adversely affect reliability.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V, 3.3 V, 5 V and ± 5 V, T_A = 25 °C, $R_L \geq$ 10 kΩ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IO}	Input Offset Voltage (NCS2004)	VIC = V_{DD}/2, V_O = V_{DD}/2, R_L = 10 kΩ, R_S = 50 Ω		–	0.5	5.0	mV
		T_A = −40 °C to +125 °C		–	–	7.0	
V_{IO}	Input Offset Voltage (NCS2004A)	VIC = V_{DD}/2, V_O = V_{DD}/2, R_L = 10 kΩ, R_S = 50 Ω		–	–	3.0	mV
		T_A = −40 °C to +125 °C		–	–	5.0	
ICV_{OS}	Offset Voltage Drift	VIC = V_{DD}/2, V_O = V_{DD}/2, R_L = 10 kΩ, R_S = 50 Ω		–	2.0	–	μV/°C
CMRR	Common Mode Rejection Ratio	0 V ≤ VIC ≤ V_{DD} - 1.35 V, R_S = 50 Ω	V_{DD} = 2.5 V	55	94	–	dB
		T_A = −40 °C to +125 °C		52	–	–	
		0 V ≤ VIC ≤ V_{DD} - 1.35 V, R_S = 50 Ω	V_{DD} = 5 V	65	130	–	
		T_A = −40 °C to +125 °C		62	–	–	
		0 V ≤ VIC ≤ V_{DD} - 1.35 V, R_S = 50 Ω	V_{DD} = ± 5 V	69	140	–	
		T_A = −40 °C to +125 °C		66	–	–	
PSRR	Power Supply Rejection Ratio	V_{DD} = 2.5 V to 16 V, VIC = V_{DD}/2, No Load		70	135	–	dB
		T_A = −40 °C to +125 °C		65	–	–	
A_{VD}	Large Signal Voltage Gain	$V_{O(pp)}$ = V_{DD}/2, R_L = 10 kΩ	V_{DD} = 2.5 V	90	130	–	dB
		T_A = −40 °C to +125 °C		76	–	–	
		$V_{O(pp)}$ = V_{DD}/2, R_L = 10 kΩ	V_{DD} = 3.3 V	92	123	–	
		T_A = −40 °C to +125 °C		76	–	–	
		$V_{O(pp)}$ = V_{DD}/2, R_L = 10 kΩ	V_{DD} = 5 V	95	127	–	
		T_A = −40 °C to +125 °C		86	–	–	
		$V_{O(pp)}$ = V_{DD}/2, R_L = 10 kΩ	V_{DD} = ± 5 V	95	130	–	
		T_A = −40 °C to +125 °C		90	–	–	

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V, 3.3 V, 5 V and ±5 V, T_A = 25 °C, R_L ≥ 10 kΩ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_B	Input Bias Current	V_{DD} = 5 V, VIC = V_{DD}/2, V_O = V_{DD}/2, R_S = 50 Ω	T_A = 25 °C	–	45	150	pA
			T_A = 125°C	–		1000	
I_{IO}	Input Offset Current	V_{DD} = 5 V, VIC = V_{DD}/2, V_O = V_{DD}/2, R_S = 50 Ω	T_A = 25 °C	–	45	150	pA
			T_A = 125 °C	–	–	1000	
$r_{i(d)}$	Differential Input Resistance			–	1000	–	GΩ
C_{IC}	Common-mode Input Capacitance	f = 21 kHz		–	8.0	–	pF
V_{OH}	Output Swing (High-level)	VIC = V_{DD}/2, I_{OH} = −1 mA	V_{DD} = 2.5 V	2.35	2.43	–	V
		T_A = −40 °C to +125 °C		2.28	–	–	
		VIC = V_{DD}/2, I_{OH} = −1 mA	V_{DD} = 3.3 V	3.15	3.21	–	
		T_A = −40 °C to +125 °C		3.00	–	–	
		VIC = V_{DD}/2, I_{OH} = −1 mA	V_{DD} = 5 V	4.8	4.93	–	
		T_A = −40 °C to +125 °C		4.75	–	–	
		VIC = V_{DD}/2, I_{OH} = −1 mA	V_{DD} = ±5 V	4.92	4.96	–	
		T_A = −40 °C to +125 °C		4.9	–	–	
		VIC = V_{DD}/2, I_{OH} = −5 mA	V_{DD} = 2.5 V	1.7	2.14	–	V
		T_A = −40 °C to +125 °C		1.5	–	–	
		VIC = V_{DD}/2, I_{OH} = −5 mA	V_{DD} = 3.3 V	2.5	2.89		
		T_A = −40 °C to +125 °C		2.1	–	–	
		VIC = V_{DD}/2, I_{OH} = −5 mA	V_{DD} = 5 V	4.5	4.68	–	
		T_A = −40 °C to +125 °C		4.35	–	–	
		VIC = V_{DD}/2, I_{OH} = −5 mA	V_{DD} = ±5 V	4.7	4.78	–	
		T_A = −40 °C to +125 °C		4.65	–	–	
V_{OL}	Output Swing (Low-level)	VIC = V_{DD}/2, I_{OL} = −1 mA	V_{DD} = 2.5 V	–	0.03	0.15	V
		T_A = −40 °C to +125 °C		–	–	0.22	
		VIC = V_{DD}/2, I_{OL} = −1 mA	V_{DD} = 3.3 V	–	0.03	0.15	
		T_A = −40 °C to +125 °C		–	–	0.22	
		VIC = V_{DD}/2, I_{OL} = −1 mA	V_{DD} = 5 V	–	0.03	0.1	
		T_A = −40 °C to +125 °C		–	–	0.15	
		VIC = V_{DD}/2, I_{OL} = −1 mA	V_{DD} = ±5 V	–	0.05	0.08	
		T_A = −40 °C to +125 °C		–	–	0.1	
		VIC = V_{DD}/2, I_{OL} = −5 mA	V_{DD} = 2.5 V	–	0.15	0.7	V
		T_A = −40 °C to +125 °C		–	–	1.1	
		VIC = V_{DD}/2, I_{OL} = −5 mA	V_{DD} = 3.3 V	–	0.13	0.7	
		T_A = −40 °C to +125 °C		–	–	1.1	
		VIC = V_{DD}/2, I_{OL} = −5 mA	V_{DD} = 5 V	–	0.13	0.4	
		T_A = −40 °C to +125 °C		–	–	0.5	
		VIC = V_{DD}/2, I_{OL} = −5 mA	V_{DD} = ±5 V	–	0.16	0.3	
		T_A = −40 °C to +125 °C		–	–	0.35	

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V, 3.3 V, 5 V and ±5 V, T_A = 25 °C, R_L ≥ 10 kΩ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_O	Output Current	V_O = 0.5 V from rail, V_{DD} = 2.5 V	Positive rail	–	4.0	–	mA
			Negative rail	–	5.0	–	
		V_O = 0.5 V from rail, V_{DD} = 5 V	Positive rail	–	7.0	–	
			Negative rail	–	8.0	–	
		V_O = 0.5 V from rail, V_{DD} = 10 V	Positive rail	–	13	–	
			Negative rail	–	12	–	
I_{DD}	Power Supply Quiescent Current	V_O = V_{DD}/2	V_{DD} = 2.5 V	–	380	560	μA
			V_{DD} = 3.3 V	–	385	620	
			V_{DD} = 5 V	–	390	660	
			V_{DD} = 10 V	–	400	800	
		T_A = −40 °C to +125 °C		–	–	1000	

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 2.5 V, 5 V, & ±5 V, T_A = 25 °C, and R_L ≥ 10 kΩ unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UGBW	Unity Gain Bandwidth	R_L = 2 kΩ, C_L = 10 pF	V_{DD} = 2.5 V	–	3.2	–	MHz
			V_{DD} = 5 V to 10 V	–	3.5	–	
SR	Slew Rate at Unity Gain	$V_{O(pp)}$ = V_{DD}/2, R_L = 10 kΩ, C_L = 50 pF	V_{DD} = 2.5 V	1.35	2.0	–	V/μS
		T_A = −40 °C to +125 °C		1	–	–	
		$V_{O(pp)}$ = V_{DD}/2, R_L = 10 kΩ, C_L = 50 pF	V_{DD} = 5 V	1.45	2.3	–	
		T_A = −40 °C to +125 °C		1.2	–	–	
		$V_{O(pp)}$ = V_{DD}/2, R_L = 10 kΩ, C_L = 50 pF	V_{DD} = ±5 V	1.8	2.6	–	
		T_A = −40 °C to +125 °C		1.3	–	–	
θ_m	Phase Margin	R_L = 2 kΩ, C_L = 10 pF		–	45	–	°
	Gain Margin	R_L = 2 kΩ, C_L = 10 pF		–	14	–	dB
t_S	Settling Time to 0.1%	V-step(pp) = 1 V, AV = −1, R_L = 2 kΩ, C_L = 10 pF	V_{DD} = 2.5 V	–	2.9	–	μS–
		V-step(pp) = 1 V, AV = −1, R_L = 2 kΩ, C_L = 68 pF	V_{DD} = 5 V, ±5 V	–	2.0	–	
THD+N	Total Harmonic Distortion plus Noise	V_{DD} = 2.5 V, $V_{O(pp)}$ = V_{DD}/2, R_L = 2 kΩ, f = 10 kHz	AV = 1	–	0.004	–	%
			AV = 10	–	0.04	–	
			AV = 100	–	0.3	–	
		V_{DD} = 5 V, ± 5 V, $V_{O(pp)}$ = V_{DD}/2, R_L = 2 kΩ, f = 10 kHz	AV = 1	–	0.004	–	
			AV = 10	–	0.04	–	
			AV = 100	–	0.03	–	
e_n	Input-Referred Voltage Noise	f = 1 kHz		–	30	–	nV/√Hz
		f = 10 kHz		–	20	–	
i_n	Input-Referred Current Noise	f = 1 kHz		–	0.6	–	fA/√Hz

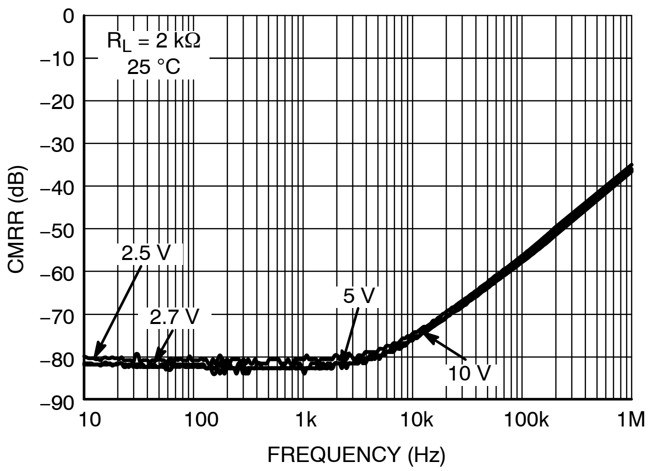


Figure 1. CMRR vs. Frequency

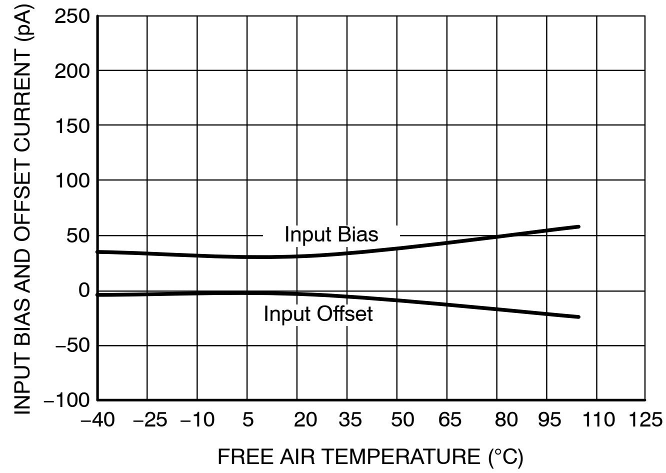


Figure 2. Input Bias and Offset Current vs. Temperature

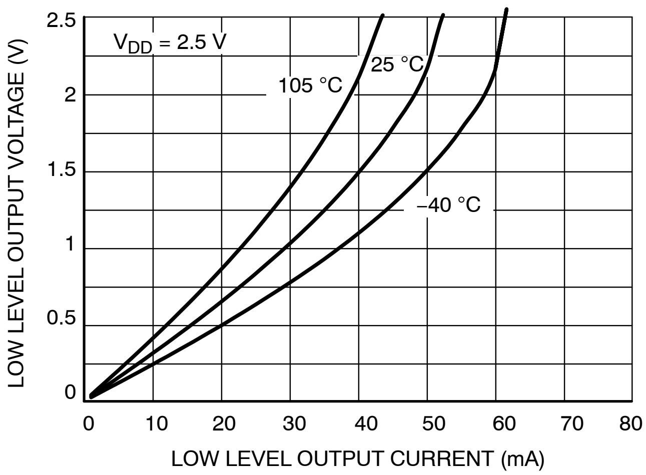


Figure 3. 2.5 V V_{OL} vs. I_{out}

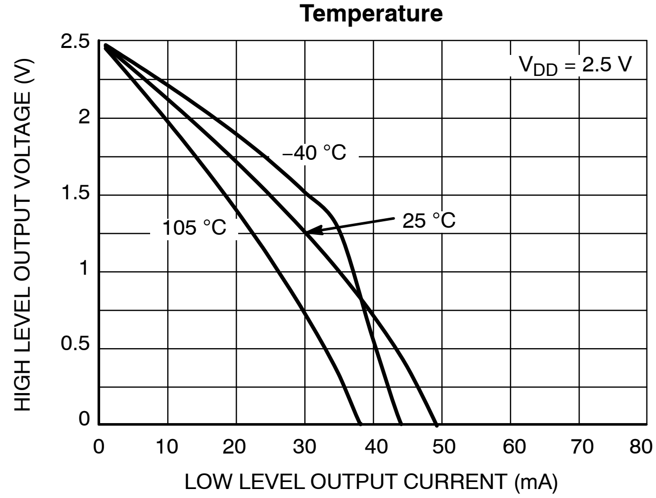


Figure 4. 2.5 V V_{OH} vs. I_{out}

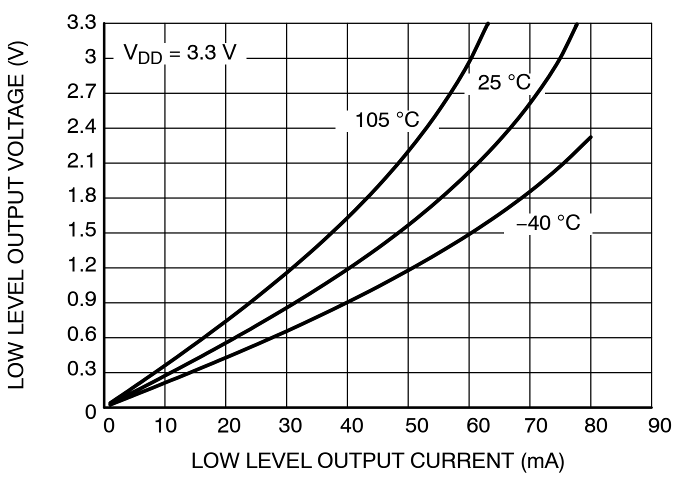


Figure 5. 3.3 V V_{OL} vs. I_{out}

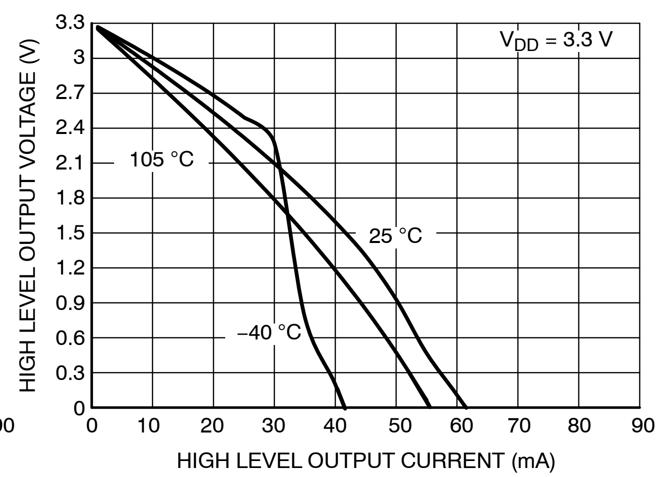


Figure 6. 3.3 V V_{OH} vs. I_{out}

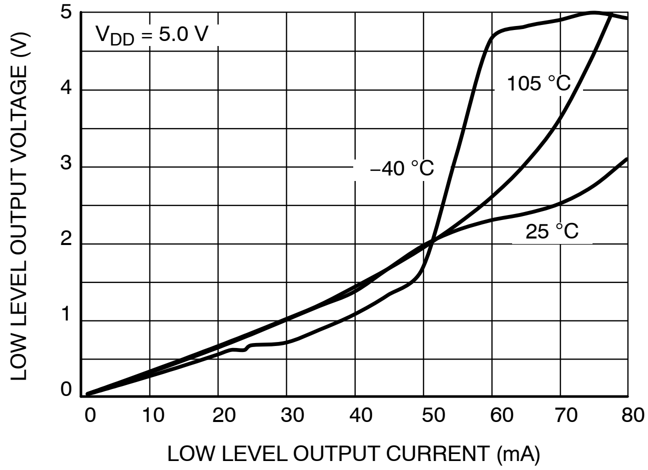


Figure 7. V_{OL} vs. I_{out}

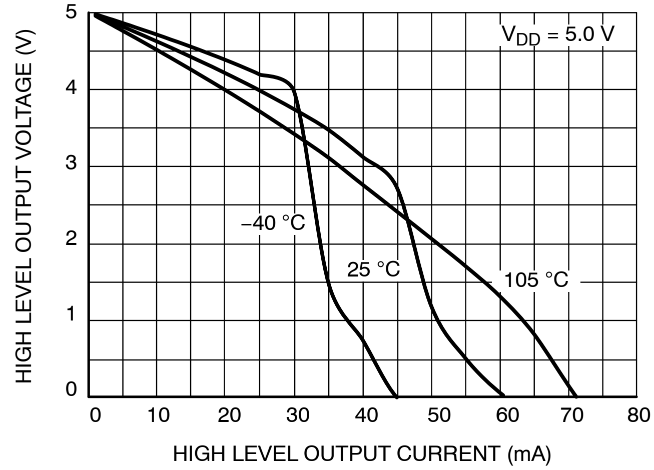


Figure 8. V_{OH} vs. I_{out}

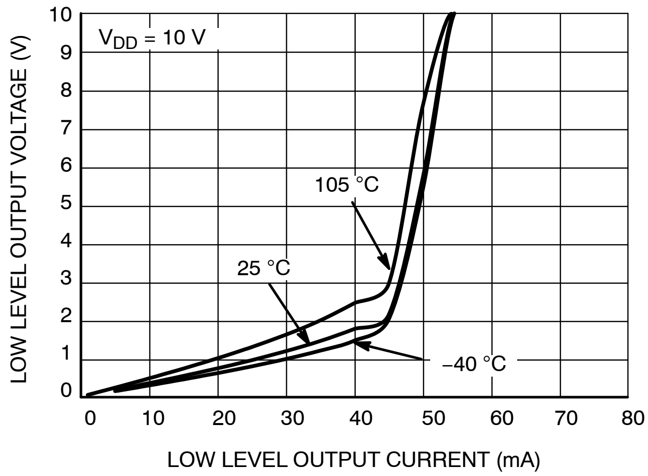


Figure 9. 10 V V_{OL} vs. I_{out}

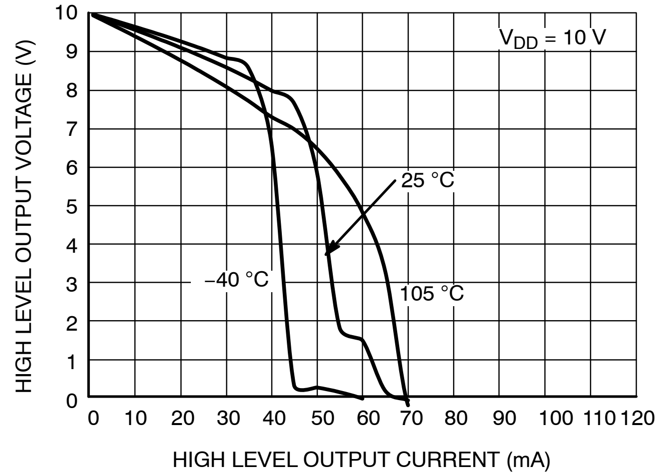


Figure 10. 10 V V_{OH} vs. I_{out}

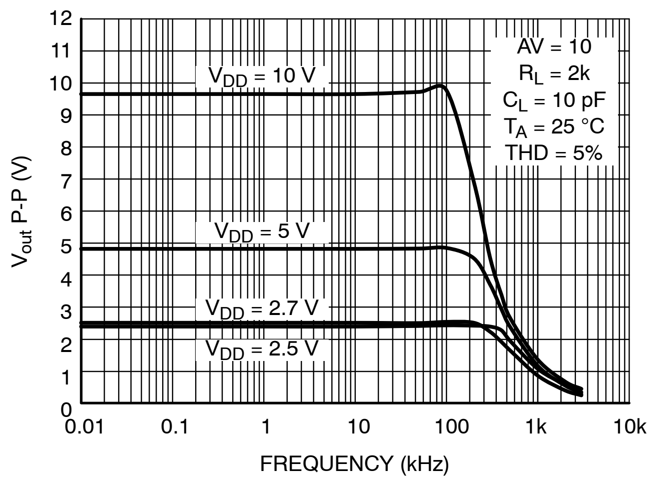


Figure 11. Peak-to-Peak Output vs. Supply vs. Frequency

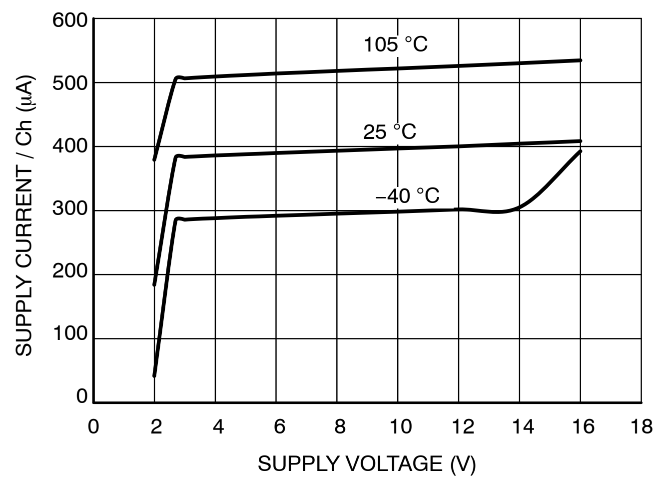


Figure 12. Supply Current vs. Supply Voltage

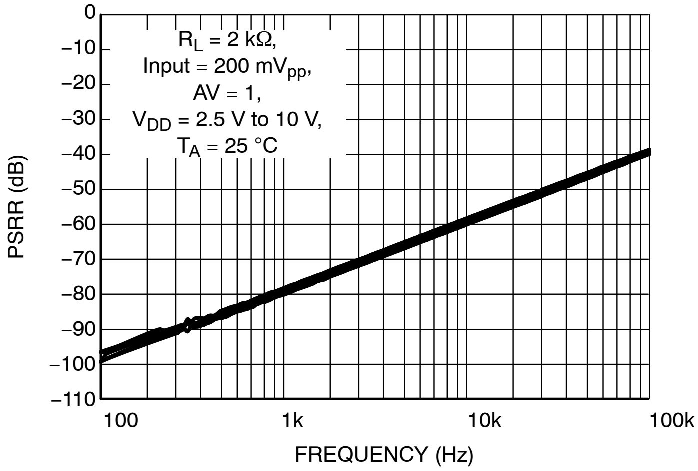


Figure 13. PSRR vs. Frequency

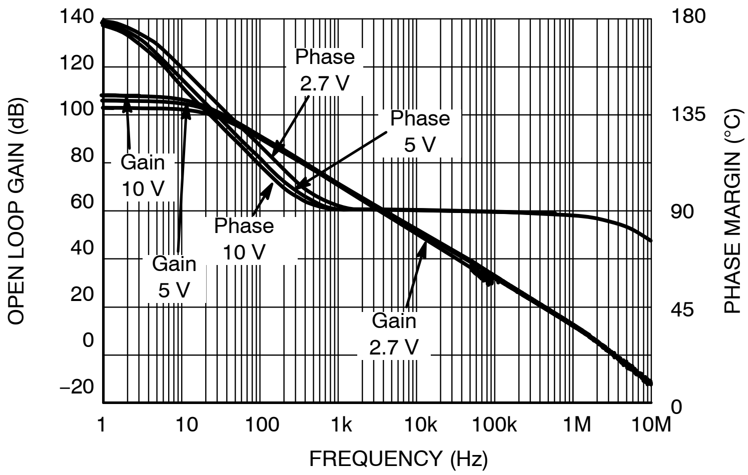


Figure 14. Open Loop Gain and Phase vs. Frequency

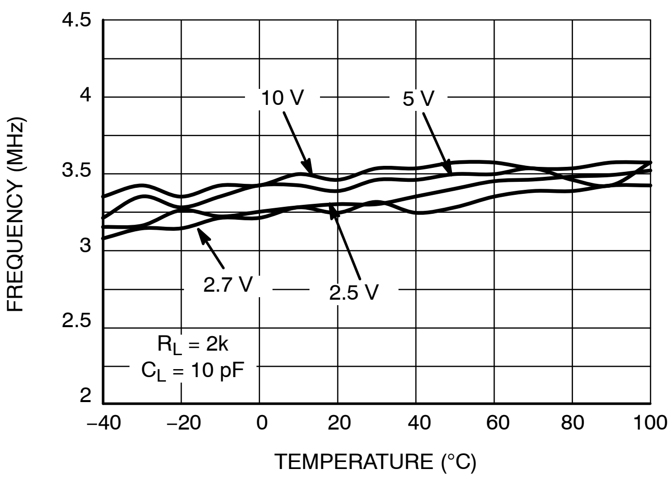


Figure 15. Gain Bandwidth Product vs. Temperature

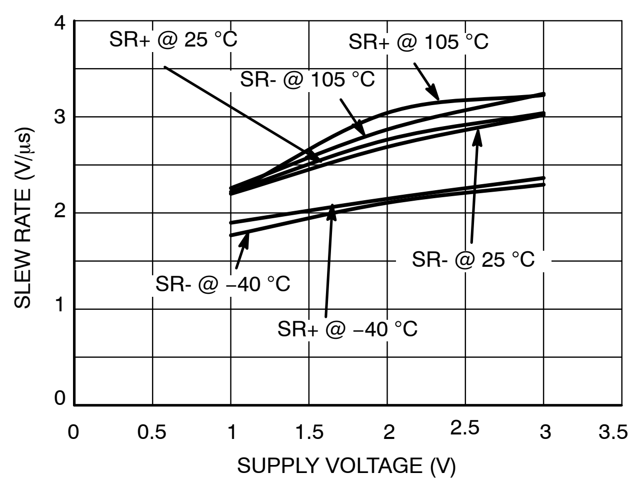


Figure 16. Slew Rate vs. Supply Voltage

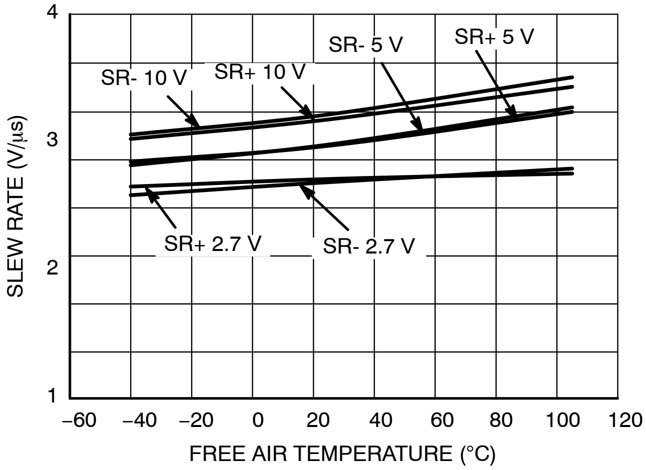


Figure 17. Slew Rate vs. Temperature

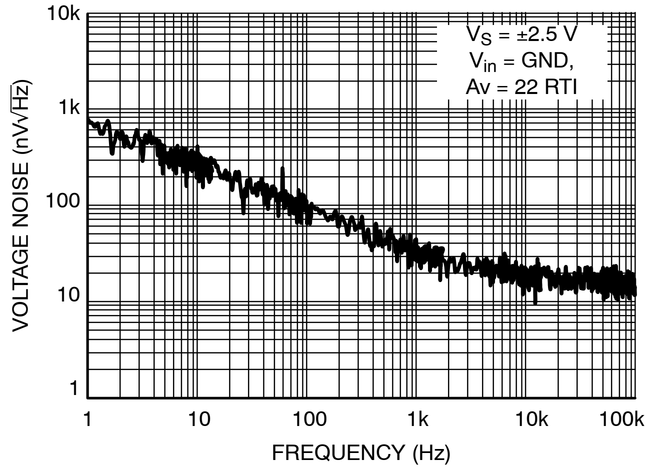


Figure 18. Voltage Noise vs. Frequency

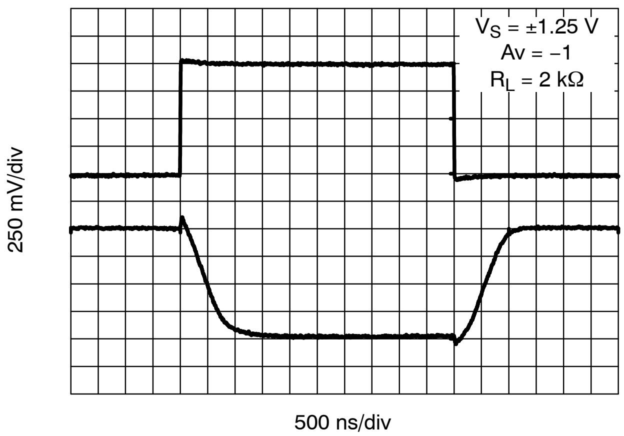


Figure 19. 2.5 V Inverting Large Signal Pulse Response

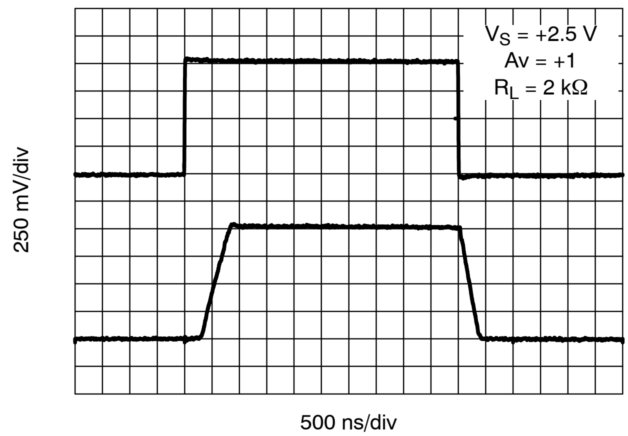


Figure 20. 2.5 V Non-Inverting Large Signal Pulse Response

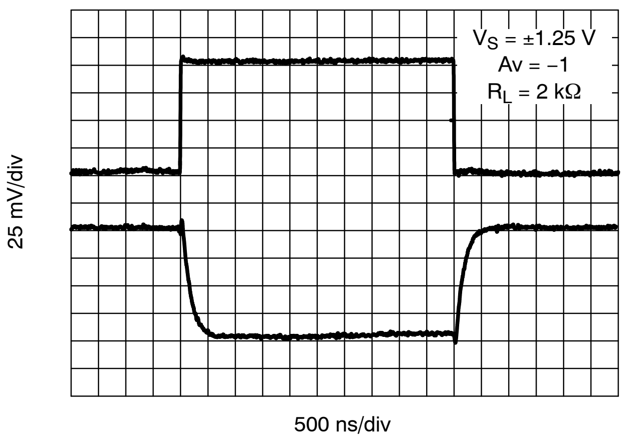


Figure 21. 2.5 V Inverting Small Signal Pulse Response

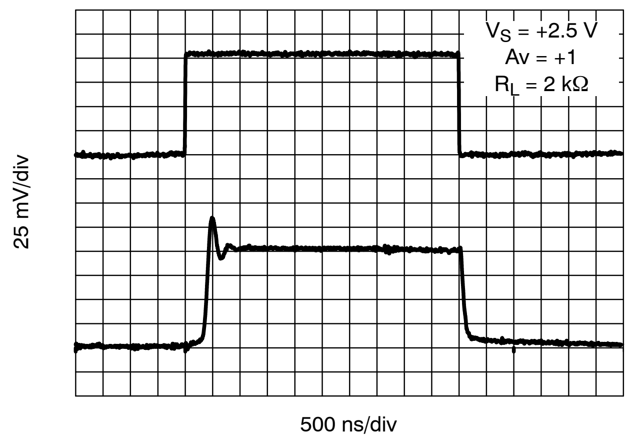


Figure 22. 2.5 V Non-Inverting Small Signal Pulse Response

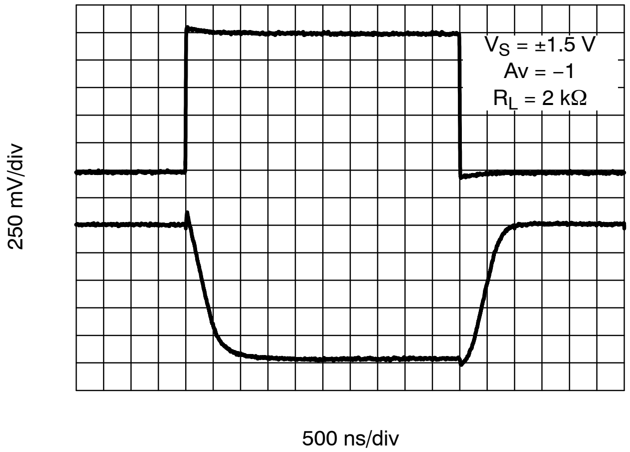


Figure 23. 3 V Inverting Large Signal Pulse Response

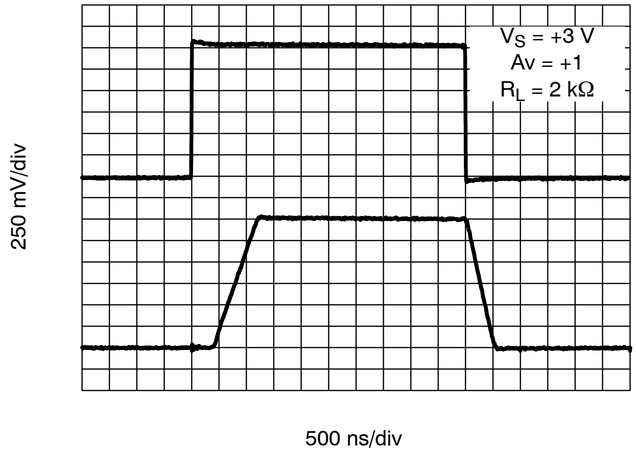


Figure 24. 3 V Non-Inverting Large Signal Pulse Response

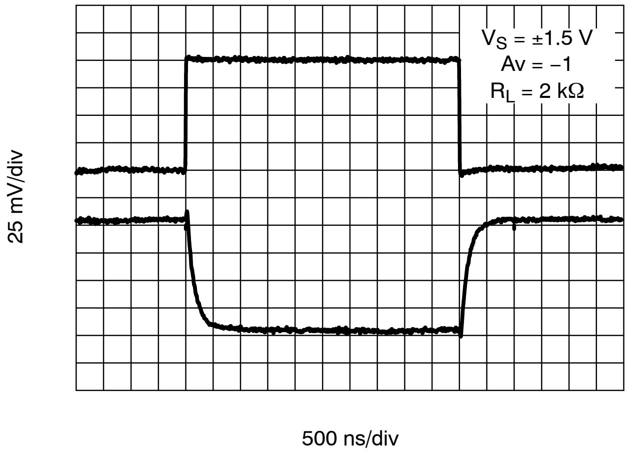


Figure 25. 3 V Inverting Small Signal Pulse Response

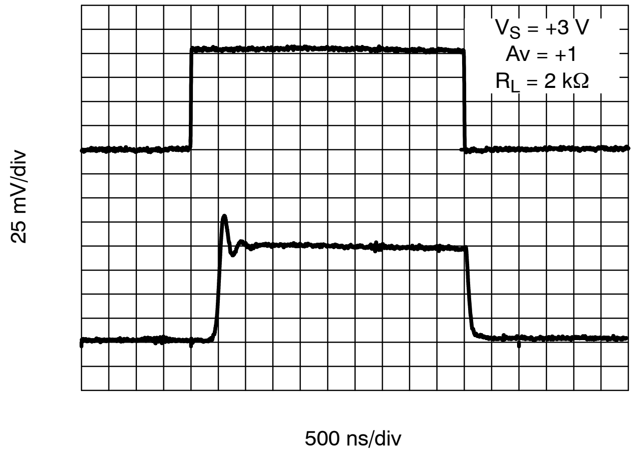


Figure 26. 3 V Non-Inverting Small Signal Pulse Response

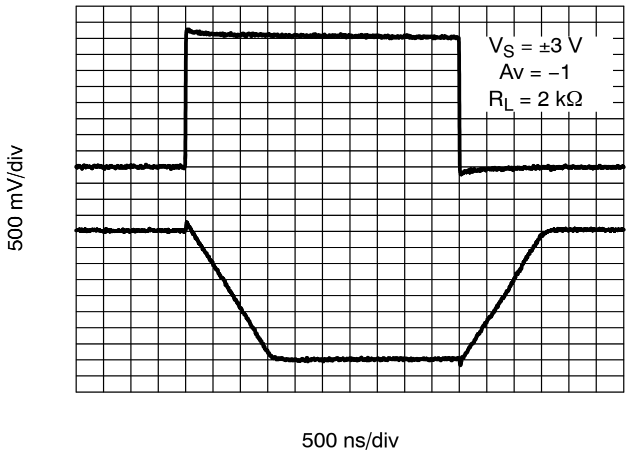


Figure 27. 6 V Inverting Large Signal Pulse Response

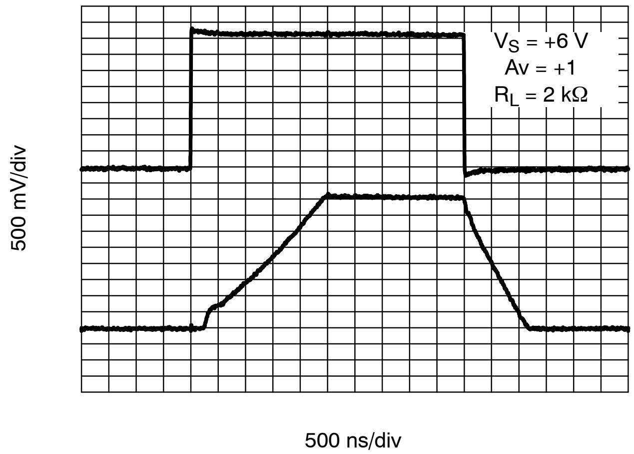


Figure 28. 6 V Non−Inverting Large Signal Pulse Response

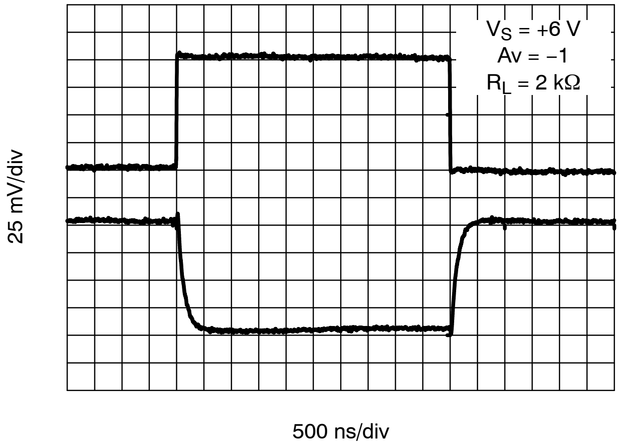


Figure 29. 6 V Inverting Small Signal Pulse Response

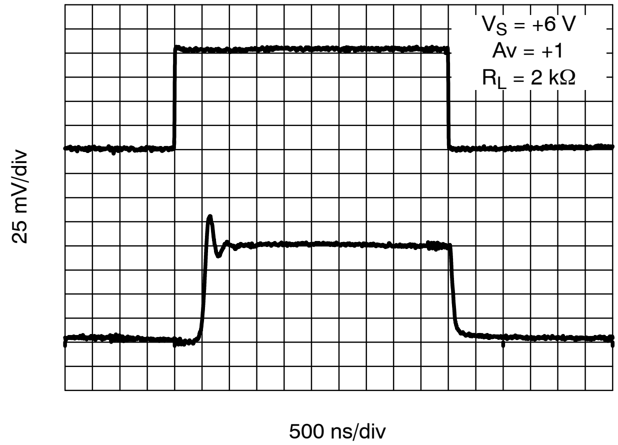
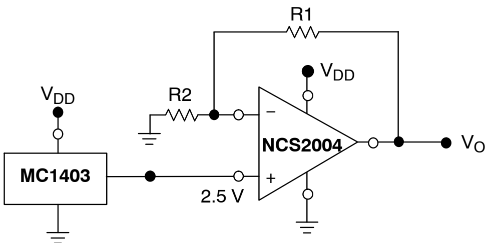


Figure 30. 6 V Non-Inverting Small Signal Pulse Response

APPLICATIONS



$$V_O = 2.5\,V\left(1 + \frac{R1}{R2}\right)$$

Figure 31. Voltage Reference

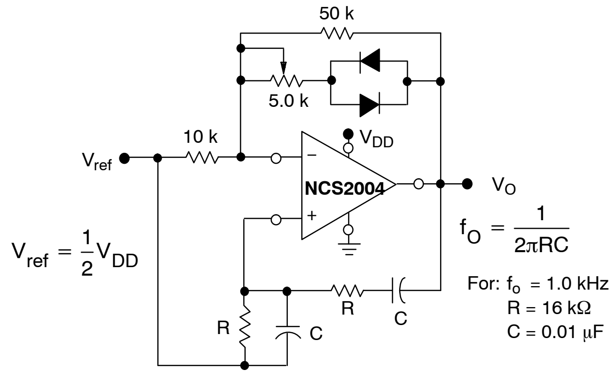
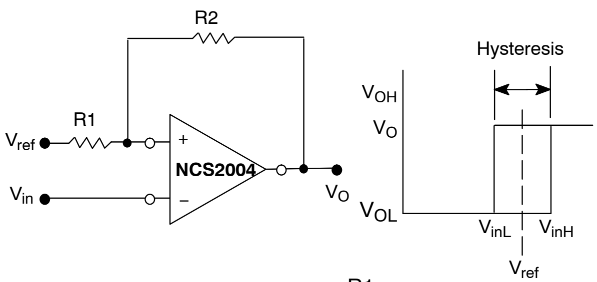


Figure 32. Wien Bridge Oscillator

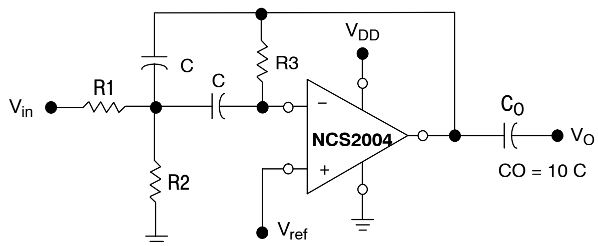


$$V_{in}L = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{in}H = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Figure 33. Comparator with Hysteresis



Given: f_o = center frequency
$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then : $R3 = \dfrac{Q}{\pi f_O C}$

$$R1 = \frac{R3}{2\,A(f_O)}$$

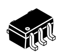
$$R2 = \frac{R1\,R3}{4Q^2\,R1 - R3}$$

For less than 10% error from operational amplifier, $((Q_O f_O)/BW) < 0.1$ where f_o and BW are expressed in Hz. If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Figure 34. Multiple Feedback Bandpass Filter

REVISION HISTORY

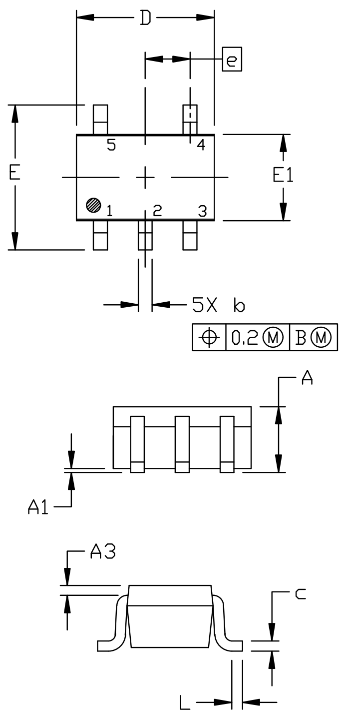
Revision	Description of Changes	Date
10	NCS2004AMUTAG, NCS2004SQ3T2G OPN's Marked as Discontinued + Rebranded the Data Sheet to **onsemi** format.	02/03/2026



SCALE 2:1

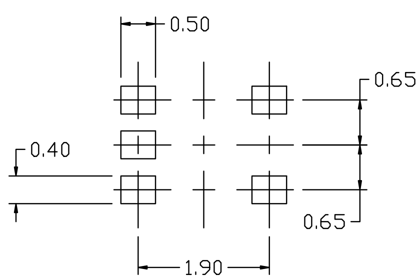
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

DATE 11 APR 2023



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

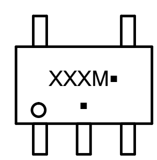
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

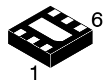
STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

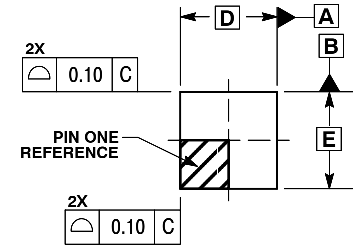
DOCUMENT NUMBER:	**98ASB42984B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SC−88A (SC−70−5/SOT−353)**	**PAGE 1 OF 1**

UDFN6 1.6x1.6, 0.5P
CASE 517AP
ISSUE O

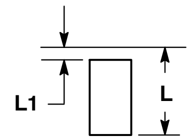
DATE 26 OCT 2007



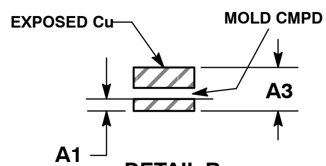
SCALE 4:1



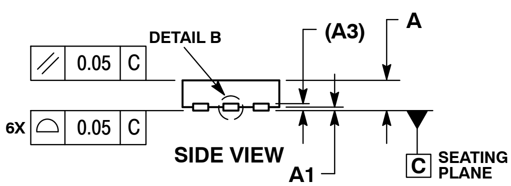
TOP VIEW



DETAIL A
OPTIONAL CONSTRUCTION



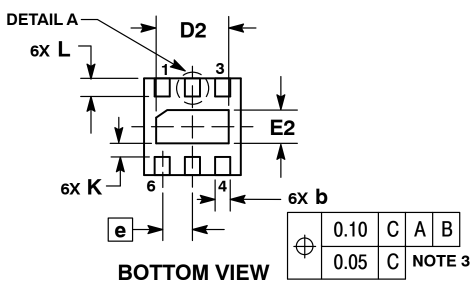
DETAIL B
OPTIONAL CONSTRUCTION



SIDE VIEW

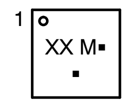
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
D2	1.10	1.30
E2	0.45	0.65
K	0.20	---
L	0.20	0.40
L1	0.00	0.15



BOTTOM VIEW

GENERIC MARKING DIAGRAM*

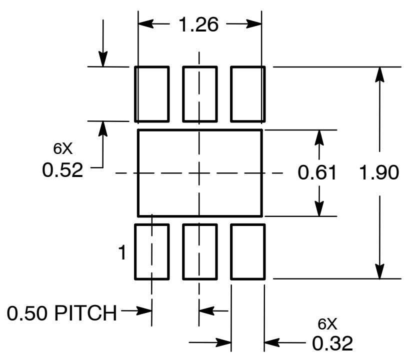


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

SOLDERMASK DEFINED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON25711D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	6 PIN UDFN, 1.6X1.6, 0.5P	PAGE 1 OF 1

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