Dual Interface RFID 64 Kb EEPROM Tag ISO 15693 RF and I²C Bus Compliant

N24RF64



SOIC 8
CASE 751BD



TSSOP8, 4.4x3
CASE 948AL

Description

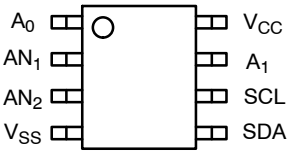
The N24RF64 is a RFID/NFC tag with a 64 Kb EEPROM device, offering both contactless and contact interface. In addition to the ISO/IEC 15693 radio frequency identification (RFID) interface protocol, the device features an I²C interface to communicate with a microcontroller. The I²C contact interface requires an external power supply.

The 64 Kb EEPROM array is internally organized as 2048 x 32 bits in RF mode and as 8192 x 8 bits when accessed from the I²C interface.

Features

- Contactless Transmission of Data
- ISO 15693 / ISO 18000−3 Mode1 Compliant
  - Vicinity Range Communication (up to 150 cm)
  - Air Interface Communication at 13.56 MHz (HF)
  - To tag: ASK Modulation with 1.65 Kbit/s or 26.48 Kbit/s Data Rate
  - From Tag: Load Modulation Using Manchester Coding with 423 kHz and 484 kHz Subcarriers in Low (6.6 Kbit/s) or high (26 Kbit/s) Data Rate Mode. Supports the 53 Kbit/s Data Rate with Fast Commands
- Read & Write 32−bit Block Mode
- Anti−collision Support
- Security:
  - 64−bit Unique Identifier (UID)
  - Multiple 32−bit Passwords and Lock Feature for Each User Memory Sector
- Supports Fast (400 kHz) and Fast−Plus (1 MHz) I²C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 4−Byte Page Write Buffer
- I²C Timeout
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- 2048 Blocks x 32 Bits (64 Sectors of 32 Blocks Each): RF Mode
- 8192 x 8 Bits I²C Mode
- 2,000,000 Program/Erase Cycles
- 200 Year Data Retention
- −40°C to +105°C Temperature Range
- SOIC, TSSOP 8−lead Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

PIN CONFIGURATION

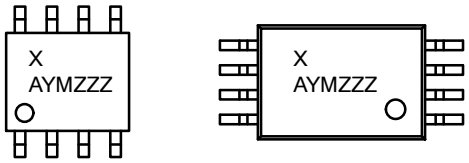


SOIC (W, X), TSSOP (Y)

PIN FUNCTION

Pin Name	Function
A0, A1	Device Address
SDA	Serial Data
SCL	Serial Clock
AN1, AN2	Antenna Coil
V_{CC}	Power Supply
V_{SS}	Ground

MARKING DIAGRAMS



X = Specific Device Code
A = Assembly Site Code
Y = Production Year (Last Digit)
M = Production Month Code
ZZZ = Last 3 Characters of Assembly Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 21 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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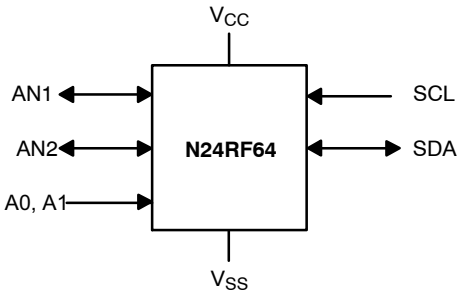


Figure 1. Functional Symbol

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Storage Temperature	−65 to +150	°C
Ambient Operating Temperature	-40 to +105	°C
Voltage on SCL, SDA, A0, A1 and V_{CC} pins with respect to Ground (Note 1)	−0.5 to 6.5	V
RF Input Voltage Peak to Peak Amplitude between AN1 and AN2, VSS pad floating	28	V
AC Voltage on AN1 or AN2 with respect to GND	-1 to 15	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. During transitions, the voltage undershoot on any pin should not exceed −1 V for more than 20 ns. Voltage overshoot on the SCL and SDA I^2C pins should not exceed the absolute maximum ratings, irrespective of VCC.

Table 2. RELIABILITY CHARACTERISTICS – EEPROM (Note 2)

Symbol	Parameter	Test Conditions	Max	Unit
N_{END}	Endurance	$T_A \le 25°C$, 1.8 V < V_{CC} < 5.5 V	2,000,000	Write Cycles (Note 3)
		$T_A = 85°C$, 1.8 V < V_{CC} < 5.5 V	800,000	
		$T_A = 105°C$, 1.8 V < V_{CC} < 5.5 V	300,000	
T_{DR}	Data Retention	$T_A = 25°C$	200	Year

2. Determined through qualification/characterization.
3. A Write Cycle refers to writing a Byte or a Page.

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Table 3. DC OPERATING CHARACTERISTICS – I²C MODE

(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +105°C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Max	Unit
ICCR	Supply Current (Read Mode)	Read, f_{SCL} = 400 kHz	V_{CC} = 1.8 V		0.15	mA
ICCR	Supply Current (Read Mode)		V_{CC} = 2.5 V		0.2	
			V_{CC} = 5.5 V		0.3	
ICCW	Supply Current (Write Mode)	Write Cycle			0.4	mA
ISB1	Standby Current	V_{IN} = GND or V_{CC}	No RF Field on antenna coil		10	μA
			Both V_{CC} Supply and RF Field on antenna coil		100	
IL	Input Leakage Current (Note 4)	V_{IN} = GND or V_{CC}		−2	2	μA
ILO	Output Leakage Current (SDA)	SDA = Hi−Z, V_{OUT} = GND or V_{CC}		−2	2	μA
VIL1	Input Low Voltage	V_{CC} ≥ 2.5 V		−0.5	0.3 V_{CC}	V
VIH1	Input High Voltage	V_{CC} ≥ 2.5 V		0.7 V_{CC}	V_{CC}+0.5	V
VIL2	Input Low Voltage	V_{CC} < 2.5 V		−0.5	0.25 V_{CC}	V
VIH2	Input High Voltage	V_{CC} < 2.5 V		0.75 V_{CC}	V_{CC}+0.5	V
VOL1	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
VOL2	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 2.1 mA			0.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. When not driven, the A0 and A1 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong as long as the input level is below the trip point of the CMOS input buffer (~0.5 x V_{CC}); therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer, the strong pull−down is disabled.

Table 4. PIN IMPEDANCE CHARACTERISTICS

Symbol	Parameter	Conditions	Max	Unit
C_{IN} (Note 5)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 5)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

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Table 5. AC CHARACTERISTICS – I²C MODE (Note 6)
(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +105°C, unless otherwise specified)

Symbol	Parameter	I²C Fast		I²C Fast Plus		Unit
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency	25	400	25	1000	kHz
t_{LOW}	Low Period of SCL Clock	1.3	20000	0.45	20000	μs
t_{HIGH}	High Period of SCL Clock	0.6	20000	0.40	20000	μs
$t_{SU:STA}$	START Condition Setup Time	0.6		0.25		μs
$t_{HD:STA}$	START Condition Hold Time	0.6	20000	0.25	20000	μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	100		50		ns
t_R (Note 7)	SDA and SCL Rise Time	20	300	20	100	ns
t_F (Note 7)	SDA and SCL Fall Time	20	300	20	100	ns
$t_{SU:STO}$	STOP Condition Setup Time	0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		0.9		0.4	μs
t_{DH}	Data Out Hold Time	100		50		ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50	ns
t_{WR}	Write Cycle Time		5		5	ms
t_{PU} (Notes 7, 8)	Power−up to Ready Mode		1		1	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Test conditions according to “AC Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. AC TEST CONDITIONS

Parameter	Condition
Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_{OL} = 3 mA (V_{CC} ≥ 2.5 V); I_{OL} = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

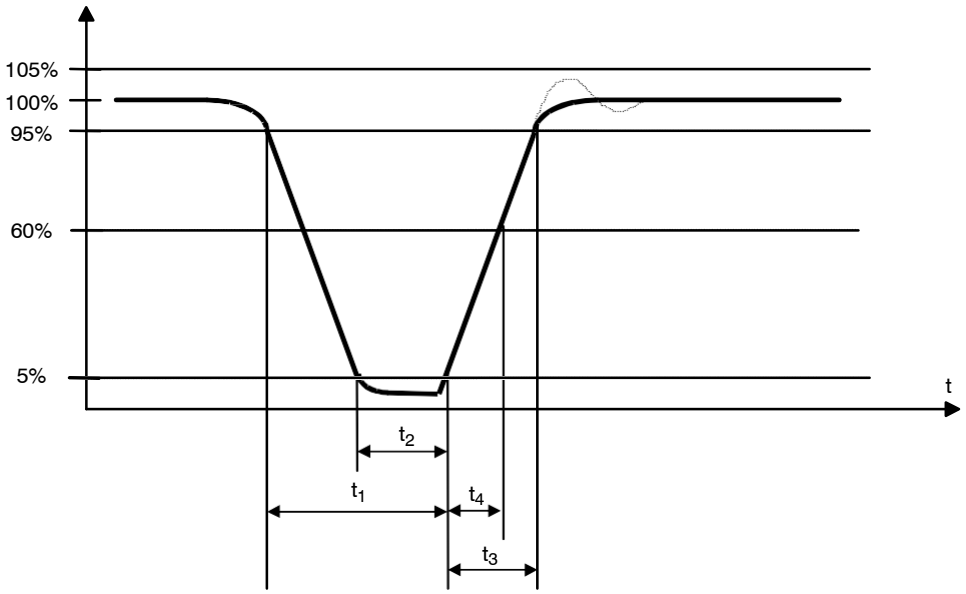
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Table 7. RF CHARACTERISTICS (Notes 9, 10) (T_A = −40°C to +105°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{CC}	External RF signal frequency		13.553	13.56	13.567	MHz
H_ISO	Operating field		150		5000	mA/m
MI_Carrier (10%)	10% Carrier Modulation Index MI = (a−b) / (a+b)	150 mA/m < H_ISO < 1000 mA/m	10		30	%
		H_ISO > 1000 mA/m	15		30	
$t_{1:10\%}$	10% Fall and Low Time	t1 = t2	6.0		9.44	us
$t_{2:10\%}$	10% Minimum Low Time	t1 = 9.44 μs	4.5		t1	us
$t_{3:10\%}$	10% Rise Time	t1 = 9.44 μs	0		4.5	us
MI_Carrier (100%)	100% Carrier Modulation Index	MI = (a−b) / (a+b)	95		100	%
$t_{1:100\%}$	100% Fall and Low Time	t1 = t2	6.0		9.44	μs
$t_{2:100\%}$	100% Minimum Pulse Width Low Time	t1 = 9.44 μs	2.1		t1	μs
$t_{3:100\%}$	100% Rise Time	t1 = 9.44 μs	0		3	μs
$t_{4:100\%}$	100% Rise Time to 60% of Amplitude		0		0.8	μs
$t_{MIN\ C-D}$	Minimum delay from Carrier generation to first Data	150 mA/m < H_ISO < 1000 mA/m			1	ms
		H_ISO > 1000 mA/m			2	
f_{SH}	Subcarrier Frequency High	fCC/32		423.75		kHz
f_{SL}	Subcarrier Frequency Low	fCC/28		484.28		kHz
t_{RESP}	N24RF64 Tag Response Time	4352/FS	318.4	320.9	323.5	μs
t_{WRF}	RF Write Time (with internal Verify)	78080/FS	5.753	5.758	5.763	ms
C_{TUN}	Internal Tuning Capacitor (TSSOP−8) (Note 11)	f = 13.56 MHz; Vac0 − Vac1 = 1 Vp−p		26		pF
V_{MAX-1}	RF Input Voltage between AN1 and AN2 (peak to peak), V_{SS} pad floating (Note 11)				22	V
V_{MAX-2}	AC voltage on AN1 or AN2 with respect to GND (Note 11)		−1		11	V
V_{MIN-1}	RF Input Voltage between AN1 and AN2 (peak to peak), VSS pad floating (Note 11)			4		V
V_{MIN-2}	AC voltage on AN1 or AN2 with respect to GND (Note 11)			2.1		V
V_{BACK}	Backscattered Level (ISO Test)	ISO10373−7	10			mV
T_{RF-OFF}	RF Off Time	Chip reset	2			ms

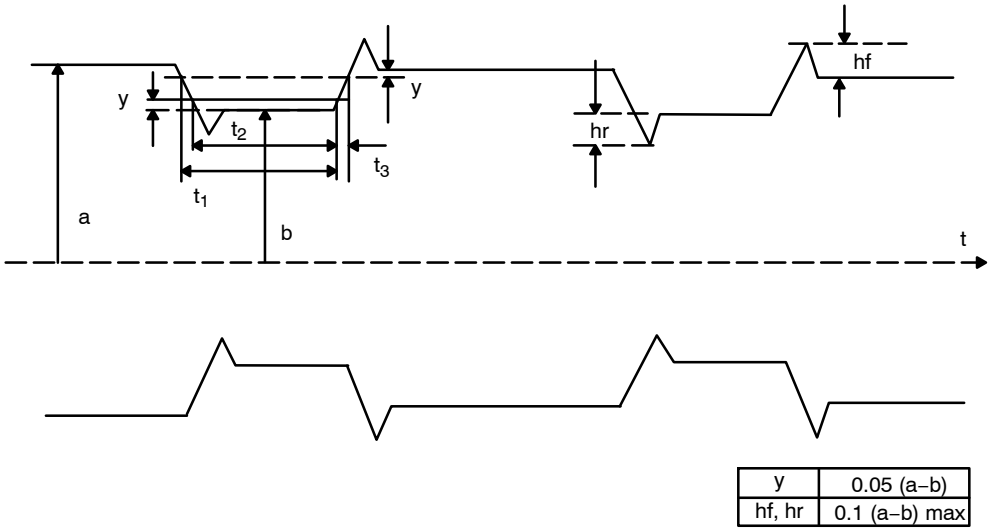
9. Characterized only.
10. All measurements performed on an antenna with the following characteristics:
    ·External size: 72 mm x 42 mm
    ·Number of turns: 7
    ·Antenna is printed on the PCB plated with 35 μm of Cooper
    ·Track width: 0.8 mm
    ·Space: 0.5 mm
    ·Coil: 5 μH
11. Characterized at room temperature only.

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The clock recovery must be operational after t_4 max.

Figure 2. 100% Modulation Waveform



y	0.05 (a−b)
hf, hr	0.1 (a−b) max

Figure 3. 10% Modulation Waveform

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Power−On Reset (POR)

Each N24RF64 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the

POR trigger level. This bi−directional POR behavior protects the device against ‘brown−out’ failure following a temporary loss of power.

Pin Description

- SCL: The Serial Clock input pin accepts the clock signal generated by the Master
- SDA: The Serial Data I/O pin accepts input data and delivers output data. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL
- A_0, A_1: The Address inputs set the device address that must be matched by the corresponding Slave address bits. The Address inputs are hard−wired HIGH or LOW allowing for up to four devices to be used (cascaded) on the same bus. When left floating, these pins are pulled LOW internally
- AN_1, AN_2: These inputs are used to connect the device to an external antenna. The coil is used to power and access the device through the ISO 15693 and ISO 18000−3 mode 1 RF protocols

Functional Description

The N24RF64 is a dual interface RFID/NFC tag with 64 Kb EEPROM.

The device follows the ISO 15693 and ISO 18000−3 mode 1 standard for the radio frequency power and signal interface via the 13.56 MHz carrier. When connected to an antenna coil, no external power supply is required, as the operating power is derived from the RF energy The communication from the RF Reader to the N24RF64 tag takes place using the ASK modulation with a 1.65 Kb/s data rate using the 1/256 pulse coding or a data rate of 26.48 Kb/s using the 1/4 pulse coding. The communication from the EEPROM tag to the RF reader takes place via load modulation using Manchester coding with 423 kHz and 484 kHz subcarrier frequencies at 6.62 Kb/s or 26.48 Kb/s data rate. The device supports also the 53 Kb/s fast mode.

The N24RF64 supports the Inter−Integrated Circuit (I^2C) Bus protocol. The protocol relies on the use of a Master device, which provides the clock and directs bus traffic and Slave devices which execute requests. The N24RF64 operates as a Slave device with a 4−bit device identifier code (1010b) according to the I^2C standard definition.

Memory Organization

In the RF mode, the user memory area is organized into 64 sectors of 32 blocks each for a total of 2048 blocks x 32 bits. The memory access from the I^2C interface is organized as 8192 x 8 bits, divided into 64 sectors of 128 bytes each. The user and system memory organization is shown in Figure 4.

Each memory sector can be individually read and/or write protected using a specific password. The N24RF64 provides four 32−bit blocks to store three RF password and one I^2C password codes.

In RF mode, the read and write access is done by 32−bit block. Read and Write access is controlled by a Sector Security Status (SSS) byte which includes 5 significant bits: Sector Lock bit, two Read / Write protection bits and two Password Control bits.

In I^2C mode, a sector has 128 bytes that can be individually accessed for Read and Write. Each sector can be protected against write operations using the I^2C−Write_Lock bit from the 16−bit block area.

The N24RF64 features a 64−bit block to store the 64−bit Unique Identifier (UID) per the ISO 15963 requirements. The UID value is written by **onsemi** during manufacturing and it is used during the anti−collision sequence.

The system memory area also includes the application family identifier (AFI) and a data storage family identifier (DSFID) used in the anti−collision algorithm.

The access to the user memory area requires the A2 bit from the Slave address byte set to “0” (Figure 5). All system memory blocks are accessed with A2 bit set to “1”.

Unique Identifier

The N24RF is programed at the factory with a 64−bit unique identifier. The UID conforms to IS0 15693 / ISO 18000 and is read−only. The UID is comprised of:

- Eight MSBs with a value of 0xE0
- IC manufacturer code for **onsemi** 0x67
- Unique 48 bit serial number

MSB		
63 56	55 48	47 0
0xE0	0x67	Unique serial number

Table 8.

I^2C Byte Address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
A2=1	0	SSS 3 (00h)	SSS 2 (00h)	SSS 1 (00h)	SSS 0 (00h)
A2=1	4	SSS 7 (00h)	SSS 6 (00h)	SSS 5 (00h)	SSS 4 (00h)
A2=1	…	…	…	…	…
A2=1	56	SSS 59 (00h)	SSS 58 (00h)	SSS 57 (00h)	SSS 56 (00h)
A2=1	60	SSS 63 (00h)	SSS 62 (00h)	SSS 61 (00h)	SSS 60 (00h)
A2=1	2048	I^2C Write Lock [31:24] (00h)	I^2C Write Lock [23:16] (00h)	I^2C Write Lock [15:8] (00h)	I^2C Write Lock [7:0] (00h)

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Table 8. (continued)

I²C Byte Address		Bits [31:24]	Bits [23:16]	Bits [15:8]	Bits [7:0]
A2=1	2052	I²C Write Lock [63:56] (00h)	I²C Write Lock [55:48] (00h)	I²C Write Lock [47:40] (00h)	I²C Write Lock [39:32] (00h)
A2=1	2304	I²C password (0000 0000h)			
A2=1	2308	RF password 1 (0000 0000h)			
A2=1	2312	RF password 2 (0000 0000h)			
A2=1	2316	RF password 3 (0000 0000h)			
A2=1	2320	DSFID (FFh)	AFI (00h)	ON reserved	ON reserved
A2=1	2324	UID	UID	UID	UID
A2=1	2328	UID (E0h)	UID (67h)	UID	UID
A2=1	2332	Mem Size (03 07FFh)			IC Ref (6Ah)

Sector	Area	Sector Security Status
0	1 Kbit EEPROM Sector	5 bits
1	1 Kbit EEPROM Sector	5 bits
2	1 Kbit EEPROM Sector	5 bits
3	1 Kbit EEPROM Sector	5 bits
…		
60	1 Kbit EEPROM Sector	5 bits
61	1 Kbit EEPROM Sector	5 bits
62	1 Kbit EEPROM Sector	5 bits
63	1 Kbit EEPROM Sector	5 bits
	I²C Password	System
	RF Password 1	System
	RFPassword 2	System
	RF Password 3	System
	8−bit DSFID	System
	8−bit AFI	System
	64−bit UID	System
	64−bit I²C Write Lock bits	System
	320−bit SSS	System

Figure 4. Memory Organization

Sector Security Status

The five Sector Security Status bits are organized as follows:

b4	b3	b2	b1	b0
Password control bits		Read/Write Protection bits		Sector Lock

The Sector Lock bit enables (1) or disables (0) the sector protection. The password control bits determine whether and which password protects the sector. The read/write protection bits determine whether reading and/or writing the sector is permitted. (See table below for combinations.)

Sector Lock (b0)	b2, b1	Sector Access When Password Presented		Sector Access When Password Not Presented	
0	xx	Read	Write	Read	Write
1	00	Read	Write	Read	No Write
1	01	Read	Write	Read	Write
1	10	Read	Write	No Read	No Write
1	11	Read	No Write	No Read	No Write

b4	b0
b4, b3	Password
00	Sector not protected by password
01	Sector protected by Password 1
10	Sector protected by Password 2
11	Sector protected by Password 3

I²C Bus Protocol

The 2−wire I²C bus consists of two lines, SCL and SDA, connected to the V_{CC} supply via pull−up resistors. The Master provides the clock to the SCL line, and either the Master or the Slaves drive the SDA line. A ‘0’ is transmitted by pulling a line LOW and a ‘1’ by letting it stay HIGH. Data transfer may be initiated only when the bus is not busy (see AC Characteristics). During data transfer, SDA must remain stable while SCL is HIGH.

START/STOP Condition

An SDA transition while SCL is HIGH creates a START or STOP condition (Figure 5). The START consists of a HIGH to LOW SDA transition, while SCL is HIGH. Absent the START, a Slave will not respond to the Master. The STOP completes all commands, and consists of a LOW to HIGH SDA transition, while SCL is HIGH.

Device Addressing

The Master addresses a Slave by creating a START condition and then broadcasting an 8−bit Slave address. For the N24RF64, the first four bits of the Slave address are set to 1010. The A2 bit is used to control the access to the user or system memory area. The A1 and A0 bits must match the logic state of the similarly named input pins. The R/$\overline{W}$ bit

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tells the Slave whether the Master intends to read (1) or write (0) data (Figure 6).

Acknowledge

During the 9th clock cycle following every byte sent to the bus, the transmitter releases the SDA line, allowing the receiver to respond. The receiver then either acknowledges (ACK) by pulling SDA LOW, or does not acknowledge (NoACK) by letting SDA stay HIGH (Figure 7). Bus timing is illustrated in Figure 8.

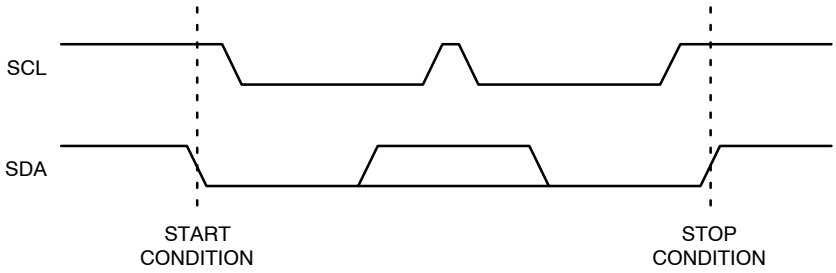
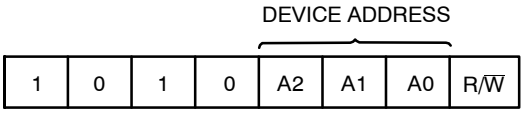


Figure 5. Slave Address Bits



NOTE: A2 bit is used to control the memory addressing: A2 = 0: User memory area; A2 = 1: System memory area
A1, A0 bits must match the logic state of the similarly named pins.

Figure 6. Slave Address Bits

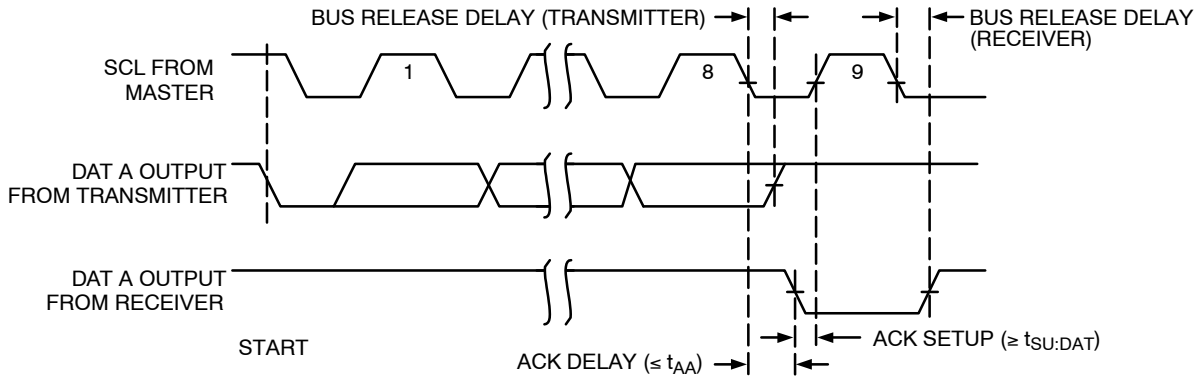


Figure 7. Acknowledge Timing

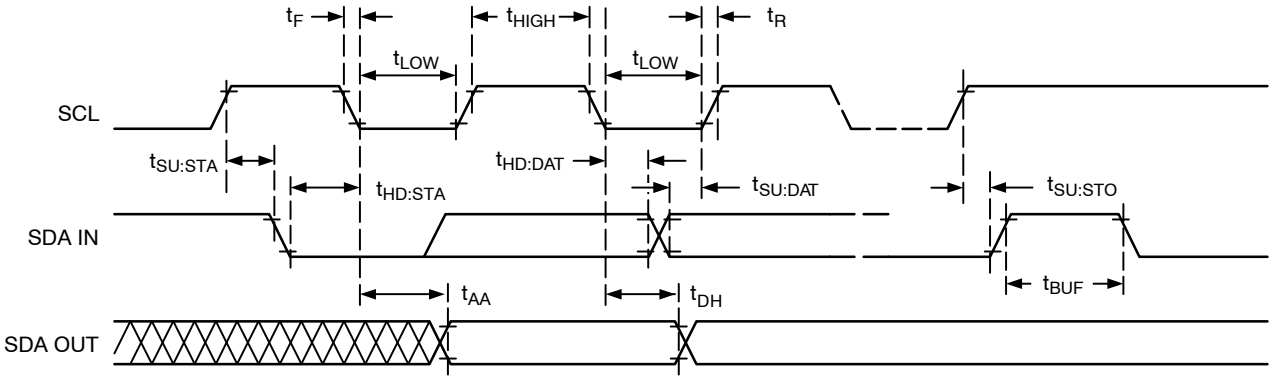


Figure 8. Bus Timing

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WRITE OPERATIONS

Byte Write

To write data to memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to '0'. The Master then sends two address bytes and a data byte and concludes the session by creating a STOP condition on the bus. The Slave responds with ACK after every byte sent by the Master (Figure 9). The STOP starts the internal Write cycle, and while this operation is in progress (t_{WR}), the SDA output is tri−stated and the Slave does not acknowledge the Master (Figure 10).

Page Write

The Byte Write operation can be expanded to Page Write, by sending more than one data byte to the Slave before issuing the STOP condition (Figure 11). Up to 4 distinct data bytes can be loaded into the internal Page Write Buffer starting at the address provided by the Master. The page address is latched, and as long as the Master keeps sending data, the internal byte address is incremented up to the end of page, where it then wraps around (within the page). New data can therefore replace data loaded earlier. Following the STOP, data loaded during the Page Write session will be written to memory in a single internal Write cycle (t_{WR}).

Acknowledge Polling

As soon (and as long) as internal Write is in progress, the Slave will not acknowledge the Master. This feature enables the Master to immediately follow−up with a new Read or Write request, rather than wait for the maximum specified Write time (t_{WR}) to elapse. Upon receiving a NoACK response from the Slave, the Master simply repeats the request until the Slave responds with ACK.

The remainder of the instruction is identical to a normal Page Write.

Delivery State

The N24RF64 is shipped erased, i.e., all bytes are FFh.

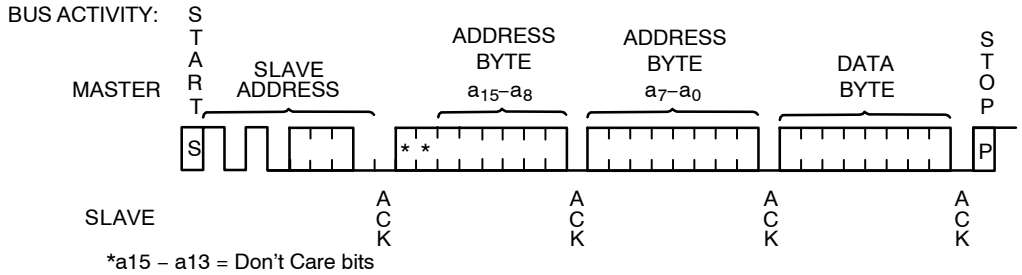


Figure 9. Byte Write Sequence

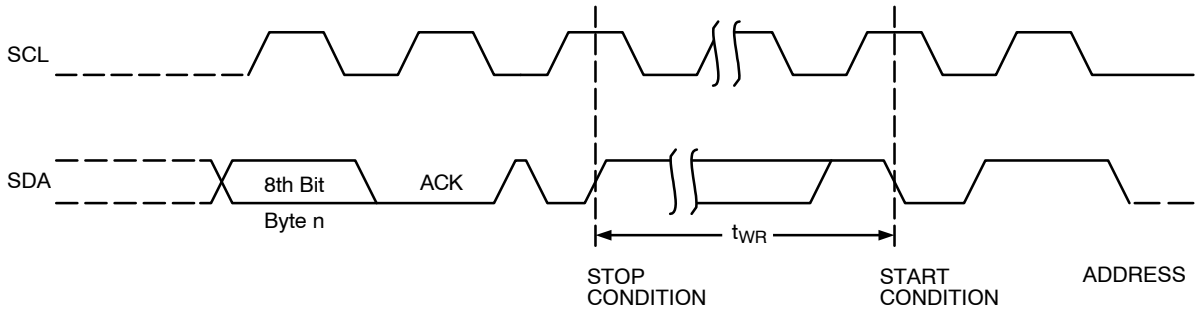


Figure 10. Write Cycle Timing

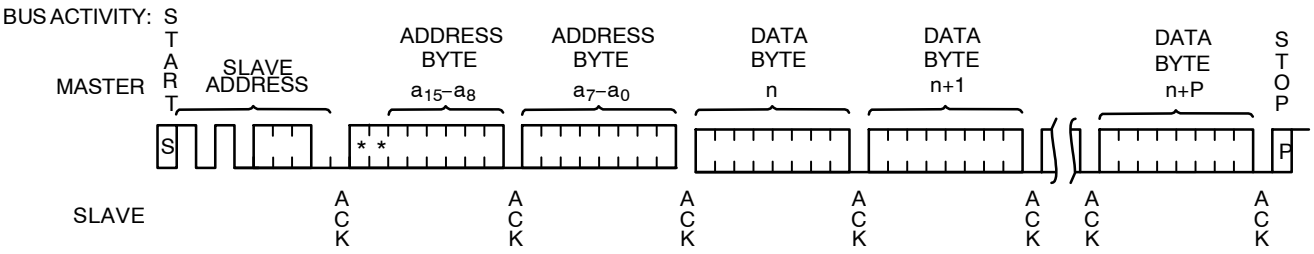


Figure 11. Page Write Sequence

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READ OPERATIONS

Immediate Read

To read data from memory, the Master creates a START condition on the bus and then broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK and starts shifting out data residing at the current address. After receiving the data, the Master responds with NoACK and terminates the session by creating a STOP condition on the bus (Figure 12). The Slave then returns to Standby mode.

Selective Read

To read data residing at a specific address, the selected address must first be loaded into the internal address register. This is done by starting a Byte Write sequence, whereby the Master creates a START condition, then broadcasts a Slave address with the R/$\overline{W}$ bit set to '0' and then sends two address bytes to the Slave. Rather than completing the Byte Write sequence by sending data, the Master then creates a START condition and broadcasts a Slave address with the R/$\overline{W}$ bit set to '1'. The Slave responds with ACK after every byte sent by the Master and then sends out data residing at the selected address. After receiving the data, the Master responds with NoACK and then terminates the session by creating a STOP condition on the bus (Figure 13).

Sequential Read

If, after receiving data sent by the Slave, the Master responds with ACK, then the Slave will continue transmitting until the Master responds with NoACK followed by STOP (Figure 14). During Sequential Read the internal byte address is automatically incremented up to the end of memory, where it then wraps around to the beginning of memory.

I^2C SECURITY

In the I^2C mode it is possible to protect each memory sector from user area against write operations. The sector write access is controlled using the 64−bit I2C_Write_Lock bit area and the 32−bit I^2C password. There are two commands to control the I^2C password: I^2C Present Password and I^2C Write Password.

I^2C Present Password

The I^2C Present Password command is used to modify the write access rights of the sectors protected by the I^2C Write−Lock bits, including the password itself. N24RF64 will allow this only if the correct password is presented, via I^2C bus. If the password is correct, the access rights remain activated until a new I^2C Present Password command is received, or the device is powered off.

Following a Start condition, the master sends a write instruction with the slave address with the Read/Write bit equal to 0 and the A2 bit equal to 1 (system memory). The device acknowledges this and expects two I^2C password address bytes, 09h and 00h. The device responds to each address byte with an ACK. The device then expects the 4 password data bytes, the validation code, 09h, and a resend of the 4 password data bytes. The most significant byte of the password is sent first, followed by the least significant bytes.

The 32−bit password must be sent twice to prevent any data corruption during the sequence. If the two 32−bit passwords sent are not exactly the same, the command will not be accepted.

When the bus master generates a Stop condition immediately after the Ack bit, an internal delay equivalent to the write cycle time is triggered. A Stop condition at any other time does not trigger the internal delay. During that delay, the N24RF64 compares the 32 received data bits with the 32 bits of the stored I^2C password.

If the values match, the write access rights to all protected sectors are modified after the internal delay. If the values do not match, the protected sectors remains protected.

During the internal delay, the SDA output is tri−stated and the Slave does not acknowledge the Master.

I^2C Write Password

The I^2C Write Password command is used to overwrite the 32−bit I^2C password block. This command is used in I^2C mode to update the I^2C password value. It cannot be used to modify any of the RF passwords. After the write cycle, the new I^2C password value is automatically activated. The I^2C password value can only be modified after issuing a valid I^2C Present Password command.

Following a Start condition, the master sends a write instruction with the slave address with the Read/Write bit equal to 0 and the A2 bit equal to 1 (system memory). The device acknowledges this and expects two I^2C password address bytes, 09h and 00h. The device responds to each address byte with an ACK. The device then expects the 4 password data bytes, the validation code, 07h, and a resend of the 4 password data bytes. The most significant byte of the password is sent first, followed by the least significant bytes. N24RF64 is shipped with the default I^2C password 00000000h. By default, the password is activated.

The 32−bit password must be sent twice to prevent any data corruption during the sequence. If the two 32−bit passwords sent are not exactly the same, the command will not be accepted.

When the bus master generates a Stop condition immediately after the Ack bit, the internal write cycle is triggered. A Stop condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the SDA output is tri−stated and the Slave does not acknowledge the Master.

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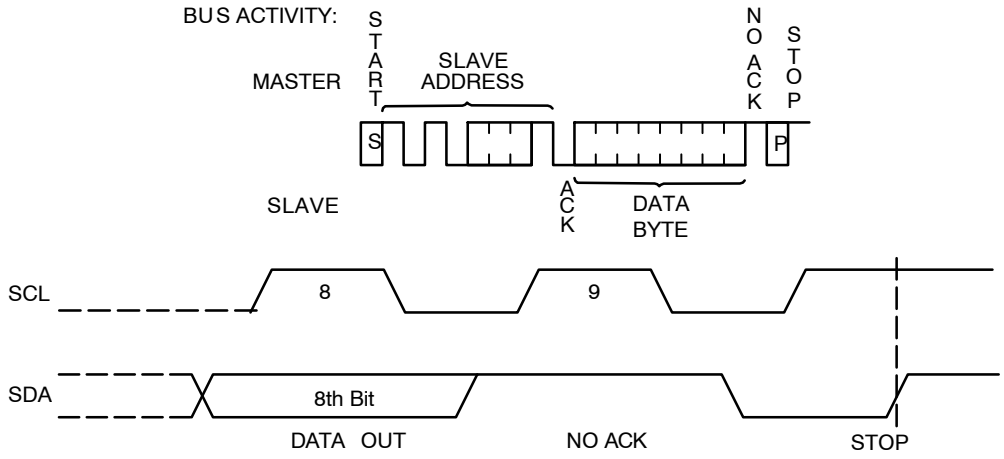


Figure 12. Immediate Read Sequence and Timing

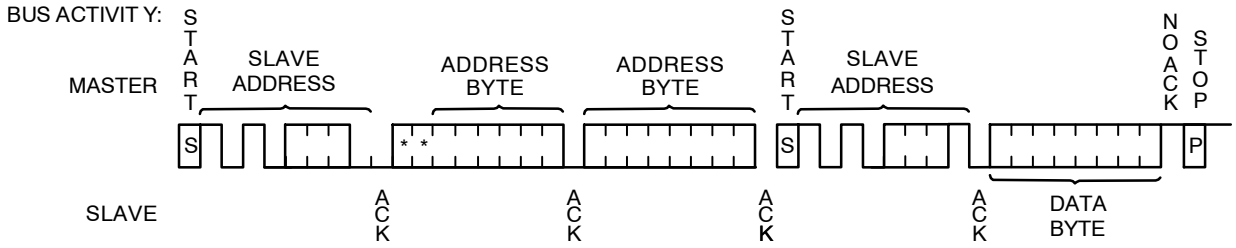


Figure 13. Selective Read Sequence

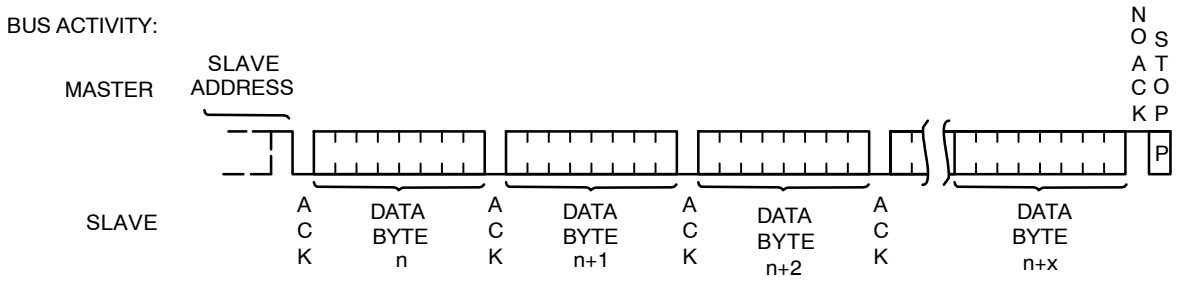


Figure 14. Sequential Read Sequence

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RF MODE OPERATION

The communication protocol between the RF Reader and the N24RF64 tag is based on the RTF technique (Reader Talks First):

- Activation of the N24RF64 memory tag by the electromagnetic field of the RF Reader
- Transmission of a command / request by the RF Reader
- Transmission of a response by the memory tag

The memory tag operates continuously under the electromagnetic field (H) generated by the RF Reader. The transmission of data and power is based on inductive coupling using the carrier frequency (f_C) as 13.56 MHz ±7 kHz per ISO 15693 standard.

Each request from the Reader and each response from the N24RF64 tag are organized in a frame, delimited by a start of frame (SOF) and an end of frame (EOF).

Communication from RF Reader to N24RF64 Tag

The communication between the RF Reader and memory tag uses the ASK (Amplitude Shift Keying) modulation. The received signal is demodulated by the ASK demodulator of the memory tag. The N24RF64 supports both 100% and 10% modulation index. The Reader selects which index is used. Figure 14 shows the 100% ASK modulation waveform.

The data transmission uses pulse position coding described in the ISO 15693: 1 out of 256 data coding with a resulting data rate of 1.65 Kb/s or 1 out of 4 data coding with a data rate of 26.48 Kb/s.

The request from RF Reader to the memory tag consists of: a request SOF, flags, command code, parameters, data, 2−byte CRC, a request EOF. The SOF defines the data coding mode that will be used by the RF Reader for the following command. Figure 15 shows a SOF to select 1 out of 256 data coding and Figure 16 illustrates the SOF to select

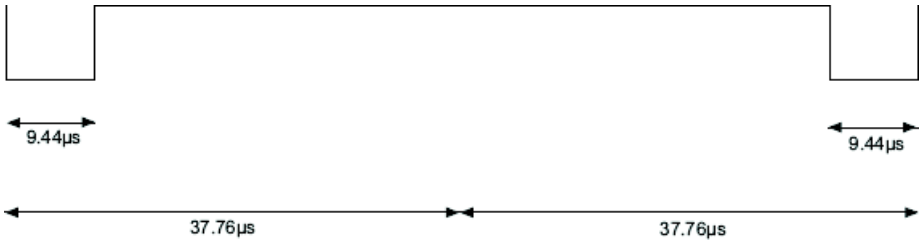


Figure 15. Request SOF for 1 out of 256 Data Coding

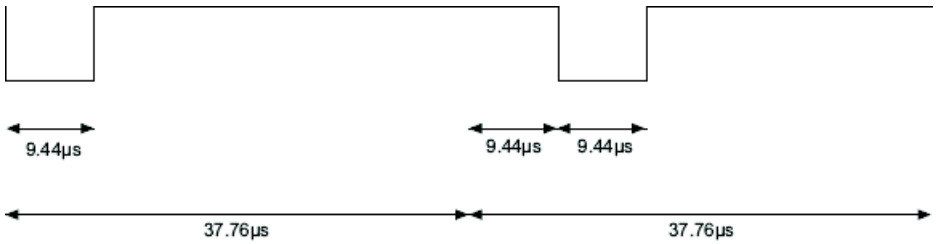


Figure 16. Request SOF for 1 out of 4 Data Coding

Communication from N24RF64 Tag to RF Reader

The communication between the N24RF64 memory tag and the RF reader uses the load modulation with Manchester data coding. Via the inductive coupling, the carrier is loaded to generate a subcarrier with fs frequency. The device supports the one−subcarrier with 423.75 kHz (fc/32) frequency and two−subcarrier response with 423.75 kHz (fc/32) and 484.28 kHz (fc/28) frequencies. The one−subcarrier or two−subcarrier response format is selected by the RF Reader.

The N24RF64 responds using the low or high data rate for standard commands. The fast commands use a data rate multiplied by two. The data rate is selected by the RF Reader through the protocol header. Table 9 shows the data rates supported by the memory tag using one carrier and two carriers format.

Table 9. TAG RESPONSE DATA RATES

Command Type	Data Rate	One−Subcarrier	Two−Subcarrier
Standard Commands	Low	6.62 Kb/s (fc/2028)	6.67 Kb/s (fc/2032)
Fast Commands		13.24 Kb/s (fc/1024)	N/A
Standard Commands	High	26.48 Kb/s (fc/512)	26.69 Kb/s (fc/508)
Fast Commands		52.97 Kb/s (fc/256)	N/A

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The N24RF64 supports the following commands in RF mode:

Table 10. RF COMMAND DESCRIPTION

Nr	Command Name	Command Description
1	Inventory	Perform the anticollision sequence
2	Stay quiet	Put the N24RF64 in quiet mode, where it does not respond to any inventory command
3	Read single block	Output the 32 bits of the selected block and its locking status
4	Write single block	Write the 32−bit value in the selected block, if it is not locked
5	Read multiple blocks	Read the selected blocks and send back their value
6	Select	Select the N24RF64; after this command the device processes all Read/Write commands with Select_flag set
7	Reset to ready	Enter the ready state
8	Write AFI	Write the 8−bit value in the AFI register
9	Lock AFI	Used to lock the AFI register
10	Write DSFID	Write the 8−bit value in the DSFID register
11	Lock DSFID	Lock the DSFID register.
12	Get system info	Provide the system information value
13	Get multiple block security status	Send the security status of the selected block
14	Write sector password	Write the 32−bit selected password
15	Lock sector	Write the sector security status bits of the selected sector
16	Present sector password	Enables the user to present a password to unprotect the user blocks linked to this password
17	Fast read single block	Output the 32 bits of the selected block and its locking status
18	Fast inventory initiated	Perform the anticollision sequence triggered by the Initiate command
19	Fast initiate	Trigger the tag response to the Inventory initiated sequence
20	Fast read multiple blocks	Read the selected blocks and send back their value
21	Inventory initiated	Perform the anticollision sequence triggered by the Initiate command
22	Initiate	Trigger the tag response to the Inventory initiated sequence

Table 11. RF COMMAND FORMAT

Nr. Crt.	Function	SOF	Flags	Command	IC Mfg. code	UID	Optional AFI	Number	Data	CRC16	EOF
1	Inventory	x	8 bits	01h	–	–	8 bits	8 bits (Note 13)	0 to 8 bytes (Note 16)	16 bits	x
2	Stay Quiet	x	8 bits	02h	–	8 bytes	–	–	–	16 bits	x
3	Read single block	x	8 bits	20h	–	8 bytes	–	16 bits (Note 14)	–	16 bits	x
4	Write single block	x	8 bits	21H	–	8 bytes (Note 12)	–	16 bits (Note 14)	32 bits	16 bits	x
5	Read multiple blocks	x	8 bits	23H	–	8 bytes (Note 12)	–	16 bits (Note 14)	8 bits (Note 17)	16 bits	x
6	Select	x	8 bits	25h	–	8 bytes	–	–	–	16 bits	x

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Table 11. RF COMMAND FORMAT (continued)

Nr. Crt.	Function	SOF	Flags	Command	IC Mfg. code	UID	Optional AFI	Number	Data	CRC16	EOF
7	Reset to ready	x	8 bits	26h	–	8 bytes (Note 12)	–	–	–	16 bits	x
8	Write AFI	x	8 bits	27h	–	8 bytes (Note 12)	–	–	8 bits	16 bits	x
9	Lock AFI	x	8 bits	28h	–	8 bytes (Note 12)	–	–	–	16 bits	x
10	Write DSFID	x	8 bits	29h	–	8 bytes (Note 12)	–	–	8 bits	16 bits	x
11	Lock DSFID	x	8 bits	2Ah	–	8 bytes (Note 12)	–	–	–	16 bits	x
12	GET System Info	x	8 bits	2Bh	–	8 bytes (Note 12)	–	–	–	16 bits	x
13	Get multiple block security status	x	8 bits	2Ch	–	8 bytes (Note 12)	–	16 bits (Note 14)	16 bits (Note 17)	16 bits	x
14	Write sector password	x	8 bits	B1h	67h	8 bytes (Note 12)	–	8 bits (Note 15)	32 bits	16 bits	x
15	Lock sector	x	8 bits	B2h	67h	8 bytes (Note 12)	–	16 bits (Note 14)	8 bits	16 bits	x
16	Present sector password	x	8 bits	B3h	67h	8 bytes (Note 12)	–	8 bits (Note 15)	32 bits	16 bits	x
17	Fast read single Block	x	8 bits	C0h	67h	8 bytes (Note 12)	–	16 bits (Note 14)	–	16 bits	x
18	Fast Inventory Initiated	x	8 bits	C1h	67h	–	8 bits	8 bits (Note 13)	0 to 8 bytes (Note 16)	16 bits	x
19	Fast Initiate	x	8 bits	C2h	67h	–	–	–	–	16 bits	x
20	Fast read multiple Blocks	x	8 bits	C3h	67h	8 bytes (Note 12)	–	16 bits (Note 14)	8 bits (Note 17)	16 bits	x
21	Inventory Initiated	x	8 bits	D1h	67h	–	8 bits	8 bits (Note 13)	0 to 8 bytes (Note 16)	16 bits	x
22	Initiate	x	8 bits	D2h	67h	–	–	–	–	16 bits	x

12. UID optional.
13. Mask length.
14. Block number/First block number.
15. Password number.
16. Mask value.
17. Number of blocks.

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Table 12. INSTRUCTION RESPONSE FORMAT (No Error)

Nr. Crt.	Function	SOF	Flags Response	Data Byte	UID	DSFID	AFI	Memory Size	IC Ref	Data	CRC16	EOF
1	Inventory	x	00h	DSFID	8 bytes	–	–	–	–	–	16 bits	x
2	Stay Quiet	x	–	–	–	–	–	–	–	–	–	x
3	Read single block	x	00h	SSS (Note 18)	–	–	–	–	–	32 bits	16 bits	x
4	Write single block	x	00h	–	–	–	–	–	–	–	16 bits	x
5	Read multiple block	x	00h	SSS (Notes 18, 19)	–	–	–	–	–	32 bits (Note 19)	16 bits	x
6	Select	x	00h	–	–	–	–	–	–	–	16 bits	x
7	Reset to ready	x	00h	–	–	–	–	–	–	–	16 bits	x
8	Write AFI	x	00h	–	–	–	–	–	–	–	16 bits	x
9	Lock AFI	x	00h	–	–	–	–	–	–	–	16 bits	x
10	Write DSFID	x	00h	–	–	–	–	–	–	–	16 bits	x
11	Lock DSFID	x	00h	–	–	–	–	–	–	–	16 bits	x
12	Get System Info–FL_PE = 0	x	00h	0Bh	8 bytes	8 bits	8 bits	–	8 bits	–	16 bits	x
	Get System Info–FL_PE = 1	x	00h	0Fh	8 bytes	8 bits	8 bits	24 bits	8 bits	–	16 bits	x

18. SSS optional (FL_OPT = 1).
19. Repeated as needed.

Table 13. INSTRUCTION RESPONSE FORMAT (Error Flag = 1)

Nr. Crt.	Function	SOF	Flags Response	Error code	CRC16	EOF
1	Inventory	–	–	–	–	–
2	Stay Quiet	–	–	–	–	–
3	Read single block	x	01h	8 bits	16 bits	x
4	Write single block	x	01h	8 bits	16 bits	x
5	Read multiple block	x	01h	8 bits	16 bits	x
6	Select	x	01h	8 bits	16 bits	x
7	Reset to ready	x	01h	8 bits	16 bits	x
8	Write AFI	x	01h	8 bits	16 bits	x
9	Lock AFI	x	01h	8 bits	16 bits	x
10	Write DSFID	x	01h	8 bits	16 bits	x
11	Lock DSFID	x	01h	8 bits	16 bits	x
12	Get System Info	x	01h	8 bits	16 bits	x
13	Get Multiple Block SS	x	01h	8 bits	16 bits	x
14	Write sector password	x	01h	8 bits	16 bits	x
15	Lock sector	x	01h	8 bits	16 bits	x
16	Present sector password	x	01h	8 bits	16 bits	x
17	Fast read single Block	x	01h	8 bits	16 bits	x

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Table 13. INSTRUCTION RESPONSE FORMAT (Error Flag = 1) (continued)

Nr. Crt.	Function	SOF	Flags Response	Error code	CRC16	EOF
18	Fast Inventory Initiated	–	–	–	–	–
19	Fast Initiate	–	–	–	–	–
20	Fast read multiple Block	x	01h	8 bits	16 bits	x
21	Inventory Initiated	–	–	–	–	–
22	Initiate	–	–	–	–	–

Table 14. RESPONSE ERROR CODE

Nr. Crt.	Function	Error Code								
		02h	03h	0Fh	10h	11h	12h	13h	14h	15h
1	Inventory	–	–	–	–	–	–	–	–	–
2	Stay Quiet	–	–	–	–	–	–	–	–	–
3	Read single block	–	x	–	x	–	–	–	–	x
4	Write single block	–	x	–	x	–	x	x	–	–
5	Read multiple block	–	x	x	x	–	–	–	–	x
6	Select	–	x	–	–	–	–	–	–	–
7	Reset to ready	–	x	–	–	–	–	–	–	–
8	Write AFI	–	x	–	–	–	x	x	–	–
9	Lock AFI	–	x	–	–	x	–	–	x	–
10	Write DSFID	–	x	–	–	–	x	x	–	–
11	Lock DSFID	–	x	–	–	x	–	–	x	–
12	Get System Info	–	x	–	–	–	–	–	–	–
13	Get Multiple Block SS	–	x	x	x	–	–	–	–	–
14	Write sector password	x	x	–	x	–	x	x	–	–
15	Lock sector	x	x	–	x	x	–	–	x	–
16	Present sector password	x	x	x	x	–	–	–	–	–
17	Fast read single Block	x	x	–	x	–	–	–	–	x
18	Fast Inventory Initiated	–	–	–	–	–	–	–	–	–
19	Fast Initiate	–	–	–	–	–	–	–	–	–
20	Fast read multiple Block	x	x	x	x	–	–	–	–	x
21	Inventory Initiated	–	–	–	–	–	–	–	–	–
22	Initiate	–	–	–	–	–	–	–	–	–

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Error code	Meaning
02h	The command is not recognized
03h	The option is not supported
0Fh	Unknown error
10h	The specified block is not available (doesn't exist)
11h	The specified block is already locked and this cannot be locked again
12h	The specified block is locked and its content cannot be changed
13h	The specified block was not successfully programmed
14h	The specified block was not successfully locked
15h	The specified block is read−protected

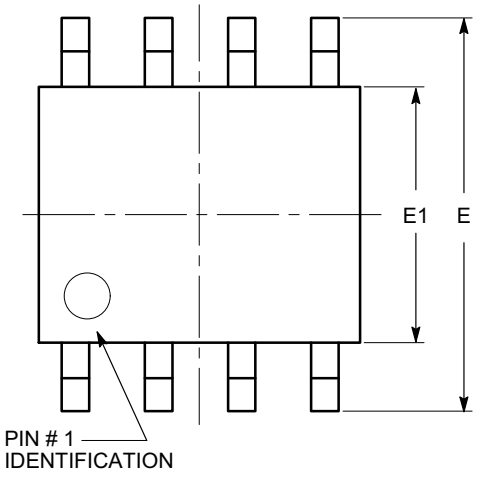
Table 15. REQUEST FLAGS

Nr. Crt.	Function	bit 7	bit6	bit5		bit4		bit3	bit2	bit1	bit0
		RFU	Option Flag	Address Flag	NB Slot Flag	Select Flag	AFI Flag	Protocol Extension Flag	Inventory Flag	Data Rate Flag	Sub−Carrier Flag
1	Inventory	0	0	–	0/1	–	0/1	0	1	0/1	0/1
2	Stay Quiet	0	0	1	–	0	–	0	0	0/1	0/1
3	Read single block	0	0/1	0/1	–	0/1	–	1	0	0/1	0/1
4	Write single block	0	0/1	0/1	–	0/1	–	1	0	0/1	0/1
5	Read multiple block	0	0/1	0/1	–	0/1	–	1	0	0/1	0/1
6	Select	0	0	1	–	0	–	0	0	0/1	0/1
7	Reset to ready	0	0	0/1	–	0/1	–	0	0	0/1	0/1
8	Write AFI	0	0/1	0/1	–	0/1	–	0	0	0/1	0/1
9	Lock AFI	0	0/1	0/1	–	0/1	–	0	0	0/1	0/1
10	Write DSFID	0	0/1	0/1	–	0/1	–	0	0	0/1	0/1
11	Lock DSFID	0	0/1	0/1	–	0/1	–	0	0	0/1	0/1
12	GET System Info	0	0	0/1	–	0/1	–	0/1	0	0/1	0/1
13	Get Multiple Block SS	0	0	0/1	–	0/1	–	1	0	0/1	0/1
14	Write sector password	0	0/1	0/1	–	0/1	–	0	0	0/1	0/1
15	Lock sector	0	0/1	0/1	–	0/1	–	0	0	0/1	0/1
16	Present sector password	0	0	0/1	–	0/1	–	0	0	0/1	0/1
17	Fast read single Block	0	0/1	0/1	–	0/1	–	1	0	0/1	0
18	Fast Inventory Initiated	0	0	–	0/1	–	0/1	0	1	0/1	0
19	Fast Initiate	0	0	0	–	0	–	0	0	0/1	0
20	Fast read multiple Block	0	0/1	0/1	–	0/1	–	1	0	0/1	0
21	Inventory Initiated	0	0	–	0/1	–	0/1	0	1	0/1	0/1
22	Initiate	0	0	0	–	0	–	0	0	0/1	0/1

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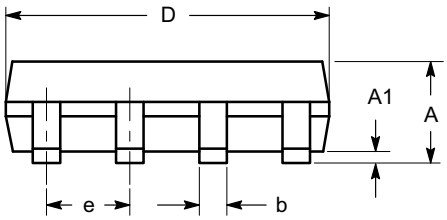
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

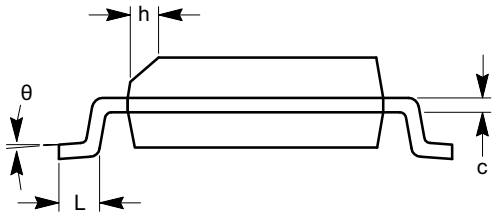


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW

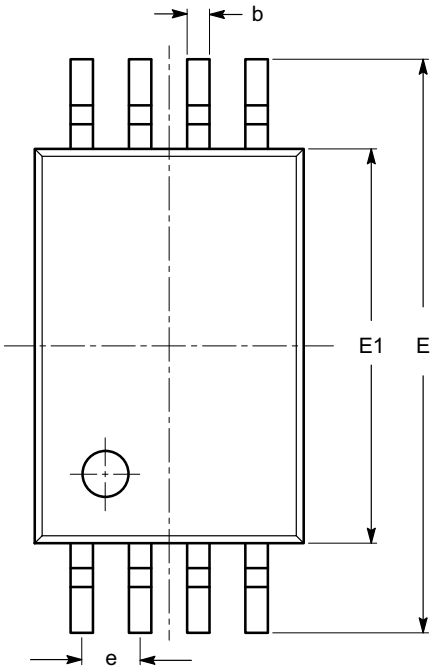


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

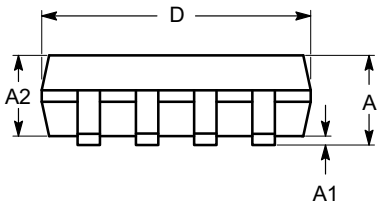
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TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

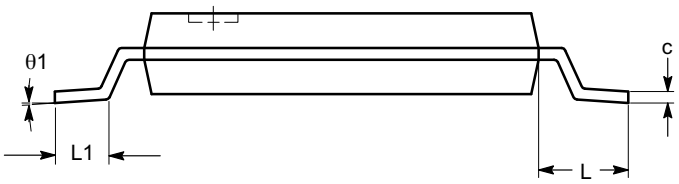


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
N24RF64DWPT3G	24RF64	SOIC−8 (Pb−Free)	−40°C to +105°C	NiPdAu	3,000 / Tape & Reel
N24RF64DTPT3G	RF64	TSSOP−8 (Pb−Free)	−40°C to +105°C	NiPdAu	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

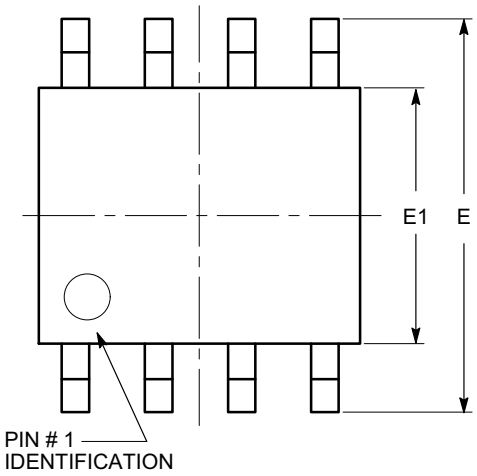
20. All packages are RoHS−compliant (Pb−Free, Halogen−free).

21. Contact factory for availability.

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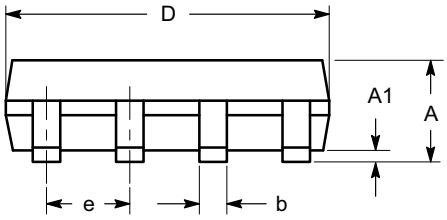
SOIC−8, 150 mils
CASE 751BD
ISSUE O

DATE 19 DEC 2008

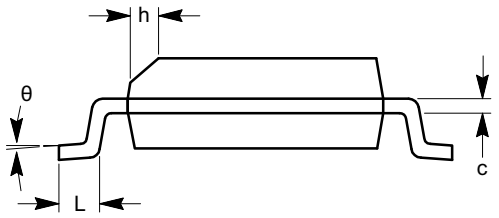


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



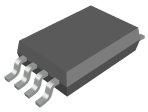
END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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DESCRIPTION:	**SOIC−8, 150 MILS**	**PAGE 1 OF 1**

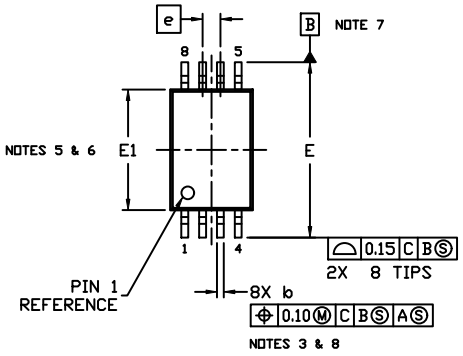
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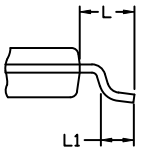


TSSOP8, 4.4x3.0, 0.65P
CASE 948AL
ISSUE A

DATE 20 MAY 2022



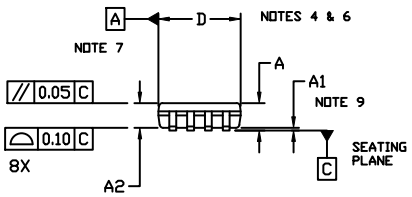
TOP VIEW



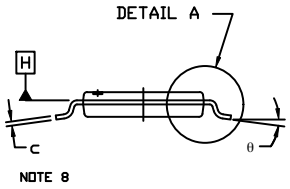
DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009..
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP..
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY..



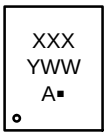
SIDE VIEW



END VIEW

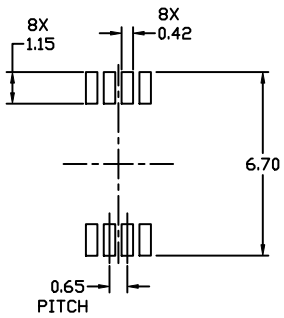
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
Y = Year
WW = Work Week
A = Assembly Location
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**TSSOP8, 4.4X3.0, 0.65P**		**PAGE 1 OF 1**

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