UM10492

PTN3460 eDP to LVDS bridge IC application board

Rev. 1.1 — 16 March 2015 **User manual**

Document information

Info	Content
Keywords	PTN3460, DisplayPort, eDP, LVDS, bridge, application board
Abstract	This user manual presents demonstration/application board capability of interfacing an (embedded) DisplayPort source to an LVDS panel. The application board (nicknamed ‘DPLVDS1’) is intended for use as an evaluation and customer demonstration tool, as well as a reference design.

Revision history

Rev	Date	Description
1.1	20150316	Table 3; Removed remark for JP10
1	20140903	User manual; initial release

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1. Introduction

This user manual describes the PTN3460 application board with 1080p LCD panel made by AUO (part number M215HW03 V1), including:

- Overall PCB connectors, jumpers, and power supplies
- Equipment/tools that this board interfaces with during bench testing
- System-level connections, such as cables and connectors, into which this board will be plugged

This application board is intended to demonstrate the bridging capabilities of PTN3460 on DP to LVDS conversion. It is also used to evaluate competitor's ICs such as Parade's PS8615, which is pin-to-pin compatible with PTN3460.

A separate document, *"Application test plan"* will be provided to list items to be verified at the system level.

1.1 Purpose

- For internal engineers to evaluate the performance of PTN3460 and to develop firmware, including collecting and verifying system-level features, performance, and functionality, such as:
  - Verify power management schemes
  - Power sequence
  - Power consumption measurement during various operating modes
  - Allow access to test points and jumpers for measurement and configuration purposes
  - Flash over AUX
  - Programming test via I^2C-bus
- For marketing to demonstrate DP-LVDS to customers in the field
  - Functional and interoperability test
  - This board should be connected to a DP or an eDP source
  - This board is powered by ATX 20-pin power supply, or
  - External power supplies with +3.3 V (1 A), +5 V (1 A), +12 V (2 A)
  - This board is connected directly to AUO 21-inch LVDS panel, or
  - Connect to NoteBook 14-inch LVDS panel via an AUO-NB adaptor board
- For customers to evaluate PTN3460
  - Use I^2C-bus to program EDID

2. General description

2.1 Block diagram

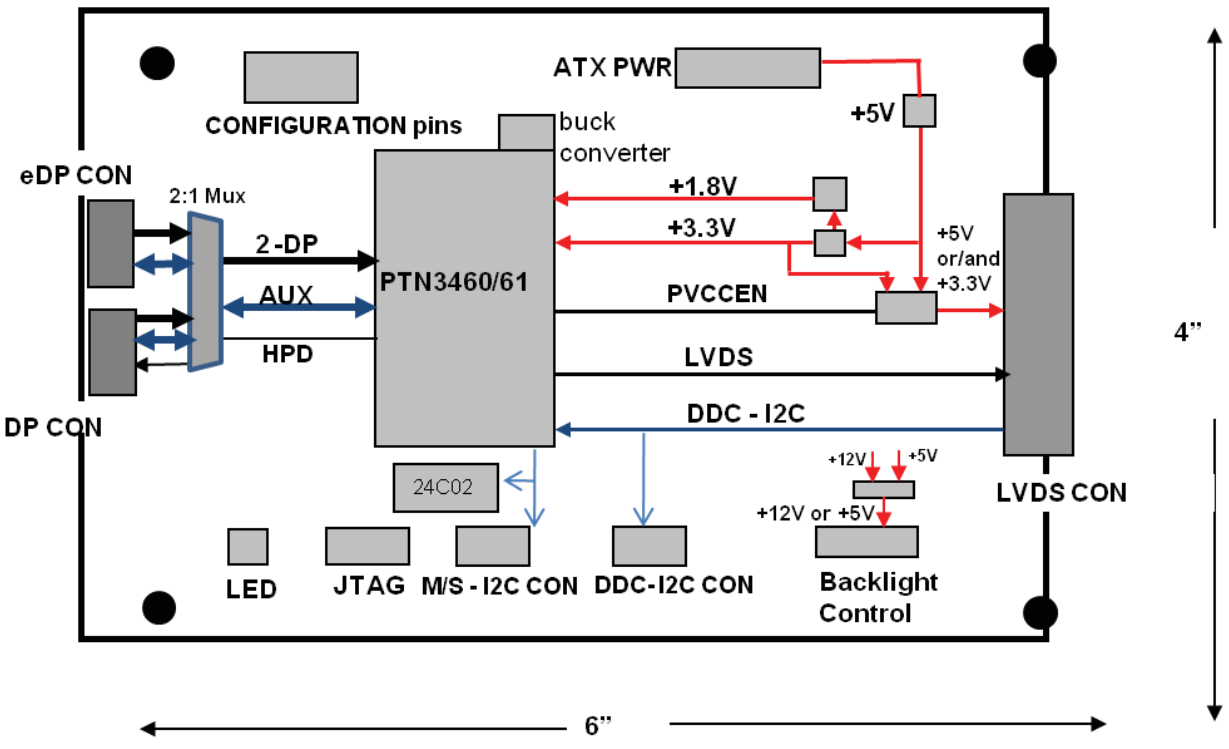

Fig 1. DP-LVDS block diagram

2.2 PCB stack ups

Stack Up

PCB Stack Up				Impedance			
Layer	Type	Thickness (mil)					
Top side solder mask			0.50 mils	Single		DIFF	
L1	TOP	copper+plating	1.58 mils	8 mils , 50Ω±5Ω	53.09 Ω	6/8/6 mils , 100Ω±5Ω	101.26 Ω
		Prepreg	6.00 mils				
L2	GND	copper	1.30 mils				
		core	42.60 mils				
L3	GND	copper	1.30 mils				
		Prepreg	6.00 mils				
L4	Bottom	copper+plating	1.58 mils	8 mils , 50Ω±5Ω	53.09 Ω	6/8/6 mils , 100Ω±5Ω	101.26 Ω
Bottom side solder mask			0.50 mils				
TOTAL			61.36 mils 1.56 mm				

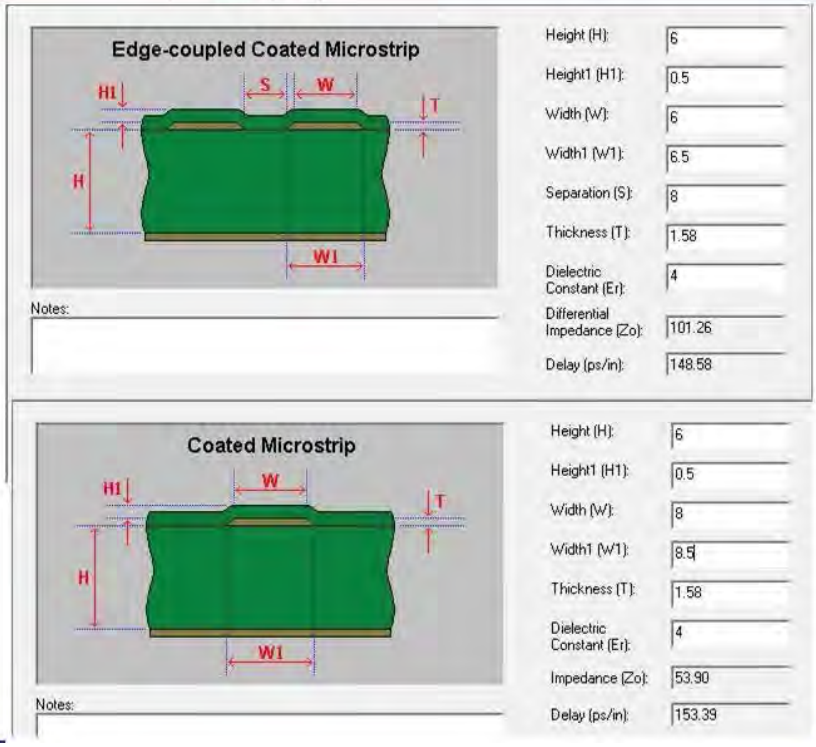

Fig 2. DP-LVDS PCB stack up example

2.3 PTN3460 application board top and bottom assemblies

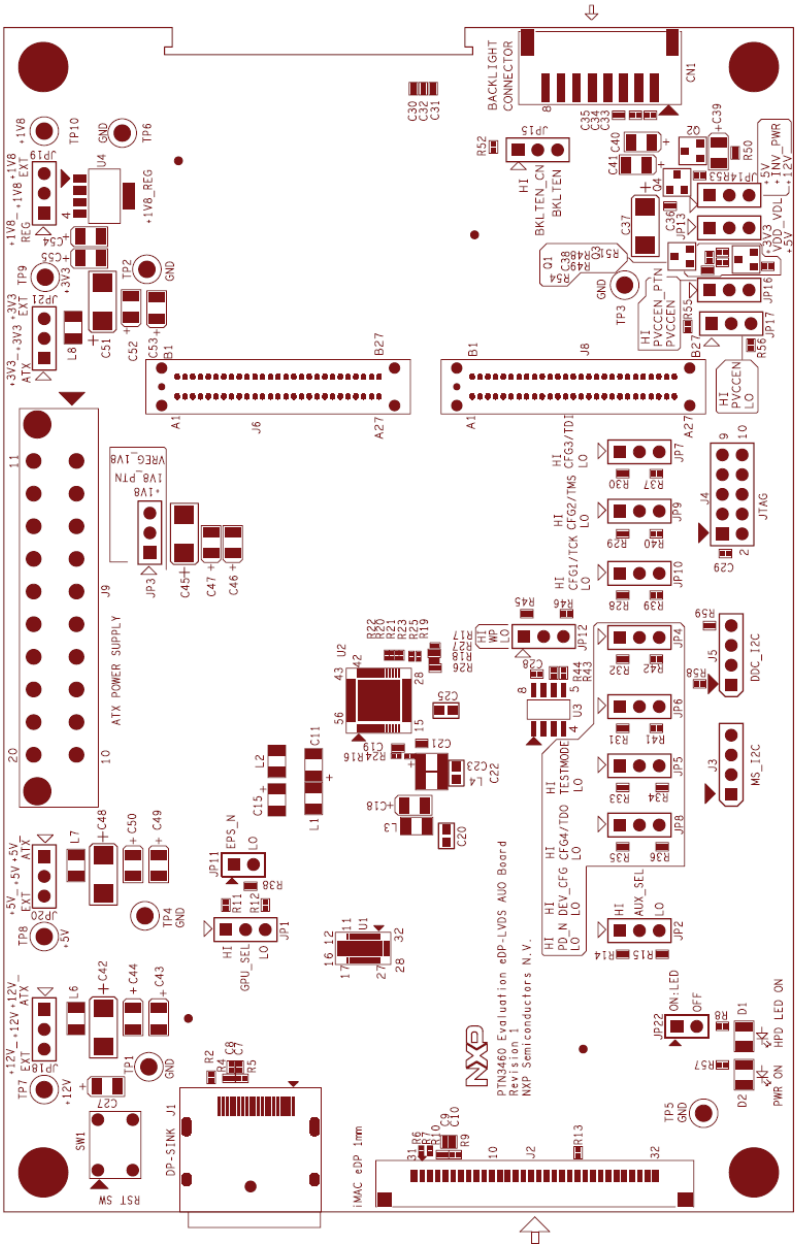

Fig 3. PTN3460 application board top assembly

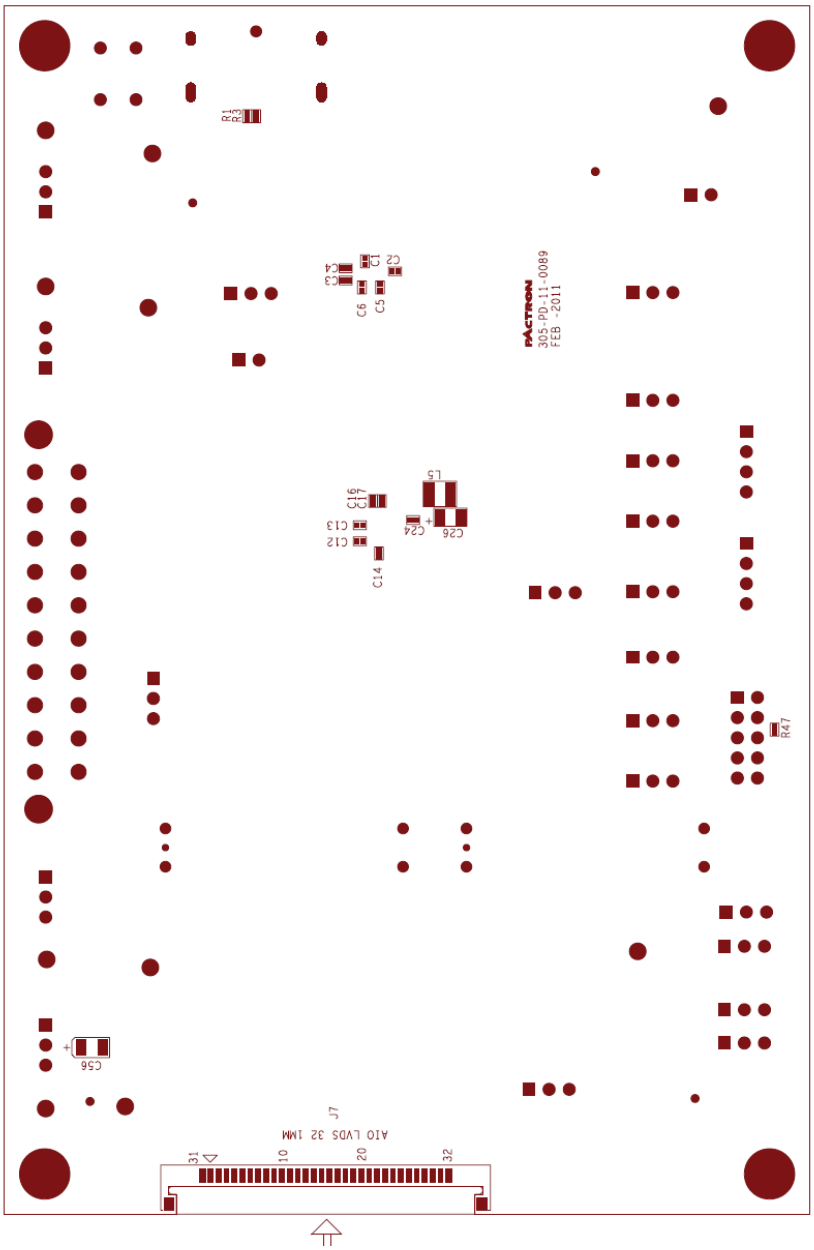

Fig 4. PTN3460 application board bottom assembly

The PTN3460 AUO application board has the following features:

- Jumpers select multiplex between DP and eDP (iMac) sources
- Stuff options for PTN3460 different pin configurations
- Stuff options for PS8615 test
- Four (4) groups of jumpers for pin configuration
- Other jumpers for test options
- One serial EEPROM to store EDID read/write via I^2C-bus
- One I^2C-bus header bringing out I^2C-bus pins (SCL, SDA, GND) to interface with an I^2C Bird (I^2C tool device name) dongle to program S-EEPROM or to read iMac System Bus
- One I^2C-bus header for DDC control
- One JTAG for firmware download
- One ATX 20-pin power supply with 12 V/5 V/3.3 V DC inputs
- External power supplies: +12 V (2 A), +5 V (1 A), +3.3 V (1 A)
- Fixed regulator provides 1.8 V ± 10 % power supply
- Two soft-touch connectors (not loaded) for Agilent differential probes to capture LVDS signals
- One 30-position, 1 mm connector with cables to connect to AUO 21-inch LVDS panel
- One 1 × 8 connector with cable to connect to backlight inverter

3. Hardware requirements

- iMac 27-inch AIO, eDP source with 30-position eDP cable
- VTG5225-DP, DP source with DP 1.1 cable
- DPA-400, AUX analyzer, via iMac eDP-DP adaptor with two DP 1.1 cables and two 30-position eDP cables
- UFG-04, LVDS grabber, via AUO-grabber adaptor with two MDR-26 twisted cables
- Desktop PC with PCIe slot to install LVDS grabber
- AUO 21-inch LVDS panel with 30-position LVDS cable
- FS2 with 2 × 5 JTAG connection for firmware download
- I^2C Bird with 1 × 4 header connection for s-EEPROM read/write

4. Board specifications

- Layers: four layers expected — trace, ground, V_{CC}, trace
- Size: 4 inches × 6 inches
- Material: FR4
- Thickness: 62 mil
- Impedance: 50 Ω single-ended, 100 Ω differential on DP and LVDS signal pairs

5. Connector specifications

5.1 Connectors

Table 1. Connectors

Connector	Type		Supplier	Part number
J1	DP CONN SINK	conn-47272-0001	Molex	47272-0001
J2	FI-X30SSL-HF	conn_FI-X30SSL-HF	JAE	FI-X30SSL-HF
J3, J5	HEADER 4	hdr_4x1	Sullins	PBC04SAAN
J4	HEADER, 2 × 5	hdr_5x2	Sullins	PBC05DAAN
J6, J8	SOFT TOUCH CONN ES387-68701	conn_ES387-68701	Agilent	ES387-68701
J7	FI-XB30SRL-HF11	conn_FI-XB30SRL-HF11	JAE	FI-XB30SRL-HF11
J9	MOLEX ATX PWR PN 39-29-9202	cn_molex_minfit20p_vt	Molex	39-29-9202
CN1	S8B-PH-SM4-TB(LF)(SN)	conn_8x1_2mm	JST Sales	S8B-PH-SM4-TB(LF)(SN)

5.2 Cables

Table 2. Cables

Test cable location	Test cable	Description
J1	DP 1.1 cable	Purchase ready-made cable
J2	iMac 30-position eDP 1 mm cable	Made from LVDS 30-position cable kit
J3, J5	I^2C Bird 1 × 4 cable	Ready-made with I^2C Bird box
J4	JTAG 2 × 5 ribbon cable	Ready-made with FS2 box
J6, J8	Agilent soft-touch probes	90-pin differential probe E5387A (2)
J7	AUO 30-position LVDS 1 mm cable	Made from LVDS 30-position cable kit
J9	Backlight inverter 1 × 8	Made from accessories

5.3 Jumpers

Table 3. Jumpers

Jumper number	Signal names	Jumper settings	Default setting
JP1	U1 MUX GPU_SEL	**1-2 HIGH —** select DP inputs **2-3 LOW —** select eDP inputs	1-2
JP2	U1 MUX AUX_SEL	**1-2 HIGH —** select AUX from DP inputs **2-3 LOW —** select AUX from eDP inputs	1-2
JP3	1V8_PTN	**1-2 —** 1.8 V from on-board regulator **2-3 —** 1.8 V from Buck converter	1-2
JP4	TESTMODE	**1-2 HIGH —** CFG[4:1] = JTAG pins **2-3 LOW —** CFG[4:1] = CONFIG pins	2-3
JP5	DEV_CFG	**1-2 HIGH —** I^2C-bus master **open —** I^2C-bus slave (0C0h) **2-3 LOW —** I^2C-bus slave (040h)	2-3

Table 3. Jumpers *...continued*

Jumper number	Signal names	Jumper settings	Default setting
JP6	CFG4/TDO	**1-2 HIGH —** LVDS output swing = 400 mV **open —** LVDS output swing = 300 mV **2-3 LOW —** LVDS output swing = 250 mV	1-2
JP7	CFG3/TDI	**1-2 HIGH —** LVDS clock frequency = 0.5 % **open —** LVDS clock frequency = 1 % **2-3 LOW —** LVDS clock frequency = 0 %	1-2
JP8	PD_N	**1-2 HIGH —** Operation mode **2-3 LOW —** Force power-down	1-2
JP9	CFG2/TMS	**1-2 HIGH —** JEIDA or VESA format (18 bpp) **open —** JEIDA format (24 bpp) **2-3 LOW —** VESA format (24 bpp)	1-2
JP10	CFG1/TCK	**1-2 HIGH —** Dual LVDS bus **2-3 LOW —** Single LVDS bus	1-2
JP11	EPS_N	**ON —** Use external 3.3 V/1.8 V option **OFF —** Use internal 1.8 V LDO	1-2
JP12	WP	**1-2 HIGH —** WP for S-EEPROM **2-3 LOW —** No WP S-EEPROM	2-3
JP13	VDD_VOL	**1-2 —** select +3V3 for panel **2-3 —** select +5V for panel	1-2
JP14	+INV_PWR	**1-2 —** select +5V for backlight inverter **2-3 —** select +12V for backlight inverter	1-2
JP15	BKLTEN_CN	**1-2 HIGH —** Backlight enable is always ON **2-3 BKLTEN —** Control by firmware	1-2
JP16	PVCCEN_PTN	**1-2 HIGH —** PVCCEN is always ON **2-3 PVCCEN —** Control by firmware	1-2
JP17 (for PS8615 only)	PVCCEN (pin 33 is used as I2C_Addr/GPIO in PS8615)	**1-2 HIGH —** I2C_ADDR 0xB0h to 0xBFh **2-3 LOW —** I2C_ADDR 0x10h to 0x1Fh	not loaded
JP18	+12V	**1-2 —** select from ATX power supply **2-3 —** select from external power supply	2-3
JP19	+1V8	**1-2 —** select from U4 regulator **2-3 —** select from external power supply	1-2
JP20	+5V	**1-2 —** select from ATX power supply **2-3 —** select from external power supply	2-3
JP21	+3V3	**1-2 —** select from ATX power supply **2-3 —** select from external power supply	2-3
JP22	AIOC_HPD	**ON —** HPD drives Green LED **OFF —** No LED drive to measure power	1-2

6. Stuffing options

6.1 PTN3460 NXP pinning

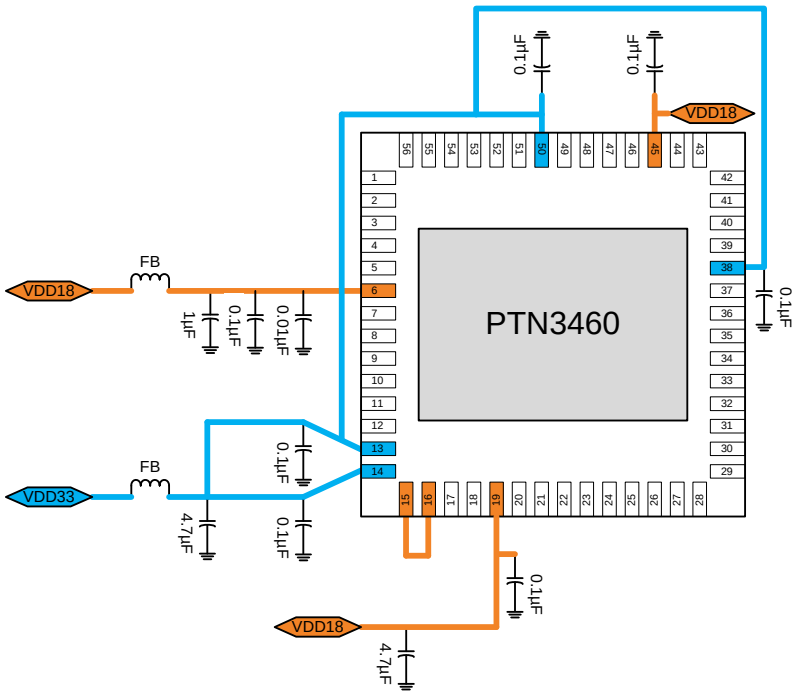

Fig 5. PTN3460 pinning

6.2 Stuffing locations

Table 4. Stuffing locations

Location	Function/value	PTN3460 (default pinning)
R16	Join +3V3_IO with +3V3_LDO	no load
R17	Pin 27 = CFG4/TDO	load
R18	Pin 26 = BKLTEN_PTN	load
R19	Pin 28 - PWMO_PTN	load
R20	Pin 32 = LVSDE_N_PTN	load
R21	Pin 31 = LVSDE_P_PTN	load
R22	Pin 32 = PWMO	no load
R23	Pin 31 = BKLTEN	no load
R24	+3V3_LDO for pin 13, 14	load
R25	Pin 28 = GND	no load
R26	Pin 26 = GND	no load
R27	Pin 27 = GND	no load
C27	1 µF for RST_N line	no load
C22	0.47 µF	no load

Table 4. Stuffing locations *…continued*

Location	Function/value	PTN3460 (default pinning)
C23	4.7 μF	no load
L4	FB	no load
C25	0.47 μF	no load
C26	4.7 μF	no load
L5	10 μH	no load
C15	2.2 μF	load

7. Abbreviations

Table 5. Abbreviations

Acronym	Description
AUO	Active User Object
DP	DisplayPort
EDID	Extended Display Identification Data
eDP	embedded DisplayPort
EEPROM	Electrically Erasable Programmable Read-Only Memory
I^2C-bus	Inter-Integrated Circuit-bus
IC	Integrated Circuit
JTAG	Joint Test Action Group
LED	Light-Emitting Diode
LDO	Low-DropOut regulator
LVDS	Low-Voltage Differential Signalling
NB	NoteBook
PC	Personal Computer
PCB	Printed-Circuit Board

8. References

[1] Data Specification, PTN3460_DP_LVDS_Bridge_v1.7.pdf

[2] Schematic, DP-LVDS-AUO rev1.14 rew.pdf

[3] BOM, DP-LVDS-AUO rev1.14.xls

[4] PTN3460 PCB Layout Guideline.pdf

[5] Allegro layout, PTN3460 Evaluation eDP-LVDS AUO Board_PCB_0089_021811-1.brd

[6] Test Cables, PTN3460 Test Cables.pdf

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