

MOSFET – Power, Single N-Channel

40 V, 1.25 mΩ, 451 A

NVMJST1D2N04C

Features

- Small Footprint (5x7 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- TCPAK57 5x7 Top Cool Package
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	40	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 100^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to $+175$	$^\circ\text{C}$
Source Current (Body Diode)	I_S	379	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 24 \text{ A}$)	E_{AS}	1541	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

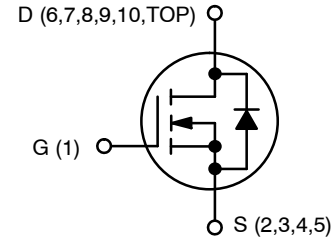
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

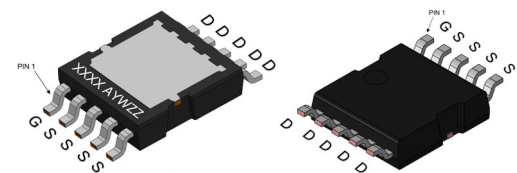
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.33	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	29	
Junction-to-Drain Lead	Ψ_{JL}	5.2	
Junction-to-Source Lead	Ψ_{JL}	5.16	
Junction-to-Heatsink Top (Note 2)	Ψ_{JH}	1.5	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. 2s2p JEDEC51-7 standard PCB mounted to a 25x25x3 (mm) aluminum heatsink with a 12 w/mK TIM interface.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	1.25 mΩ @ 10 V	451 A

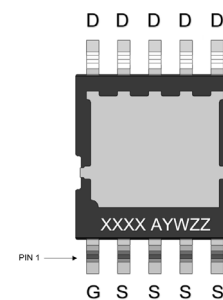


N-CHANNEL MOSFET



TCPAK57
CASE 760AG

MARKING DIAGRAM



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			20		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 40\text{ V}$	$T_J = 25\text{ }^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 200\text{ }\mu\text{A}$	2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-7.7		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		1.06	1.25	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 50\text{ A}$		161		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 20\text{ V}$		5340		pF
Output Capacitance	C_{OSS}			3500		
Reverse Transfer Capacitance	C_{RSS}			140		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}; I_D = 50\text{ A}$		82		nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}; I_D = 50\text{ A}$		5.3		
Gate-to-Source Charge	Q_{GS}			21		
Gate-to-Drain Charge	Q_{GD}			23		
Plateau Voltage	V_{GP}			4.7		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 32\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$		22		ns
Rise Time	t_r			19		
Turn-Off Delay Time	$t_{d(OFF)}$			54		
Fall Time	t_f			20		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		0.65		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$		113		ns	
Charge Time	t_a			52			
Discharge Time	t_b			61			
Reverse Recovery Charge	Q_{RR}			236		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

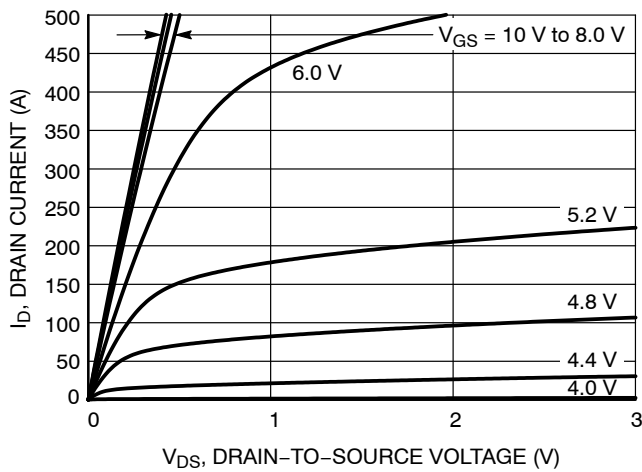


Figure 1. On-Region Characteristics

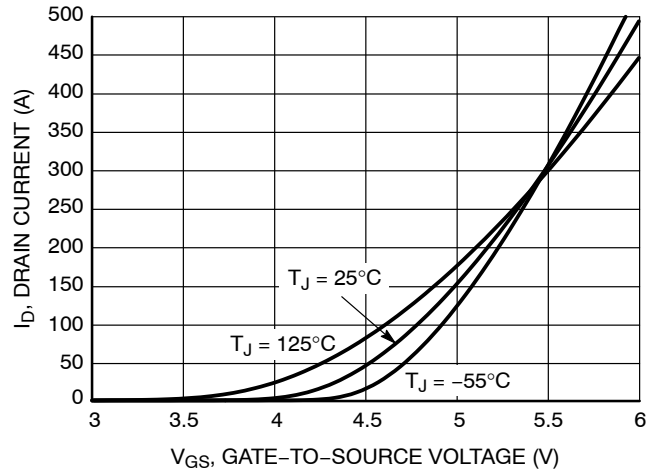


Figure 2. Transfer Characteristics

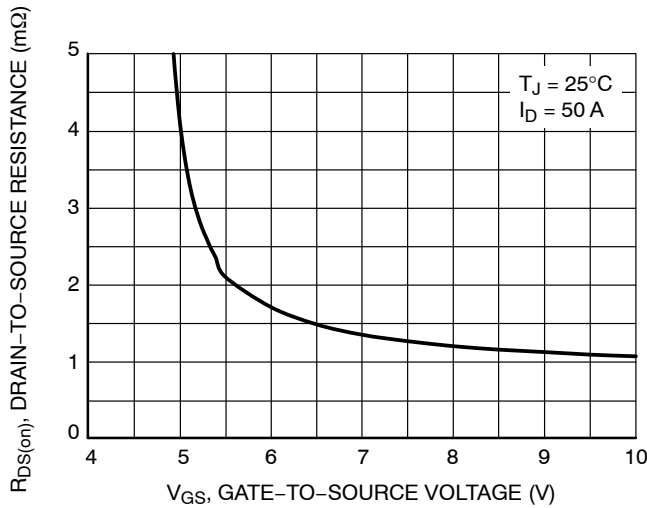


Figure 3. On-Resistance vs. Gate-to-Source Voltage

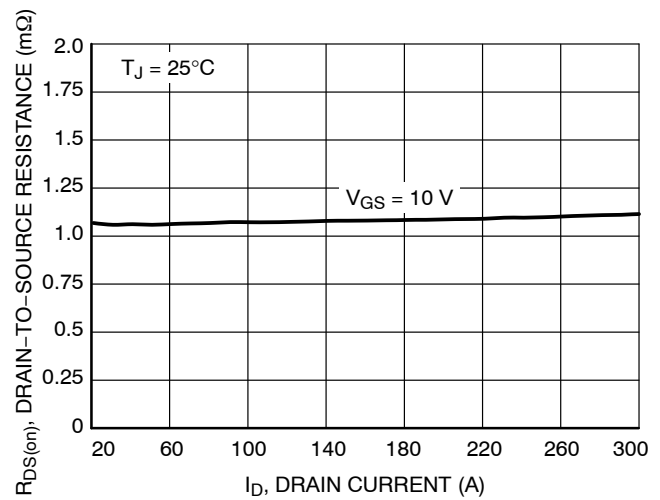


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

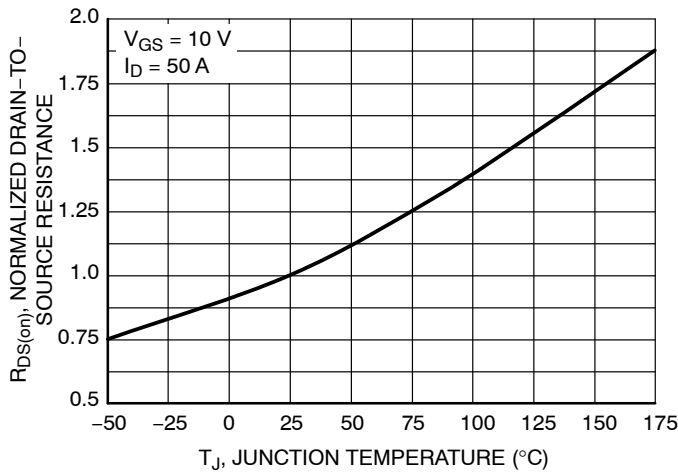


Figure 5. On-Resistance Variation with Temperature

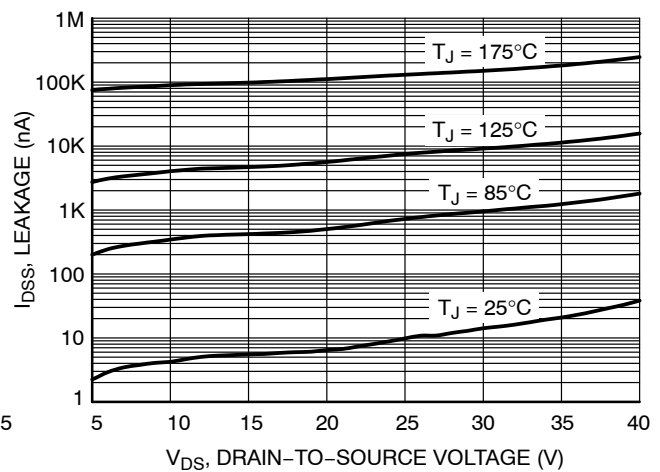


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

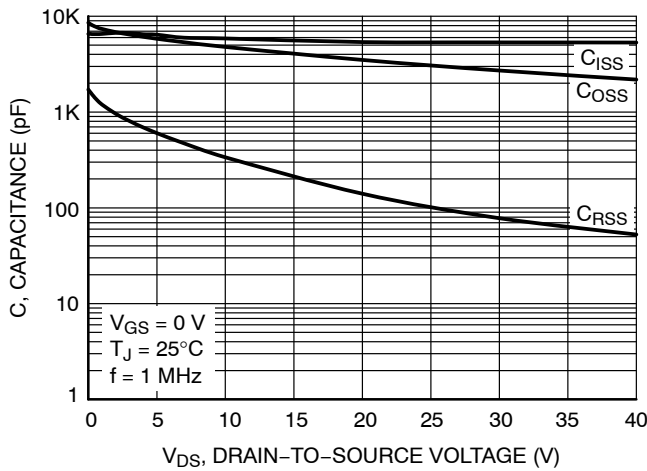


Figure 7. Capacitance Variation

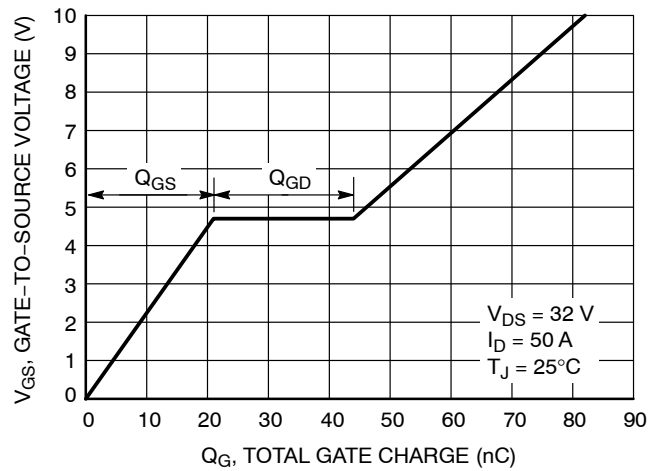


Figure 8. Gate-to-Source vs. Total Charge

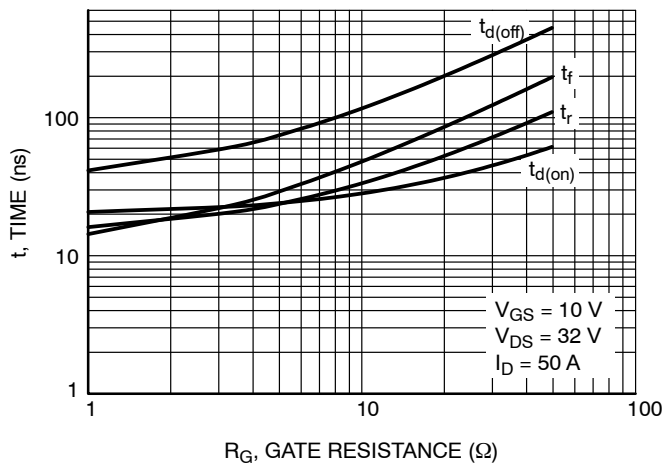


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

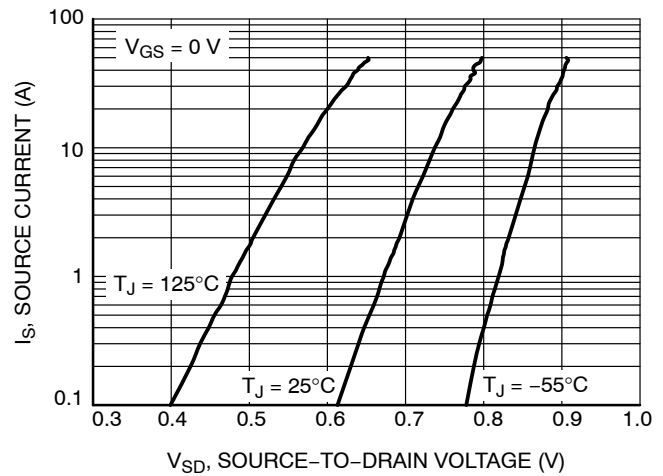


Figure 10. Diode Forward Voltage vs. Current

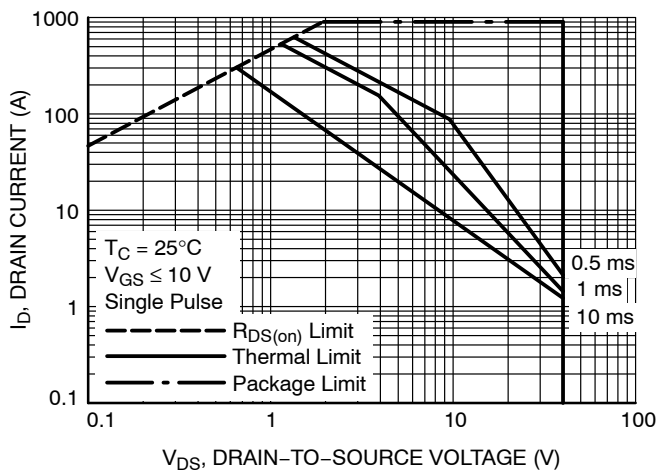


Figure 11. Maximum Rated Forward Biased Safe Operating Area

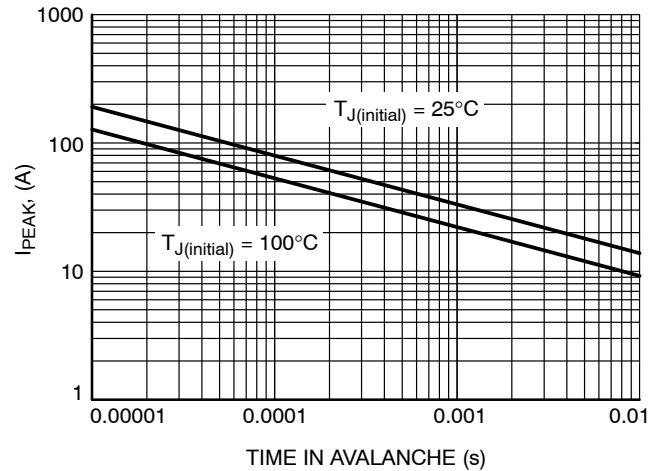


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

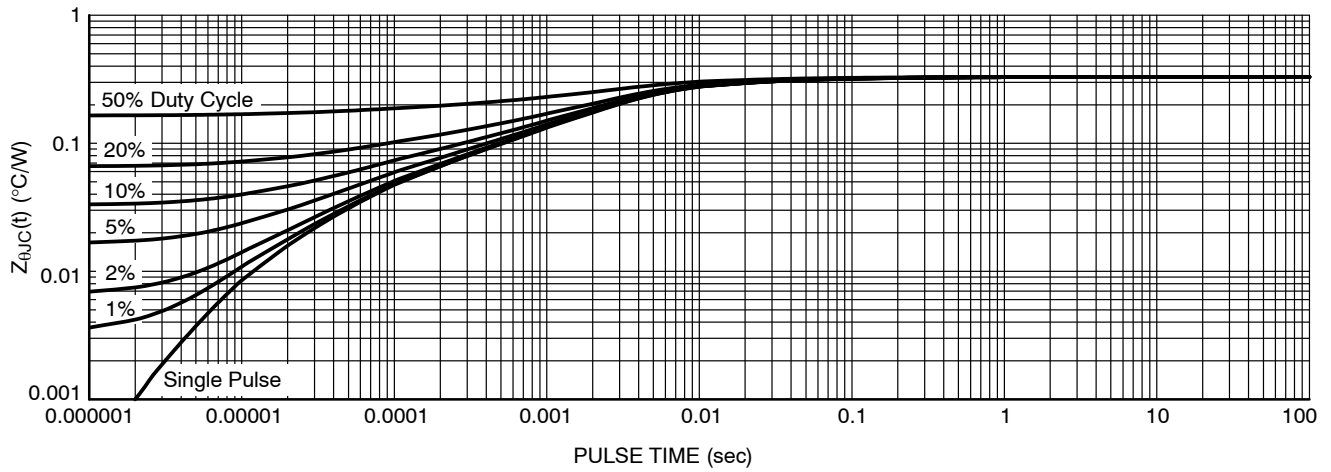


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

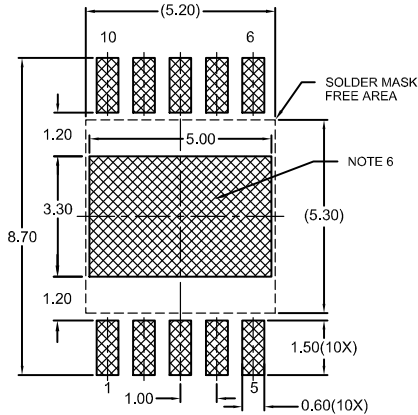
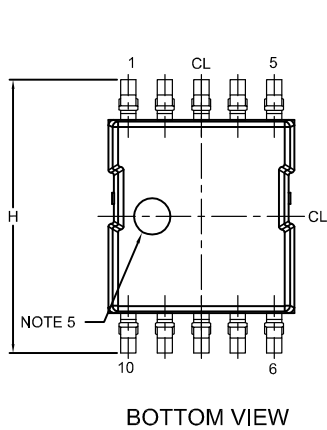
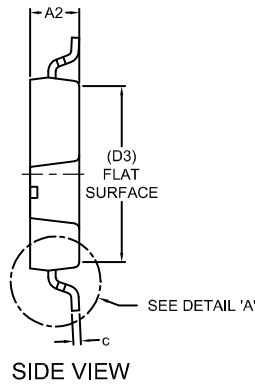
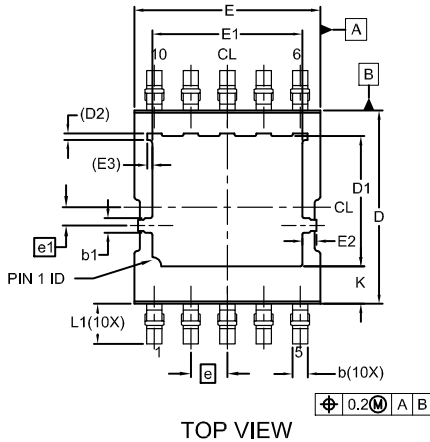
Device	Marking	Package	Shipping [†]
NVMJST1D2N04CTXG	1D24C	TCPAK57 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

LFPK10 7.5x5 CASE 760AG ISSUE C

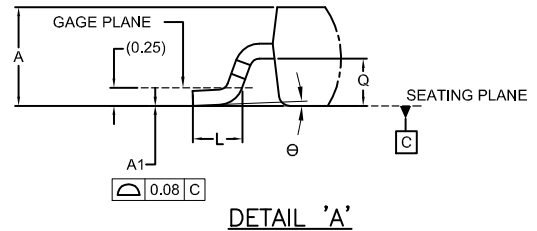


*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. UNIT DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.
6. LAND PAD UNDER THE PACKAGE BODY IS FOR MECHANICAL SUPPORT ONLY. SOLDER CONNECTION IS NOT REQUIRED.
7. DIMENSION A1 IS THE LEAD STAND-OFF FROM THE BOTTOM SURFACE OF THE PACKAGE BODY.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.30	1.35	1.45
A1	-0.05	0.00	0.05
A2	1.30	1.35	1.40
b	0.36	0.41	0.46
b1	0.30	0.40	0.50
c	0.16	0.21	0.26
D	5.20	5.30	5.40
D1	3.47	3.57	3.67
D2	0.17 REF		
D3	4.82 REF		
E	5.00	5.10	5.20
E1	4.02	4.12	4.22
E2	0.30	0.40	0.50
E3	0.14 REF		
e	1.00 BSC		
e1	0.50 BSC		
K	0.93	1.03	1.13
H	7.30	7.50	7.70
L	0.49	0.69	0.89
L1	0.90	1.10	1.30
Q	0.60	0.65	0.70
Θ	0°	2.5°	5°



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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

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For additional information, please contact your local Sales Representative

