MC74HCT132A

Quad 2-Input NAND Gate with Schmitt-Trigger Inputs with LSTTL Compatible Inputs

High−Performance Silicon−Gate CMOS

The MC74HCT132A is identical in pinout to the LS132. The device inputs are compatible with standard CMOS outputs; with pull−up resistors, they are compatible with LSTTL outputs.

The MC74HCT132A can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements as Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates
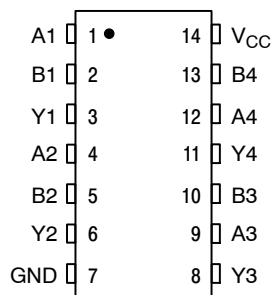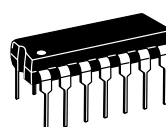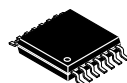- These are Pb−Free Devices

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MARKING DIAGRAMS

PDIP−14
N SUFFIX
CASE 646

MC74HCT132AN
○ AWLYYWWG

SOIC−14
D SUFFIX
CASE 751A

HCT132AG
AWLYWW
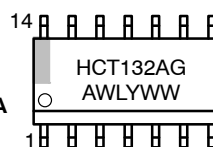
TSSOP−14
DT SUFFIX
CASE 948G

HCT
132A
ALYW▪
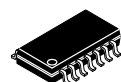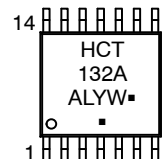
SOEIAJ−14
F SUFFIX
CASE 965

74HCT132A
ALYWG
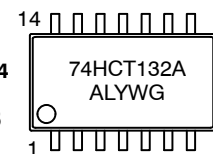
A	= Assembly Location
L, WL	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

Figure 1. Pin Assignment

Left	Pin	Pin	Right
A1	1	14	V_CC
B1	2	13	B4
Y1	3	12	A4
A2	4	11	Y4
B2	5	10	B3
Y2	6	9	A3
GND	7	8	Y3

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.
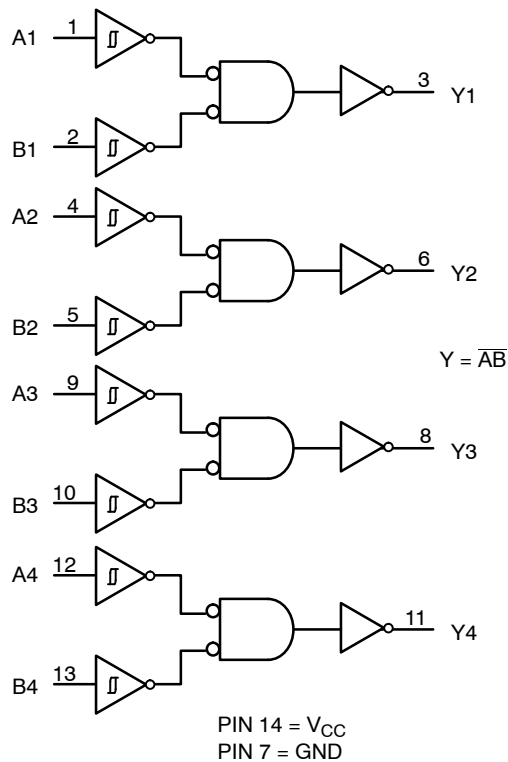
MC74HCT132A

$$Y = \overline{AB}$$

PIN 14 = V_{CC}
PIN 7 = GND

Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT132ANG	PDIP−14 (Pb−Free)	25 / Tape & Ammo Box
MC74HCT132ADG	SOIC−14 (Pb−Free)	55 Units / Rail
MC74HCT132ADR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel
MC74HCT132ADTR2G	TSSOP−14*	2500 / Tape & Reel
MC74HCT132AFELG	SOEIAJ−14 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		-0.5 to $+7.0$	V
V_{IN}	Digital Input Voltage		-0.5 to $+7.0$	V
V_{OUT}	DC Output Voltage	Output in 3−State High or Low State	-0.5 to $+7.0$ -0.5 to V_{CC} $+0.5$	V
I_{IK}	Input Diode Current		-20	mA
I_{OK}	Output Diode Current		±20	mA
I_{OUT}	DC Output Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{GND}	DC Ground Current per Ground Pin		±75	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		$+150$	°C
θ_{JA}	Thermal Resistance	14−PDIP 14−SOIC 14−TSSOP	78 125 170	°C/W
P_D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% − 35%	UL 94 V0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	>2000 >100 >500	V
$I_{Latch-Up}$	Latch−Up Performance	Above V_{CC} and Below GND at 85°C (Note 4)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Tested to EIA/JESD22−A114−A.
2. Tested to EIA/JESD22−A115−A.
3. Tested to JESD22−C101−A.
4. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	$+125$	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	–	No Limit (Note 5)	ns

5. When $V_{IN} \sim 0.5\ V_{CC}$, $I_{CC} >>$ quiescent current.
6. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				$-55°C$ to $25°C$	$\leq 85°C$	$\leq 125°C$	
V_{T+}max	Maximum Positive–Going Input Threshold Voltage	$V_{OUT} = 0.1$ V $|I_{OUT}| \leq 20$ µA	4.5 5.5	1.9 2.1	1.9 2.1	1.9 2.1	V
V_{T+}min	Minimum Positive–Going Input Threshold Voltage	$V_{OUT} = 0.1$ V $|I_{OUT}| \leq 20$ µA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V_{T-}max	Maximum Negative–Going Input Threshold Voltage	$V_{OUT} = V_{CC} - 0.1$ V $|I_{OUT}| \leq 20$ µA	4.5 5.5	1.2 1.4	1.2 1.4	1.2 1.4	V
V_{T-}min	Minimum Negative–Going Input Threshold Voltage	$V_{OUT} = V_{CC} - 0.1$ V $|I_{OUT}| \leq 20$ µA	4.5 5.5	0.5 0.6	0.5 0.6	0.5 0.6	V
$V_H$min (Note 7)	Minimum Hysteresis Voltage	$V_{OUT} = 0.1$ V or $V_{CC} - 0.1$ V $|I_{OUT}| \leq 20$ µA	4.5 5.5	0.4 0.4	0.4 0.4	0.4 0.4	V
V_{OH}	Minimum High–Level Output Voltage	$V_{IN} \leq V_{T-}$min or V_{T+}max $|I_{OUT}| \leq 20$ µA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{IN} \leq -V_{T-}$min or V_{T+}max $|I_{OUT}| \leq 4.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low–Level Output Voltage	$V_{IN} \geq V_{T+}$max $|I_{OUT}| \leq 20$ µA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{IN} \geq V_{T+}$max $|I_{OUT}| \leq 4.0$ mA	4.5	0.26	0.33	0.4	
I_{IN}	Maximum Input Leakage Current	$V_{IN} = V_{CC}$ or GND	5.5	± 0.1	± 1.0	± 1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ µA	5.5	1.0	10	40	µA

7. $V_H$min $> (V_{T+}$min$) - (V_{T-}$max$)$; $V_H$max $= (V_{T+}$max$) + (V_{T-}$min$)$.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns, $V_{CC} = 5.0$ V $\pm 10\%$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			$-55°C$ to $25°C$	$\leq 85°C$	$\leq 125°C$	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 3 and 4)	5.0	25	31	38	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 3 and 4)	5.0	15	19	22	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (per Gate) (Note 8)	24	pF

8. Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

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V_I = GND to 3.0 V
V_M = 1.3 V
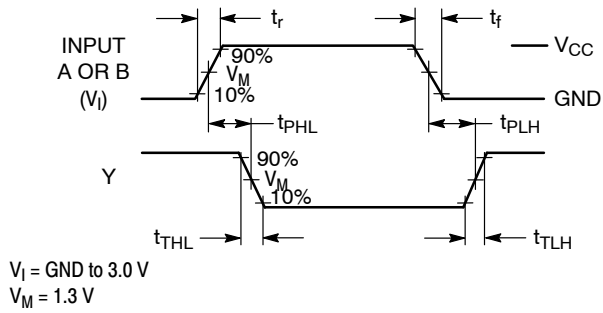
Figure 3. Switching Waveforms

*Includes all probe and jig capacitance

Figure 4. Test Circuit

(a) A SCHMITT TRIGGER SQUARES UP INPUTS
   WITH SLOW RISE AND FALL TIMES
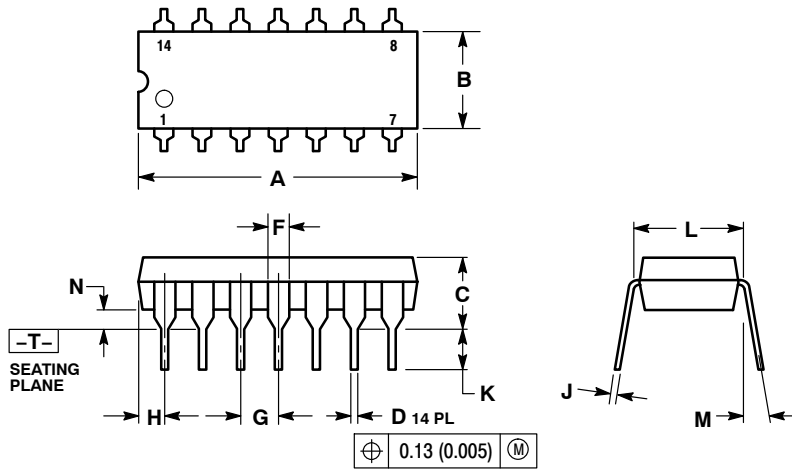
(b) A SCHMITT TRIGGER OFFERS MAXIMUM
   NOISE IMMUNITY
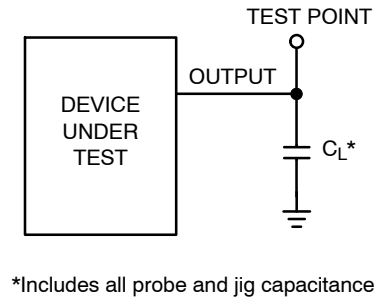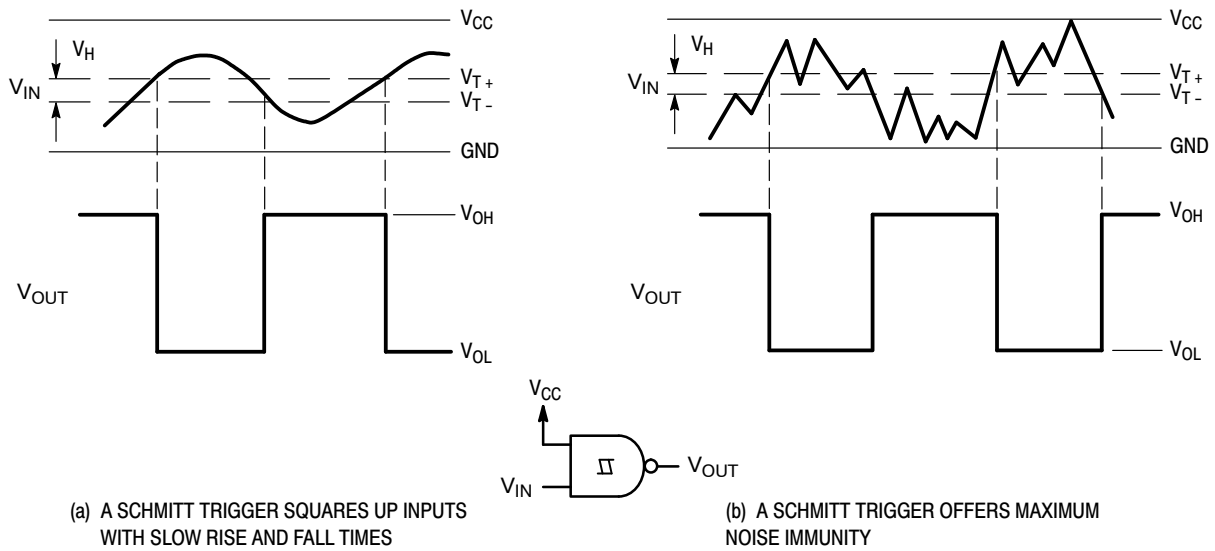
Figure 5. Typical Schmitt−Trigger Applications

PACKAGE DIMENSIONS

PDIP−14
CASE 646−06
ISSUE P

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
---	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.015	0.039	0.38	1.01

PACKAGE DIMENSIONS

SOIC−14
CASE 751A−03
ISSUE J
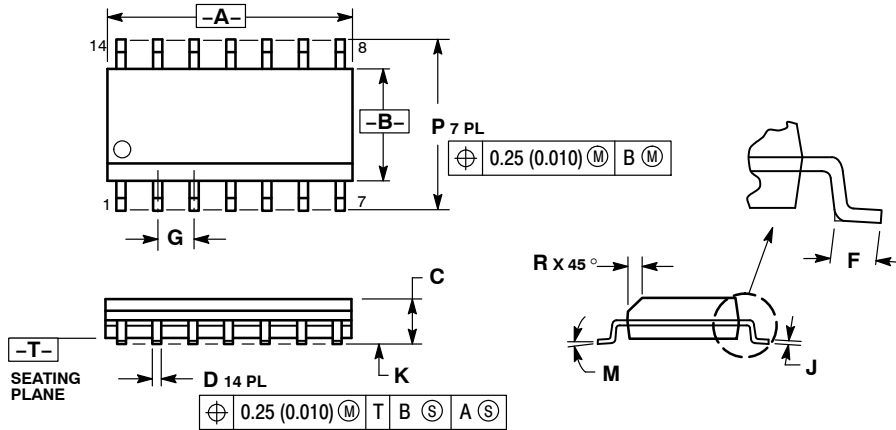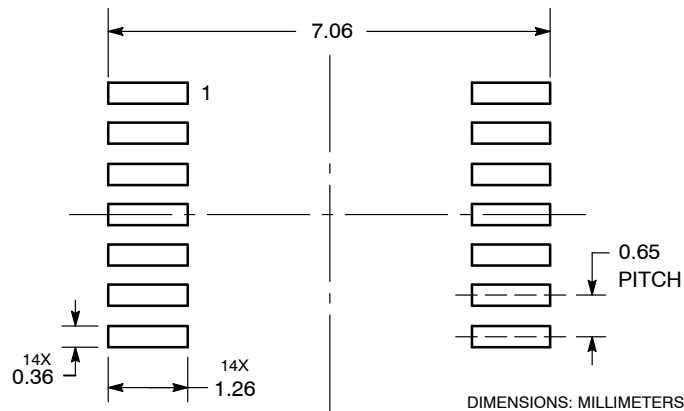
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*
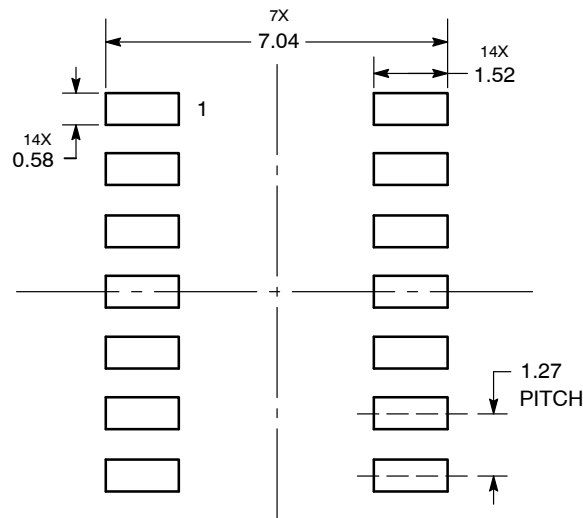
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HCT132A

PACKAGE DIMENSIONS

TSSOP−14
CASE 948G−01
ISSUE B
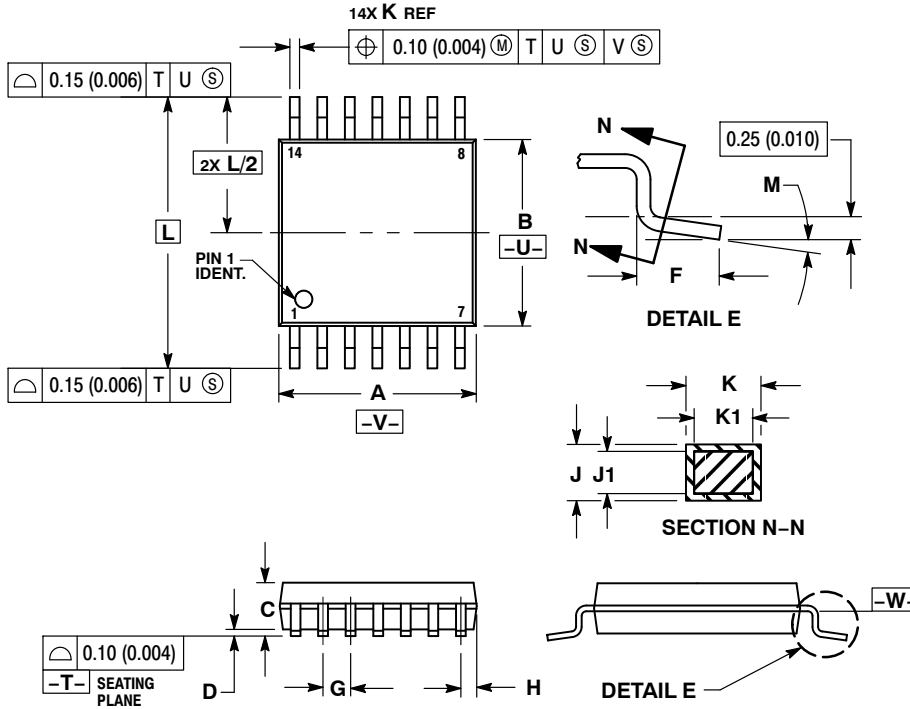
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC74HCT132A

PACKAGE DIMENSIONS

SOEIAJ–14
CASE 965–01
ISSUE B
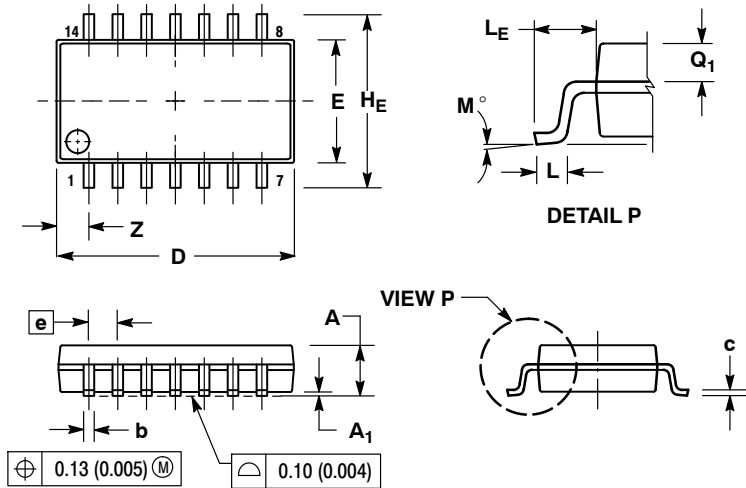
DETAIL P

VIEW P

⊕ 0.13 (0.005) Ⓜ   △ 0.10 (0.004)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	---	2.05	---	0.081
A$_1$	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H$_E$	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L$_E$	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q$_1$	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

PUBLICATION ORDERING INFORMATION

MC74HCT132A/D