

# LC717A10ARGPGEVB

## Capacitance-Digital-Converter LSI for Electrostatic Capacitive Touch Sensors Evaluation Board User's Manual



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

### EVAL BOARD USER'S MANUAL

#### Introduction

This manual contains configuration, usage and main specifications regarding Electrostatic Capacitive Touch Sensor Evaluation Board (LC717A10ARGPGEVB).

For the latest edition of this manual, please refer to ON Semiconductor homepage. (<http://www.onsemi.com>)

#### Product Outline

This product is a board that can be used to evaluate LSI "LC717A10AR". Due to the fact it is 600 mil wide DIP shape, it is easy to use. It can be set up to evaluate any given touch switch pattern.

In order for evaluation, it is necessary to obtain an USB-to-Serial conversion module for SPI communication, a PC to evaluate software, and a board with a designed switch pattern.

- Electrostatic Capacitive Touch Sensor Evaluation Board LC717A10ARGPGEVB
- Accessory Connector Pin (8pin)

### EVALUATION BOARD

#### LC717A10ARGPGEVB Evaluation Board Outline

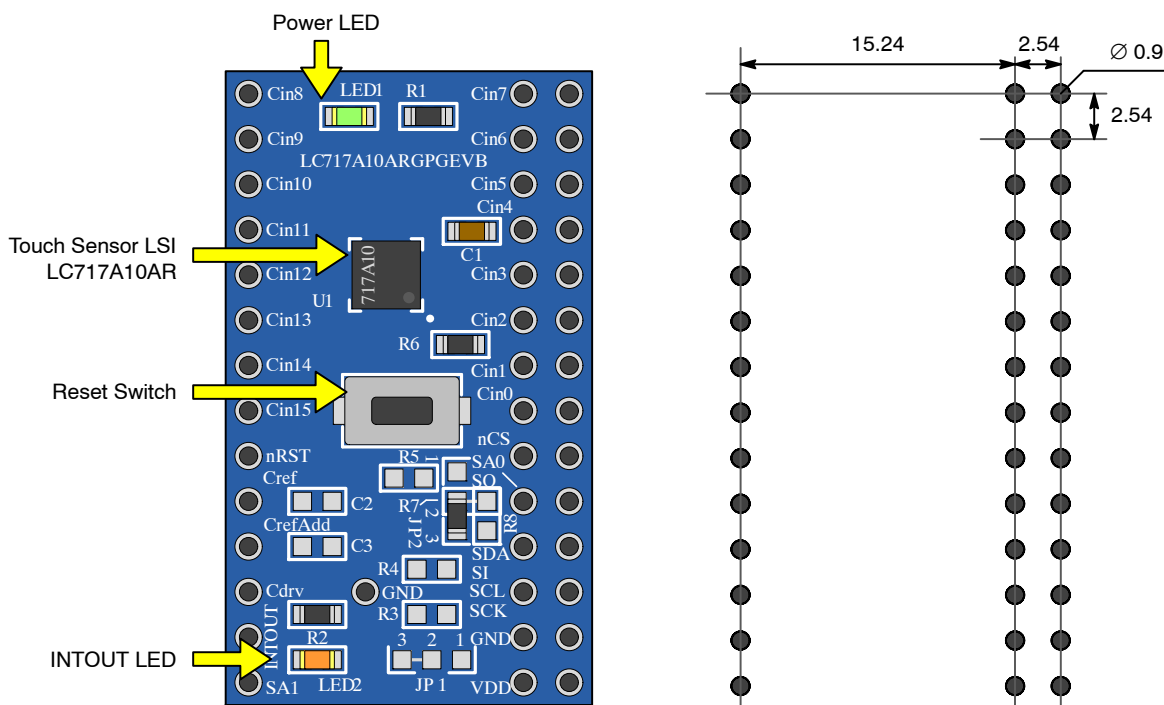


Figure 1. Configuration of LC717A10ARGPGEVB

## LC717A10ARGPGEVB

- **Touch Sensor LSI:**  
Electrostatic Capacitive Touch Sensor LSI  
LC717A10AR
- **Power LED:**  
When a power is supplied, it turns on. Power supply voltage is 2.6 to 5.5 V.
- **Reset Switch:**  
This is used to RESET Touch Sensor LSI. Use this switch if any abnormality is encountered during operation.
- **INTOUT LED:**  
When the INTOUT signal outputs, it turns on.

### Evaluation Board Specifications

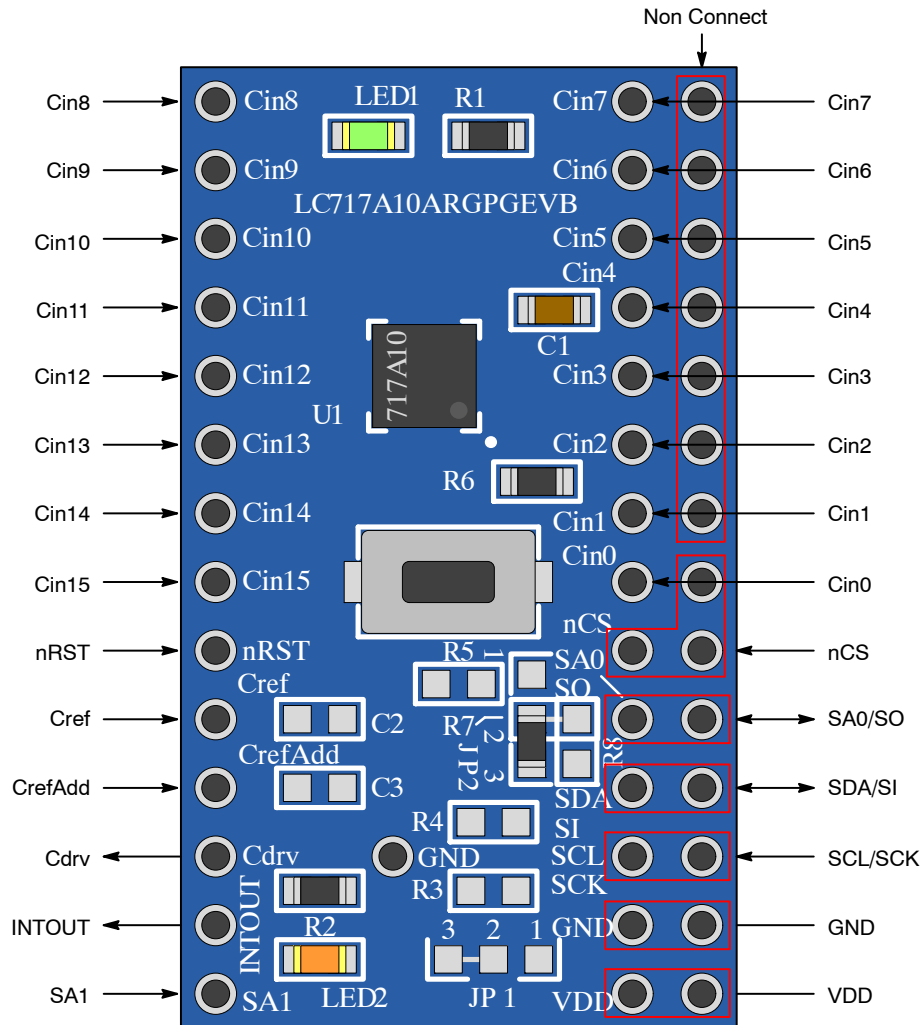


Figure 2. Terminal Pin Layout

# LC717A10ARGPGEVB

**Table 1. SIGNAL PIN FUNCTIONS**

| Pin Name | I/O | Pin Functions                                                                               |
|----------|-----|---------------------------------------------------------------------------------------------|
| Cin0     | I/O | Capacitance Sensor Input                                                                    |
| Cin1     | I/O | Capacitance Sensor Input                                                                    |
| Cin2     | I/O | Capacitance Sensor Input                                                                    |
| Cin3     | I/O | Capacitance Sensor Input                                                                    |
| Cin4     | I/O | Capacitance Sensor Input                                                                    |
| Cin5     | I/O | Capacitance Sensor Input                                                                    |
| Cin6     | I/O | Capacitance Sensor Input                                                                    |
| Cin7     | I/O | Capacitance Sensor Input                                                                    |
| Cin8     | I/O | Capacitance Sensor Input                                                                    |
| Cin9     | I/O | Capacitance Sensor Input                                                                    |
| Cin10    | I/O | Capacitance Sensor Input                                                                    |
| Cin11    | I/O | Capacitance Sensor Input                                                                    |
| Cin12    | I/O | Capacitance Sensor Input                                                                    |
| Cin13    | I/O | Capacitance Sensor Input                                                                    |
| Cin14    | I/O | Capacitance Sensor Input                                                                    |
| Cin15    | I/O | Capacitance Sensor Input                                                                    |
| Cref     | I/O | Reference Capacitance Input                                                                 |
| CrefAdd  | I/O | Reference Capacitance Input for Addition                                                    |
| Cdrv     | O   | Output for Capacitance Sensors Drive                                                        |
| INTOUT   | O   | Interrupt Output                                                                            |
| SCL/SCK  | I   | Clock Input (I <sup>2</sup> C)/Clock Input (SPI)                                            |
| nCS      | I   | Interface Selection/Chip Select Inverting Input (SPI)                                       |
| nRST     | I   | External Reset Signal Inverting Input (2.2 k $\Omega$ Pull-up, with Switch)                 |
| SA1      | I   | Slave Address Selection (I <sup>2</sup> C)                                                  |
| SDA/SI   | I/O | Data Input and Output (I <sup>2</sup> C)/Data Input (SPI)                                   |
| SA0/SO   | I/O | Slave Address Selection (I <sup>2</sup> C)/Data Output (SPI) (JP2 100 k $\Omega$ Pull-down) |
| VDD      | –   | Power Supply (2.6 V to 5.5 V). It is Connected to V <sub>DD</sub> of LC717A10AR             |
| GND      | –   | Ground (Earth). It is Connected to V <sub>SS</sub> of LC717A10AR                            |

**Table 2. MAIN SPECIFICATIONS**

| Parameter                   | Conditions         | Remarks                                                               |
|-----------------------------|--------------------|-----------------------------------------------------------------------|
| Board Size                  | 35.56 × 20.32 (mm) |                                                                       |
| Board Material              | Glass Epoxy (FR4)  | Copper Foil: 35 $\mu$ m, Thickness: 1.6 mm, 2-layer Board             |
| Supply Voltage              | 2.6 to 5.5 V       |                                                                       |
| Capacitance Touch Sensor    | LC717A10AR         |                                                                       |
| Communication Specification | SPI                | It can be change to I <sup>2</sup> C Compatible Bus by Parts Exchange |

# LC717A10ARGPEVB

**Table 3. JUMPER, PATTERN FOR ADDITIONAL PARTS**

| Pattern | Parameter                                                                        | Set Contents                                                                                                                                                                                                                                                                                                            |
|---------|----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C2      | Pattern for Cref Capacity Adjustment                                             | Implement capacitor of any capacity as needed. (Size: 1608)                                                                                                                                                                                                                                                             |
| C3      | Pattern for CrefAdd Capacity Adjustment                                          | Implement capacitor of any capacity as needed. (Size: 1608)                                                                                                                                                                                                                                                             |
| R3      | Pattern for SCL Pull-up                                                          | When I <sup>2</sup> C compatible bus is chosen by nCS, implement a resistance of 2.2 k $\Omega$ . (Size: 1608) (Pull-up VDD)                                                                                                                                                                                            |
| R4      | Pattern for SDA Pull-up                                                          | When I <sup>2</sup> C compatible bus is chosen by nCS, implement a resistance of 2.2 k $\Omega$ . (Size: 1608) (Pull-up VDD)                                                                                                                                                                                            |
| R5      | Pattern for nCS Pull-up                                                          | When I <sup>2</sup> C compatible bus is chosen by nCS, implement a resistance of 2.2 k $\Omega$ . (Size: 1608) (Pull-up VDD)                                                                                                                                                                                            |
| R7      | Reserve Pattern                                                                  | (R7 Initialization: Short) (Size: 1608)                                                                                                                                                                                                                                                                                 |
| R8      | Reserve Pattern                                                                  | (R8 Initialization: Open) (Size: 1608)                                                                                                                                                                                                                                                                                  |
| JP1     | Pattern for I <sup>2</sup> C Compatible Bus Slave Address Selection              | When I <sup>2</sup> C compatible bus is chosen by nCS, set the I <sup>2</sup> C compatible bus slave address by JP1 and JP2. When SPI is chosen, connect to the ground.<br>(JP1 Initialization: Ground Short)<br>1–2 Short: H Level<br>2–3 Short: L Level                                                               |
| JP2     | Pattern for I <sup>2</sup> C Compatible Bus Slave Address Selection/SO Pull-down | When I <sup>2</sup> C compatible bus is chosen by nCS, set the I <sup>2</sup> C compatible bus slave address by JP1 and JP2. When SPI is chosen, implement a resistance of 100 k $\Omega$ between 2 to 3. (It has been implemented.) (JP2 Initialization: Ground Pull-down)<br>1–2 Short: H Level<br>2–3 Short: L Level |

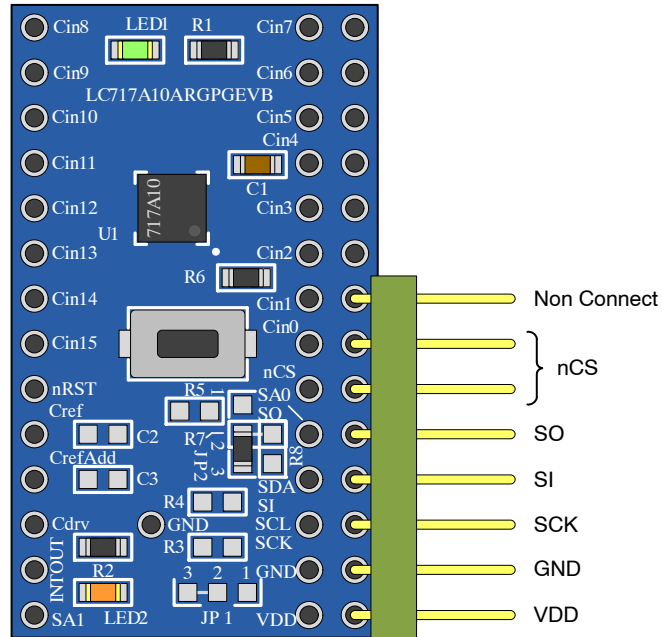
**Table 4. LC717A10AR I<sup>2</sup>C COMPATIBLE BUS SLAVE ADDRESS**

| SA1 Input (JP1) | SA0 Input (JP2) | 7bit Slave Address | Binary Notation   | 8bit Slave Address |
|-----------------|-----------------|--------------------|-------------------|--------------------|
| Low             | Low             | 0x16               | 00101100b (Write) | 0x2C               |
|                 |                 |                    | 00101101b (Read)  | 0x2D               |
| Low             | High            | 0x17               | 00101110b (Write) | 0x2E               |
|                 |                 |                    | 00101111b (Read)  | 0x2F               |
| High            | Low             | 0x18               | 00110000b (Write) | 0x30               |
|                 |                 |                    | 00110001b (Read)  | 0x31               |
| High            | High            | 0x19               | 00110010b (Write) | 0x32               |
|                 |                 |                    | 00110011b (Read)  | 0x33               |

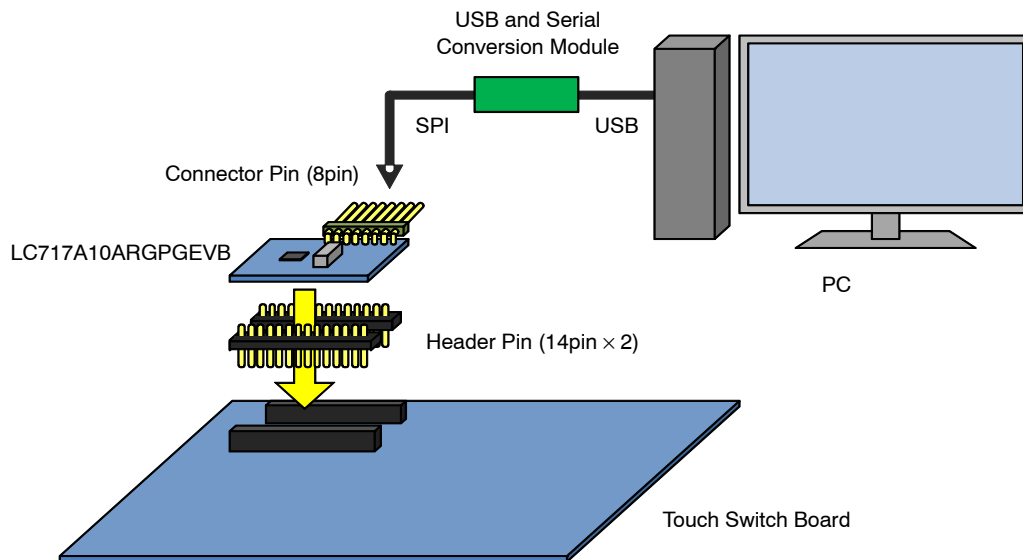
## HOW TO USE

1. Connection of connector pin.  
Solder attached connector pin (8pin) at the position pictured in Figure 3.
2. Connect the LC717A10ARGPEVB to a board with a designed switch pattern. When designing a switch pattern, please refer to the Application and Design Note on the [ON Semiconductor Touch Sensor Homepage](#).
3. Connect LC717A10ARGPEVB to PC through an USB-to-Serial conversion module. Supply the power, and verify the Power LED is turned on.
4. Install evaluation software to PC. The evaluation software is available from the [ON Semiconductor Homepage](#), and selecting “LC717A10 software”. Double-click on the icon “LC717A10App.exe” from the installed folder and start it.
5. Press RESET Switch when evaluation board is acting strange.
6. Please note: If the user directly touches the LSI on the evaluation board or patterns with their finger, it may cause malfunction or breakdown.

# LC717A10ARGPGEVB



**Figure 3. Connection of Connector Pin**



(Other than LC717A10ARGPGEVB and Connector Pin (8pin) are not Attached.)

**Figure 4. Connection Example of LC717A10ARGPGEVB**

# LC717A10ARGPGEVB

## CIRCUIT DIAGRAMS

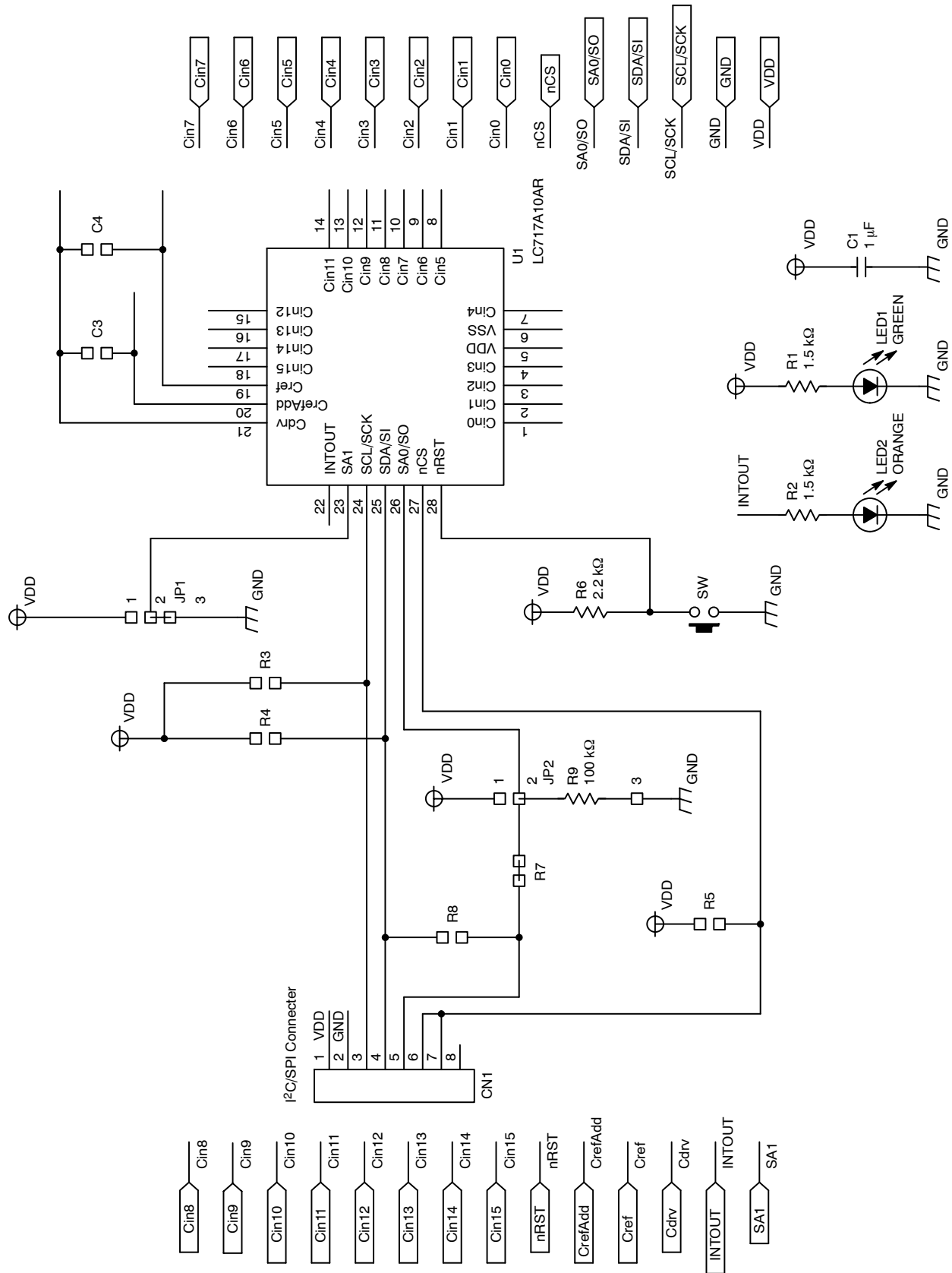


Figure 5. Circuit Diagrams

# LC717A10ARGPGEVB

## PRECAUTION FOR USE

For approach in the use of LSI and design rule of the switch pattern: Please refer to the Application Note and Design Note in [ON Semiconductor Touch Sensor Homepage](#).

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

The evaluation board/kit (research and development board/kit) (hereinafter the "board") is not a finished product and is as such not available for sale to consumers. The board is only intended for research, development, demonstration and evaluation purposes and should as such only be used in laboratory/development areas by persons with an engineering/technical training and familiar with the risks associated with handling electrical/mechanical components, systems and subsystems. This person assumes full responsibility/liability for proper and safe handling. Any other use, resale or redistribution for any other purpose is strictly prohibited.

The board is delivered "AS IS" and without warranty of any kind including, but not limited to, that the board is production-worthy, that the functions contained in the board will meet your requirements, or that the operation of the board will be uninterrupted or error free. ON Semiconductor expressly disclaims all warranties, express, implied or otherwise, including without limitation, warranties of fitness for a particular purpose and non-infringement of intellectual property rights.

ON Semiconductor reserves the right to make changes without further notice to any board.

You are responsible for determining whether the board will be suitable for your intended use or application or will achieve your intended results. Prior to using or distributing any systems that have been evaluated, designed or tested using the board, you agree to test and validate your design to confirm the functionality for your application. Any technical, applications or design information or advice, quality characterization, reliability data or other services provided by ON Semiconductor shall not constitute any representation or warranty by ON Semiconductor, and no additional obligations or liabilities shall arise from ON Semiconductor having provided such information or services.

The boards are not designed, intended, or authorized for use in life support systems, or any FDA Class 3 medical devices or medical devices with a similar or equivalent classification in a foreign jurisdiction, or any devices intended for implantation in the human body. Should you purchase or use the board for any such unintended or unauthorized application, you shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the board.

This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and may not meet the technical requirements of these or other related directives.

**FCC WARNING** – This evaluation board/kit is intended for use for engineering development, demonstration, or evaluation purposes only and is not considered by ON Semiconductor to be a finished end product fit for general consumer use. It may generate, use, or radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment may cause interference with radio communications, in which case the user shall be responsible, at its expense, to take whatever measures may be required to correct this interference.

ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**LIMITATIONS OF LIABILITY:** ON Semiconductor shall not be liable for any special, consequential, incidental, indirect or punitive damages, including, but not limited to the costs of requalification, delay, loss of profits or goodwill, arising out of or in connection with the board, even if ON Semiconductor is advised of the possibility of such damages. In no event shall ON Semiconductor's aggregate liability from any obligation arising out of or in connection with the board, under any theory of liability, exceed the purchase price paid for the board, if any.

For more information and documentation, please visit [www.onsemi.com](http://www.onsemi.com).

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative