

UM12420

ARA2-M2-16G-GT Board User Manual

Rev. 3.0 — 1 July 2026

User manual

Document information

Information	Content
Keywords	Ara240 16 GB M.2 Module, Ara240, M.2 accelerator card, M.2 module, Discrete Neural Processing Unit (DNPU), NPU, AI accelerator, AI, Generative AI, ARA2-M2-16G-GT, UM12420
Abstract	The Ara240 16 GB M.2 Module (ARA2-M2-16G-GT) is a hardware platform for evaluation and deployment of AI workloads at the edge. It uses the Ara240 AI processor and follows the M.2 M-key 2280 form factor.

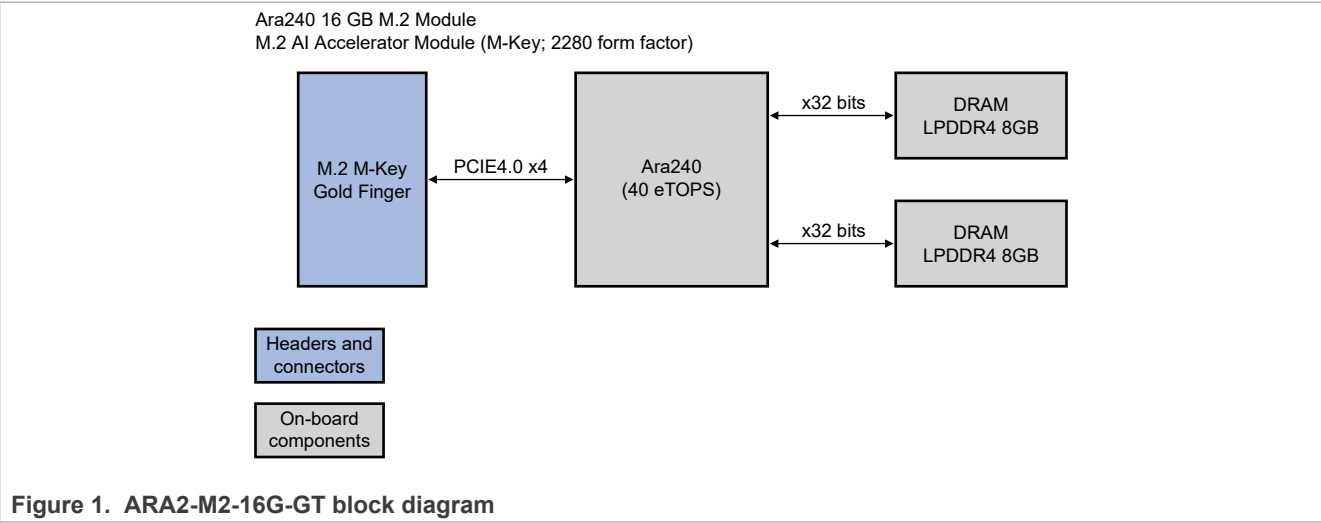


1 Overview

The Ara240 16 GB M.2 Module (ARA2-M2-16G-GT) is a high-performance AI accelerator module dedicated for Edge AI applications. The Ara240 AI processor delivers up to 40 eTOPS, with 16 GB LPDDR4 memory. This configuration allows edge devices with a host microprocessor to deploy a wide variety of AI workloads with a heavy memory footprint.

1.1 Block diagram

Figure 1 shows the ARA2-M2-16G-GT block diagram.



1.2 Board features

Table 1 lists the ARA2-M2-16G-GT features.

Table 1. ARA2-M2-16G-GT features

Board feature	Target processor feature used	Description
Ara240 AI processor		Ara240 Discrete Neural Processing Unit (DNPU), a second-generation AI accelerator built for low-latency and low-power edge applications
LPDDR4 memory	LPDDR4 controller	16 GB LPDDR4 SDRAM (2x 8 GB configuration)
M.2 M-key gold finger		M.2 M-key gold finger edge connector, supporting up to PCIe 4.0 x4
SPI interface	SPI controller	SPI NOR flash memory
Debug interface		5x Test points reserved for soldering JTAG probe
Power		3V3 provided through M.2 connector; reserved 5 V pinout for alternative power option
Mounting slot		For securing in place when installed on the host device
Orderable part number		ARA2-M2-16G-GT

1.3 Kit contents

Table 2 lists the items included in the ARA2-M2-16G-GT kit.

Table 2. Kit contents

Item	Quantity
ARA2-M2-16G-GT board	1
M2.5 screw	1
M3 screw	1

1.4 Board pictures

Figure 2 shows the top-side view of ARA2-M2-16G-GT.



Figure 2. ARA2-M2-16G-GT top-side view

Figure 3 shows the bottom-side view of ARA2-M2-16G-GT.

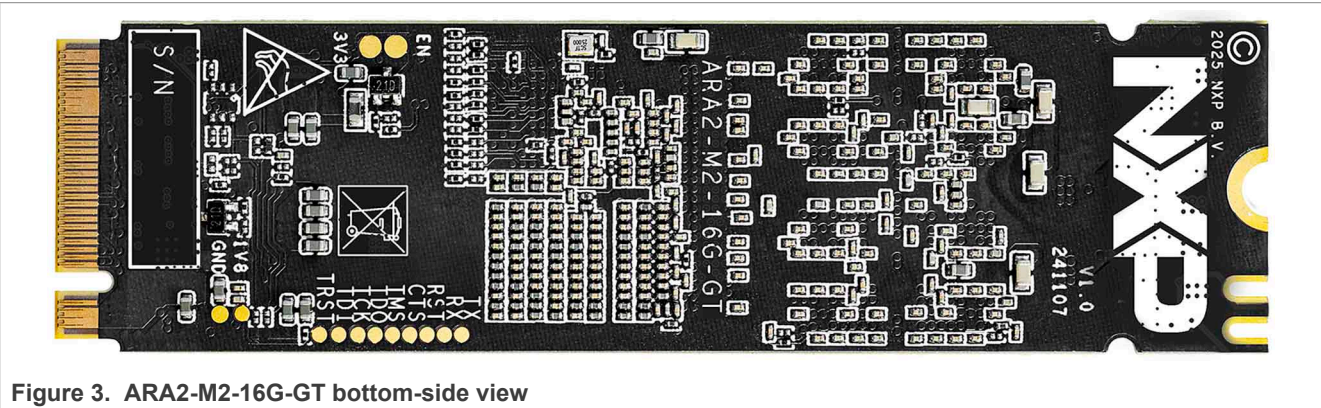


Figure 3. ARA2-M2-16G-GT bottom-side view

1.5 Connectors

Figure 4 shows the connectors at top-side of ARA2-M2-16G-GT.

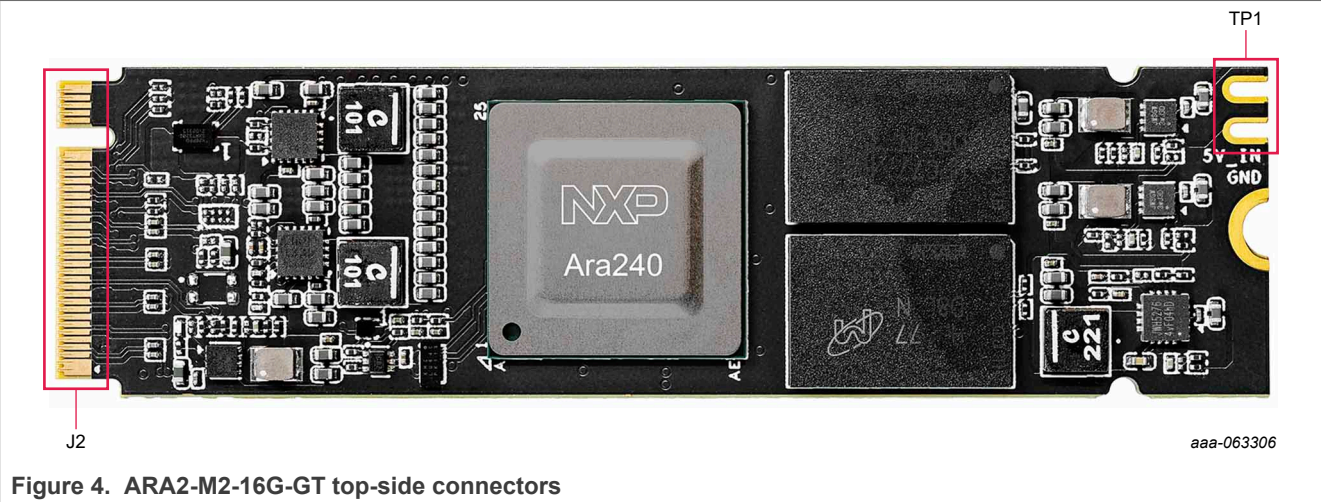


Figure 4. ARA2-M2-16G-GT top-side connectors

Figure 5 shows the connectors at bottom-side of ARA2-M2-16G-GT.

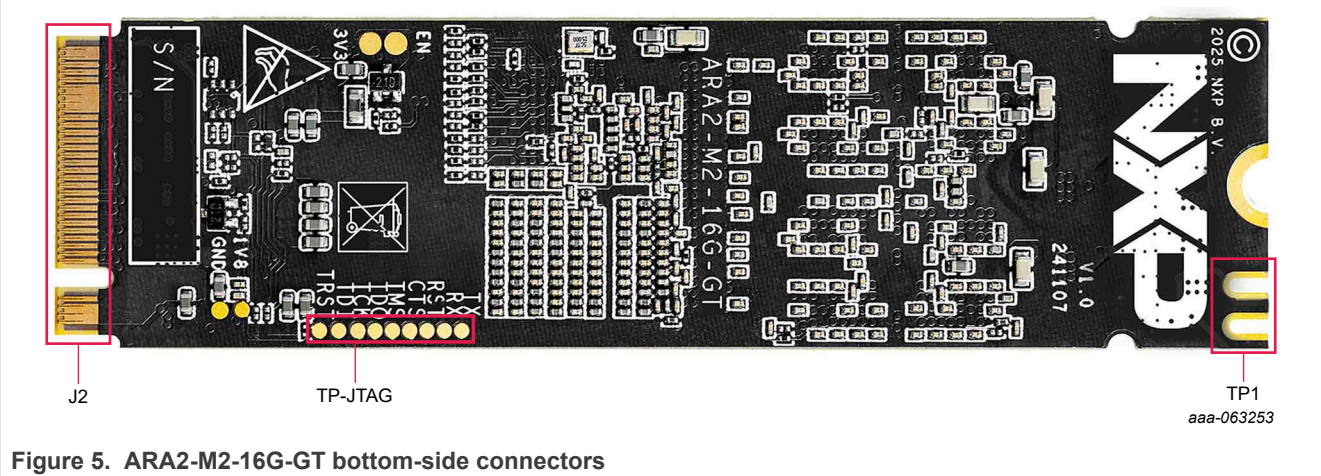


Figure 5. ARA2-M2-16G-GT bottom-side connectors

Figure 4 and Figure 5 label the connectors available on the ARA2-M2-16G-GT.

Table 3. ARA2-M2-16G-GT connectors

Part identifier	PCB label	Connector type	Description	Reference section
J2		M.2 gold finger	M.2 M-key edge connector	Section 2.7
TP1	5V_IN	Edge solder pad	Auxiliary 5 V input	Section 2.2
TP-JTAG		Test point pad	JTAG	Section 2.9

1.6 LED

ARA2-M2-16G-GT provides a Light-Emitting Diodes (LED) for indicating the module power status. The information collected from the LED can be used for debugging purposes.

Figure 6 shows the ARA2-M2-16G-GT LED. The LED is placed on the ARA2-M2-16G-GT top-side.



Table 4 describes the ARA2-M2-16G-GT LED.

Table 4. ARA2-M2-16G-GT LED

Part identifier	LED color	Name/function	Description (when LED is ON)
D1	Green	M.2 card power good indicator	The ARA2-M2-16G-GT board (M.2 card) has received power correctly and is in a stable power on state. When D1 turns on, it indicates that the module is powered and ready for operation.

2 Functional description

This section includes the following subsections:

- [Section "Processor"](#)
- [Section "Board power supply"](#)
- [Section "Clocks"](#)
- [Section "LPDDR4 memory"](#)
- [Section "SPI interface"](#)
- [Section "Sensor"](#)
- [Section "M.2 connector"](#)
- [Section "Fan connector"](#)
- [Section "JTAG"](#)
- [Section "EEPROM"](#)

2.1 Processor

The Ara240 processor is a high-performance, high-efficiency, proprietary deep learning accelerator processor. It is a complex processor composed of multiple task-oriented processing units to enable low latency inferencing at low power with minimal data movement. The processor features a Secure Boot Processor and a Management and Control Processor (MCP). These two processors combine to enable the secure mode feature of the Ara240 processor, ensuring system security in complex environments.

For the Ara240 processor, there are two Neural Network Processor (NNP) clusters with four NNPs in each cluster, each NNP operating up to 900 MHz. These NNPs are flexible and robust and are designed to run a custom instruction set specialized for deep learning algorithms. This instruction-set-based design enables the NNP to adapt to different ML algorithms and frameworks, such as CNNs, RNNs, and transformer-based models, such as LLMs or VLMs.

The Ara240 processor has its own dedicated 64-bit LPDDR4 controller to allow the AI processor to access memory and data quickly. The LPDDR caches ML models so the AI processor accesses required resources directly with minimal involvement from the host platform. The addressable memory space is up to 16 GB in a 64-bit configuration (2x 32-bit 8 GB LPDDR4). This space is sufficient for deploying AI workloads with a heavy memory footprint such as LLMs (up to 8 billion parameters).

Note: Convert and quantize the Models to Ara240-supported format before deployment.

For more information regarding the Ara240 processor, refer to the documents mentioned in [Section 3](#).

2.2 Board power supply

The ARA2-M2-16G-GT operates at full performance by solely powering with 3V3 input from the M.2 edge connector. Upon receiving a stable power supply, the M.2 module automatically initiates the power sequence for the Ara240 AI processor. The power good LED (LED1) turns on, indicating the power on the M.2 module has reached a stable state.

[Figure 7](#) shows the ARA2-M2-16G-GT power supply diagram.

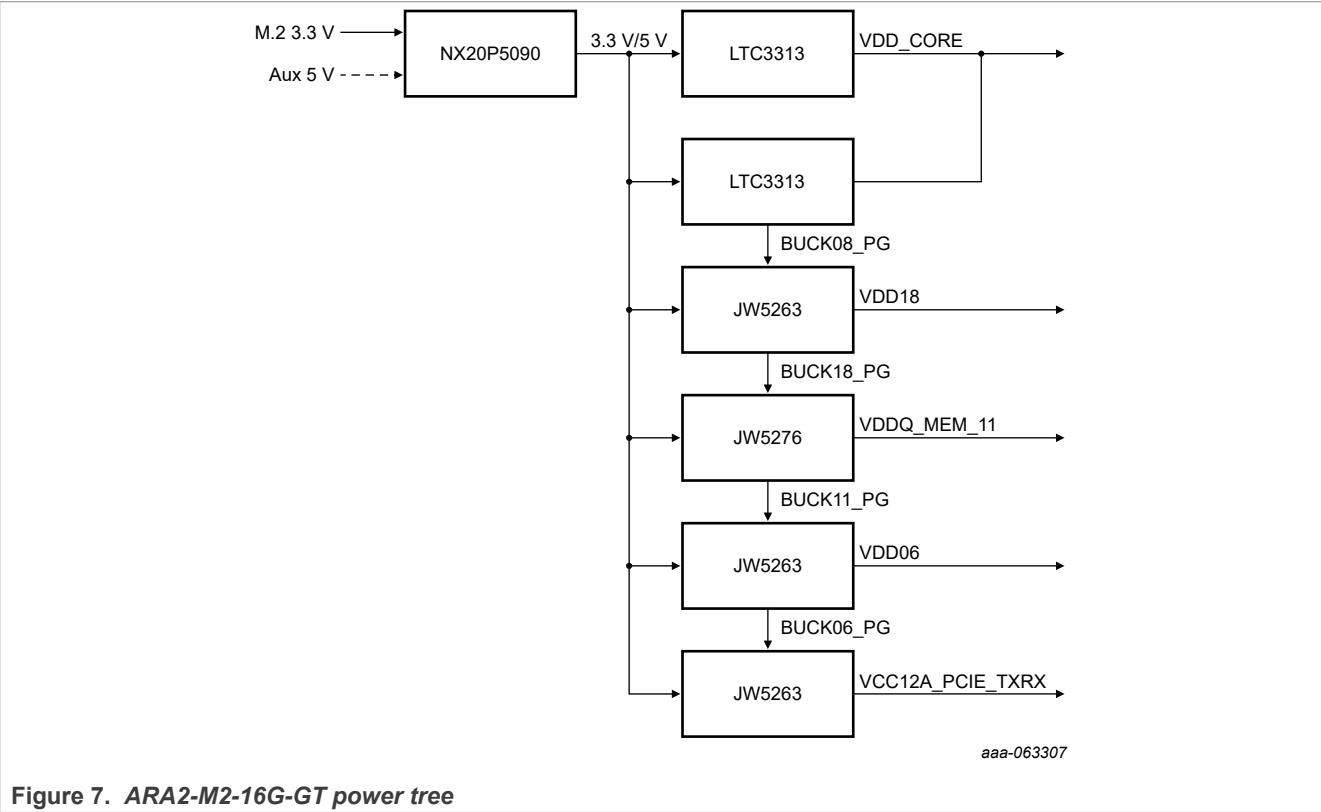


Figure 7. ARA2-M2-16G-GT power tree

[Table 5](#) describes ARA2-M2-16G-GT power supplies.

Note: Unless specified explicitly, the part identifiers mentioned in [Table 5](#) correspond to the ARA2-M2-16G-GT.

Table 5. ARA2-M2-16G-GT power supplies

Power source	Manufacturer and part number	Power supply	Description
M.2 3V3	-	3V3	Primary power supply of the module. It is provided from M.2.

Table 5. ARA2-M2-16G-GT power supplies...continued

Power source	Manufacturer and part number	Power supply	Description
Aux 5 V	-	5V0	Auxiliary 5 V power supply for system that cannot fulfill the Ara240 16 GB M.2 module power demand through M.2 connection.
Power switch NX20 P5090	NXP semiconductors NX20P5090UKAZ	3V3/5V0	Power switch for switching path between primary 3V3 input and auxiliary 5 V input.
LTC3313 (VDD_CORE)	Analog devices LTC3313JV#PBF	3V3/5V0	Provides 0.8 V to VDD_CORE and VDD_OP8 domain of Ara240 processor.
JW5263 (VDD18)	Joulwatt JW5263SL	3V3/5V0	Provides 1.8 V to VDD_1P8 domain of the Ara240 processor, and VDD1 domain of LPDDR4.
JW5263 (VDDQ_MEM_11)	Joulwatt JW5263SL	3V3/5V0	Provides 1.1 V to VDDQX domain of the Ara240 processor and VDD2 domain of LPDDR4.
JW5263 (VDD06) ^[1]	Joulwatt JW5263SL	3V3/5V0	Provides 1.1 V to VDDQ domain of the Ara240 processor and VDDQ domain of LPDDR4.
JW5263 (VCC12A_PCIE_TXRX)	Joulwatt JW5263SL	3V3/5V0	Provides 1.2 V to VDD_1P2 domain of the Ara240 processor.

[1] Power rail VDD06 is hardware-configured to output 1.1 V for operation of LPDDR4 by default.

2.3 Clocks

ARA2-M2-16G-GT provides the necessary clock on-module. No external clock source is needed for operating the module. [Table 6](#) provides details about the clock available on ARA2-M2-16G-GT.

Table 6. ARA2-M2-16G-GT clock

Clock generator	Clock	Frequency	Destination
Quartz crystal X1	XTALIN/XTAL_OUT	25 MHz	25 MHz clock for the Ara240 processor

2.4 LPDDR4 memory

The Ara240 AI processor integrates a dedicated LPDDR4 controller that supports up to 16 GB of LPDDR4 in a 64-bit configuration.

In the ARA2-M2-16G-GT module, the LPDDR4 controller connects to two 8 GB LPDDR4 DRAM devices and operates in LPDDR4 mode by default.

The DRAM chips are placed on the top side of the board.

Custom DDR pin swapping is not supported. Customer designs must use the same signal mapping as the reference design and replicate the DDR layout from the reference design.

The LPDDR4 chips in the ARA2-M2-16G-GT module use a 240 Ω 1% resistor for ZQ calibration.

To modify LPDDR timings or On-Die Termination (ODT) settings, contact your local Field Application Engineer (FAE).

2.5 SPI interface

The Ara240 processor features a 1.8 V Serial Peripheral Interface (SPI) controller, which can connect to an external SPI memory/flash device for storing AI processor firmware. The SPI interface of the Ara240 processor supports up to 32 MB Flash devices, in single or quad configuration.

On the ARA2-M2-16G-GT board, an SPI flash has been used to store a copy of the boot image for the Ara240 processor.

[Table 7](#) describes the SPI memories available on the Ara240 16 GB M.2 module.

Table 7. SPI memories

SPI controller	Processor domain	SPI memory		
		Part identifier	Manufacturer and part number	Description
SPI	VDD_1P8	U8	XMC XM25LU64CVIQT	64-Mbit, 1.8 V serial flash memory with Dual/Quad SPI and QPI/DTR

2.6 Sensor

On ARA2-M2-16G-GT, a temperature sensor (TMP102AIDRLR) has been used to monitor the temperature and state of the module. It is connected to the Ara240 processor I2C interface by default.

2.7 M.2 connector

The ARA2-M2-16G-GT board has a 75-pin M-key gold finger edge connector (J2).

[Table 8](#) explains the M.2 connector pinout.

Table 8. M.2 connector pinout

Pin numbers	Signal name	Connection details
5/7	P_TXN3/P_TXP3	PCIe transceiver lane 3 differential pair
11/13	P_RXN3/P_RXP3	PCIe receiver lane 3 differential pair
17/19	P_TXN2/P_TXP2	PCIe transceiver lane 2 differential pair
23/25	P_RXN2/P_RXP2	PCIe receiver lane 2 differential pair
29/31	P_TXN1/P_TXP1	PCIe transceiver lane 1 differential pair
35/37	P_RXN1/P_RXP1	PCIe receiver lane 1 differential pair
41/43	P_TXN0/P_TXP0	PCIe transceiver lane 0 differential pair
47/49	P_RXN0/P_RXP0	PCIe receiver lane 0 differential pair
53/55	P_REFCLKN/P_REFCLKP	PCIe reference clock differential pair
40	ARA2_I2C_SCL_1V8	ARA2_I2C_SCL_1V8 ^[1]
42	ARA2_I2C_SDA_1V8	ARA2_I2C_SDA_1V8 ^[1]
50	PCIE_PERST#	M.2 PCIe interface reset signal
52	P_CLKREQ#	M.2 PCIe clock request signal
56	I2C_SDA_3V3	M.2 management bus data signal ^[1]
58	I2C_SCL_3V3	M.2 management bus clock signal ^[1]
2,4,12,14,16,18,70,72,74	3V3	M.2 3V3 power input

Table 8. M.2 connector pinout...continued

Pin numbers	Signal name	Connection details
1, 3, 9, 15, 21, 27, 33, 39, 45, 51, 57,71,75	GND	M.2 module GND

[1] DNP by default.

2.8 Fan connector

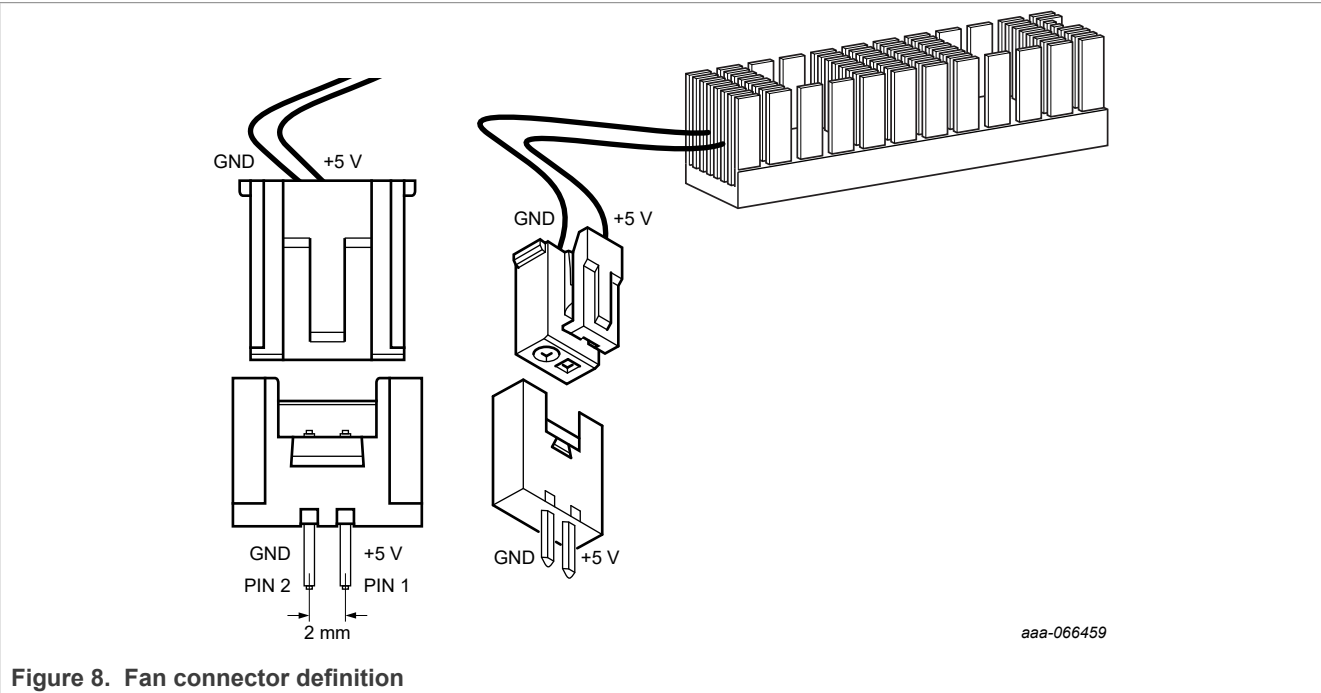
The ARA2-M2-16G-GT module requires that the motherboard provides a 2-pin fan connector to power an external cooling fan. The pin assignment must be defined as follows:

Table 9. Fan connector pin definition

Pin number	Signal name	Description
Pin 1	VCC (+5 V)	+5 V power supply
Pin 2	GND	Ground

Note:

- Ensure that the connected fan is rated for 5 V operation before use.
- Verify the polarity of the connector before plugging in the fan cable.
- Reversing VCC and GND may damage the fan or the motherboard.



2.9 JTAG

ARA2-M2-16G-GT provides auxiliary test points for debugging. To use these test points, solder wires directly onto the pads or probe with pogo pins with respect to pins arrangement. For more information regarding the use of JTAG on the Ara240 processor, contact your local FAE.

2.10 EEPROM

ARA2-M2-16G-GT provides a memory placeholder EEPROM for holding crucial data for the Ara240 processor. The EEPROM is connected to the I2C interface from the Ara240 processor by default.

This EEPROM can be used to store the following board information:

- Board ID and revision
- SoC ID and revision
- Firmware ID and revision
- Board serial number

The EEPROM has been preprogrammed during manufacture, such that the ARA2-M2-16G-GT can be plugged and used without further configuration by the user. User can reconfigure the data stored in EEPROM with careful handling. To ensure the sanity of the firmware and functional safety of the system, however, it is not suggested for users to modify the EEPROM directly.

3 Related documentation

[Table 10](#) lists and explains the additional documents and resources that you can refer to for more information on the board. Some of the documents listed below may be available only under a Non-Disclosure Agreement (NDA). To request access to these documents, contact your local FAE or sales representative.

Table 10. Related documentation

Document	Description	Link / how to obtain
Ara240 Discrete Neural Processing Unit Data Sheet - Industrial	Provides information about electrical characteristics, hardware design consideration, and features.	ARA240IND
ARA2-M2-16G-GT design files	Provides an application circuit diagram and design example. Schematic and Layout.	ARA2-M2-16G-GT-DESIGN-FILES
Ara240 Hardware Design Guide	Provides layout design guidelines for DDR interfaces, including routing strategies, signal integrity considerations.	Requires NDA, contact your local FAE/Sales
Ara240 SDK Release	Provides tools for rapid development and deployment of Neural Networks on Ara1 and Ara2 processors. It includes optimization, quantization, compilation, and runtime generation utilities.	Requires NDA, contact your local FAE/Sales
Ara240 API documentation	Provides information regarding the usage of API on the Ara240 processor, intended but not limited to software developers and engineers.	Requires NDA, contact your local FAE/Sales

For additional information, refer to [ARA2-M2-16G-GT](#) webpage.

4 Acronyms

[Table 11](#) lists the acronyms used in this document.

Table 11. Acronyms

Acronym	Description
CNN	Convolutional Neural Networks
DNP	Do Not Populate

Table 11. Acronyms...continued

Acronym	Description
DRAM	Dynamic Random-access Memory
DTR	Double Transfer Rate
HS	High-Speed
JTAG	Joint Test Action Group
LED	Light-Emitting Diode
LLM	Large Language Models
LPDDR4	Low-Power Double Data Rate
MAC	Medium Access Control
ML	Machine Learning
NC	Not Connected
PCIe	Peripheral Component Interconnect Express
PMIC	Power Management Integrated Circuit
QPI	Quad Peripheral Interface
RNN	Recurrent Neural Networks
SDRAM	Synchronous Dynamic Random-access Memory
SPI	Serial Peripheral Interface
VLM	Vision Language Models

5 Revision history

[Table 12](#) summarizes the revisions to this document.

Table 12. Revision history

Document ID	Release date	Description
UM12420 v.3.0	1 July 2026	- Updated Section 2.4 - Added Section 2.8 - Updated Table 8 for pins 40 and 42
UM12420 v.2.0	18 March 2026	Initial public release
UM12420 v.1.0	10 February 2026	Initial NDA release

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