36V, 2.5A/3.5A, Fully Integrated Synchronous Buck Converter

MAX42402/MAX42403

General Description

The MAX42402/MAX42403 IC are a tiny synchronous buck converter with integrated high-side and low-side switches. The MAX42402/MAX42403 are designed to deliver up to 2.5A/3.5A with a wide, 4.5V to 36V input voltage range. Voltage quality can be monitored by observing the PGOOD signal. The IC can operate in dropout by running at 99% duty cycle, making it ideal for industrial applications.

The MAX42402/MAX42403 offer externally programmable output voltage. Fixed internal frequency options of 1.5MHz/400kHz are available, which allow for small external components and reduced output ripple.

When SYNC is low, the MAX42402/MAX42403 automatically enter skip mode at light loads with an ultra-low quiescent current of 27uA at no load. A pin-selectable forced-PWM mode is also available, which helps to improve EMI performance. The devices have a spread-spectrum frequency modulation option designed to minimize EMI-radiated emissions due to the modulation frequency.

The MAX42402/MAX42403 are available in a small, 3mm x 3mm FC2QFN package and uses very few external components.

Key Applications

- Industrial Automation
- Point-of-Load
- Distributed DC Power Systems

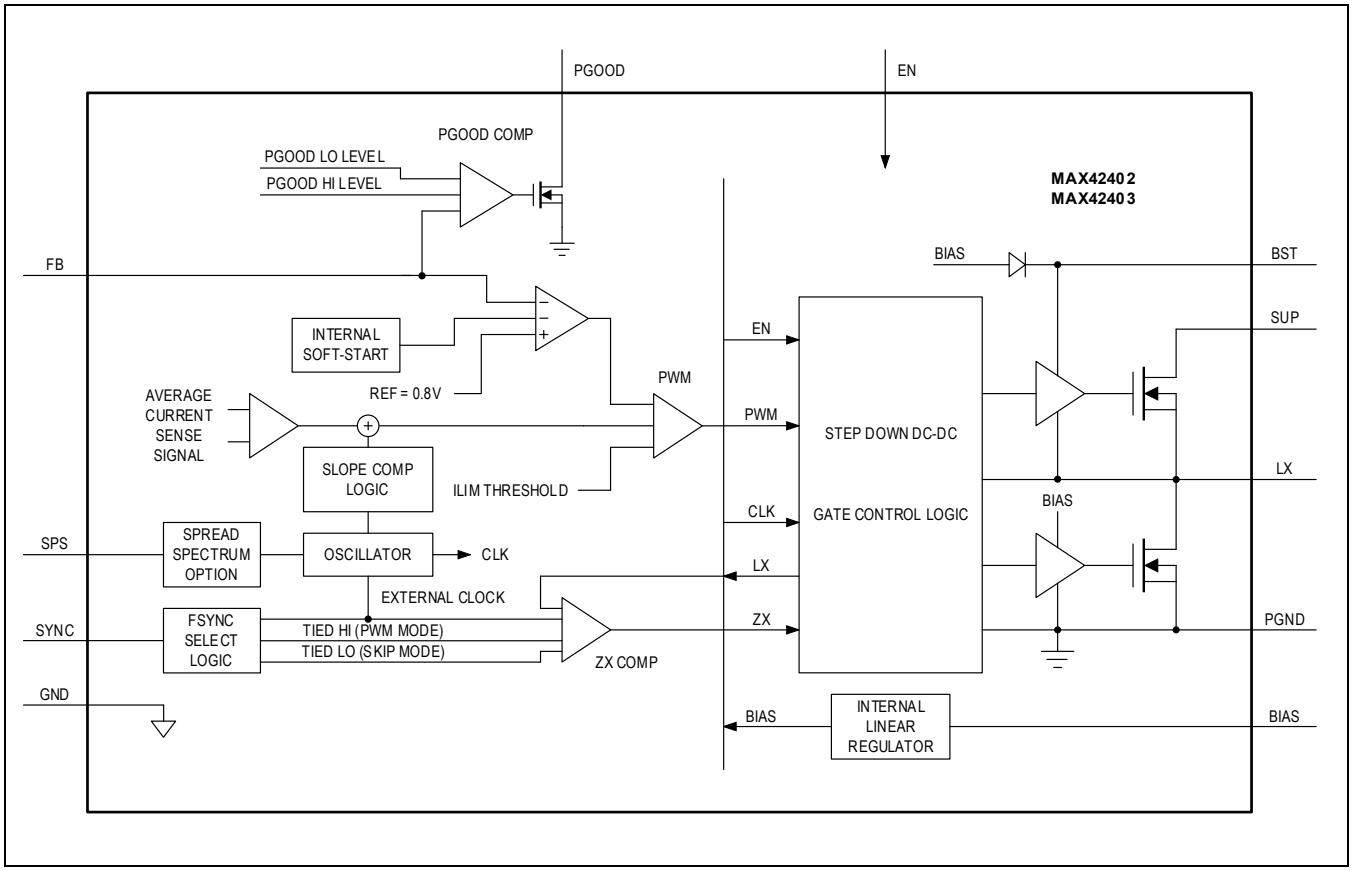
Benefits and Features

- Multiple Functions for Small Size
  - Operating Input Voltage Range: 4.5V to 36V
  - Synchronous DC-DC Converter with Integrated FETs up to 2.5A/3.5A
  - 27µA Quiescent Current in Skip Mode
  - 1.5MHz/400kHz Switching Frequency
  - Spread-Spectrum Option
  - Internal Soft-Start
    - 2.5ms for 400kHz
    - 3.5ms for 1.5MHz
  - Programmable Output Voltage
    - 0.8V to 14V for 400kHz
    - 0.8V to 12V for 1.5MHz
  - 99% Duty Cycle Operation with Low Dropout
- High Precision for Safety-Critical Applications
  - Precision Enable Thresholds for Fully Programmable UVLO Thresholds
  - Accurate Windowed PGOOD
  - Forced-PWM and Skip Operation
  - Overtemperature, Overvoltage, and Short-Circuit Protection
  - 3mm x 3mm FC2QFN
  - -40°C to +125°C Operating Temperature Range
  -

Ordering Information appears at end of data sheet.

19-101726; Rev 3; 3/25

Simplified Block Diagram



Absolute Maximum Ratings

SUP ..... -0.3V to +42V
EN ..... -0.3V to +42V
BST to LX ..... -0.3V to +2.2V
BST ..... -0.3V to +44V
LX ..... -0.3V to SUP+0.3V
SYNC ..... -0.3V to +6V
FB ..... -0.3V to +16V
PGOOD ..... -0.3V to +6V
BIAS ..... -0.3V to +2.2V
SPS ..... -0.3V to +2.2V
PGND to AGND ..... -0.3V to +0.3V
LX Continuous RMS current 3.5A
ESD Protection .....
Human Body Model ..... ±2kV
Charged Device Model ..... ±750V
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 25mW/°C above +70°C.) 2000mW
Operating Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (soldering 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	F153B3F+1F
Outline Number	*21-100701*
Land Pattern Number	*90-100241*
Thermal Resistance, Four-Layer EV Kit:	
Junction to Ambient (θ_{JA})	40°C/W
Junction to Case (θ_{JC})	15°C/W
Thermal Resistance, Four-Layer JEDEC Board:	
Junction to Ambient (θ_{JA})	51°C/W
Junction to Case (θ_{JC})	21°C/W

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the evaluation kit, a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*.

Electrical Characteristics

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. *Note 1* and *Note 2*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		4.5		36	V
		t < 1s			42	
Supply Current	I_{SUP_SHDN}	V_{EN} = 0, T_A = +25°C		2.75	5.00	µA
	I_{SUP}	V_{EN} = high, V_{OUT} = 0.8V, no load, switching, T_A = +25°C		27		
SUP Undervoltage Lockout	$V_{SUP\_UVLO\_RISE}$	SUP voltage rising	2.900	3.025	3.150	V
	$V_{SUP\_UVLO\_FALL}$	SUP voltage falling	2.600	2.725	2.850	
BIAS Voltage	V_{BIAS}			1.8		V
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	BIAS voltage rising	1.58	1.63	1.68	V
BIAS Undervoltage Lockout Hysteresis	$V_{BIAS\_UVLO\_HYS}$	BIAS UVLO hysteresis (*Note 3*)		65		mV
BUCK CONVERTER						
Output Voltage Adjustable Range	V_{OUT}	f_{SW} = 400kHz	0.8		14	V
		f_{SW} = 1.5MHz	0.8		12	
Feedback Voltage Accuracy	V_{FB_PWM}	V_{FB} = 0.8V, PWM mode, no load, T_A = -40°C to +125°C	0.788	0.800	0.812	V
Feedback Leakage Current	I_{FB}	V_{FB} = 0.8V, T_A = +25°C			100	nA
High-Side DMOS On-Resistance	R_{DSON_HS}	V_{BIAS} = 1.8V, I_{LX} = 0.5A		96	175	mΩ
Low-Side DMOS On-Resistance	R_{DSON_LS}	V_{BIAS} = 1.8V, I_{LX} = 0.5A		46	90	mΩ
High-Side DMOS Current-Limit Threshold	I_{LIM}	MAX42402	3.3	4.0	4.7	A
		MAX42403	4.375	5.300	6.200	
LX Leakage	I_{LX_LKG}	V_{SUP} = 36V, V_{LX} = 0V, or V_{LX} = 36V, T_A = +25°C			1	µA
Soft-Start Ramp Time	t_{SS}	f_{SW} = 400kHz		2.5		ms
		f_{SW} = 1.5MHz		3.5		
Minimum On-Time	t_{ON}			37	65	ns
Maximum Duty Cycle	D_{MAX}	Dropout mode	98	99		%
SWITCHING FREQUENCY						
PWM Switching Frequency	f_{SW}	f_{SW} = 400kHz	360	400	440	kHz
		f_{SW} = 1.5MHz	1.375	1.500	1.625	MHz
SYNC External Clock Frequency	f_{SYNC}	f_{SW} = 400kHz	360		600	kHz
		f_{SW} = 1.5MHz	1.215		1.845	MHz
Spread Spectrum	SPS	Percentage of f_{SW}		±6		%

(V_{SUP} = V_{EN} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. *Note 1* and *Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD OUTPUT							
PGOOD UV Threshold	$V_{PGOOD\_UV\_THR}$	V_{OUT} rising		91.75	94.00	96.25	%
	$V_{PGOOD\_UV\_THF}$	V_{OUT} falling		90.75	93.00	95.25	
PGOOD OV Threshold	$V_{PGOOD\_OV\_THR}$	V_{OUT} rising		102.75	105.00	107.25	%
	$V_{PGOOD\_OV\_THF}$	V_{OUT} falling		101.75	104.00	106.25	
PGOOD Debounce Time	t_{DEB_rising}	PWM mode	UV rising, OV falling, f_{SW} = 1.5MHz		180		µs
	$t_{DEB\_falling}$	PWM mode	UV falling, OV rising, f_{SW} = 1.5MHz		70		
PGOOD Leakage Current	I_{PGOOD_LKG}					2	µA
PGOOD Low Voltage Level	V_{PGOOD_LOW}	Sinking 1mA				0.4	V
LOGIC LEVELS							
EN High Voltage Level	V_{EN_HIGH}			0.825	0.900	0.975	V
EN Low Voltage Level	V_{EN_LOW}			0.625	0.700	0.775	V
EN Hysteresis		(*Note 3*)			200		mV
EN Input Current	I_{EN}	V_{EN} = V_{SUP} = 36V, T_A = +25°C				1	µA
SYNC High-Voltage Level	V_{SYNC_HIGH}			1.4			V
SYNC Low-Voltage Level	V_{SYNC_LOW}					0.4	V
SPS High-Voltage Level	V_{SPS_HIGH}			1.4			
SPS Low-Voltage Level	V_{SPS_LOW}					0.4	
THERMAL PROTECTION							
Thermal Shutdown	T_{SHDN}				175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}				15		°C

Note 1: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization.

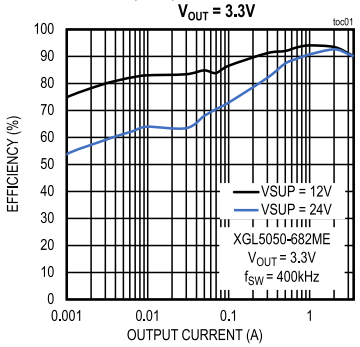
Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 3: Guaranteed by design; not production tested.

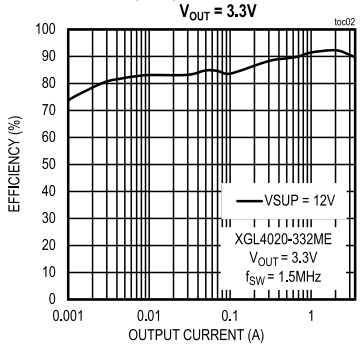
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

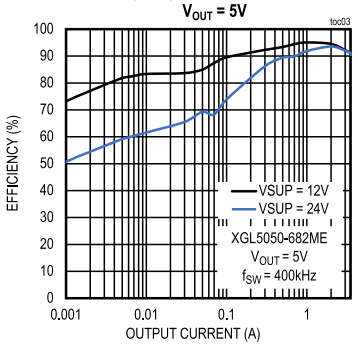
EFFICIENCY vs. OUTPUT CURRENT (SKIP) MAX42403AFLA+ V_{OUT} = 3.3V



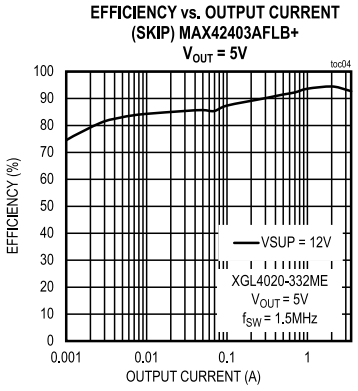
EFFICIENCY vs. OUTPUT CURRENT (SKIP) MAX42403AFLB+ V_{OUT} = 3.3V



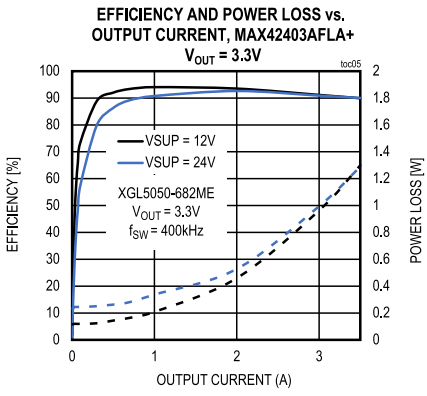
EFFICIENCY vs. OUTPUT CURRENT (SKIP) MAX42403AFLA+ V_{OUT} = 5V



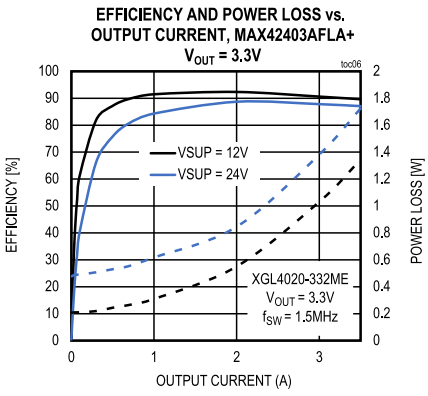
EFFICIENCY vs. OUTPUT CURRENT (SKIP) MAX42403AFLB+ V_{OUT} = 5V



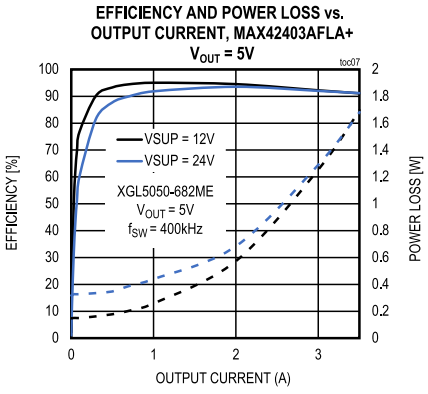
EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT, MAX42403AFLA+ V_{OUT} = 3.3V



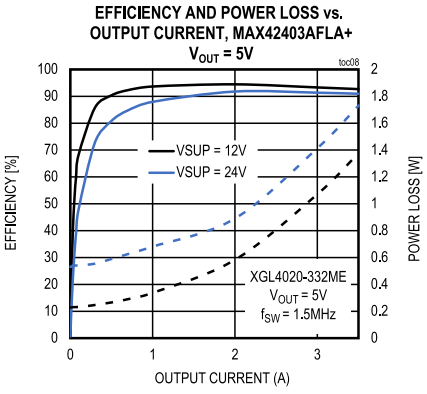
EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT, MAX42403AFLA+ V_{OUT} = 3.3V



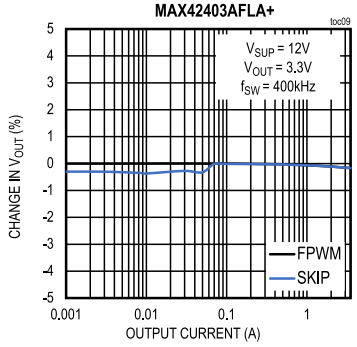
EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT, MAX42403AFLA+ V_{OUT} = 5V



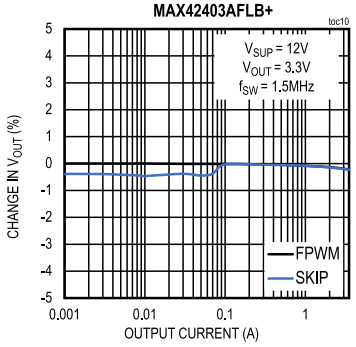
EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT, MAX42403AFLA+ V_{OUT} = 5V



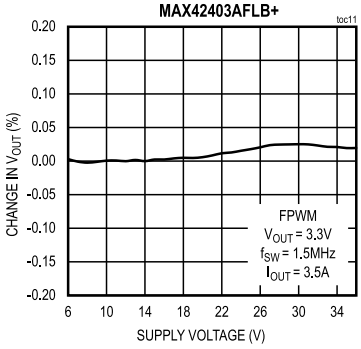
OUTPUT LOAD REGULATION
MAX42403AFLA+



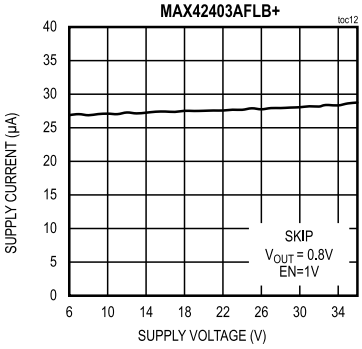
OUTPUT LOAD REGULATION
MAX42403AFLB+



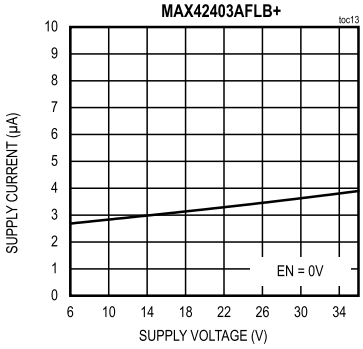
OUTPUT LINE REGULATION
MAX42403AFLB+



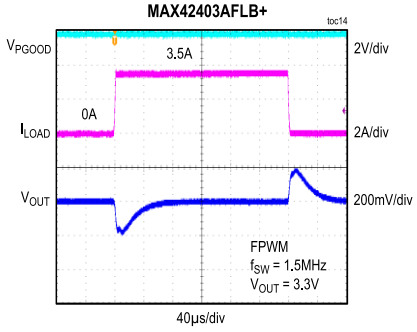
QUIESCENT CURRENT
vs. SUPPLY VOLTAGE
MAX42403AFLB+



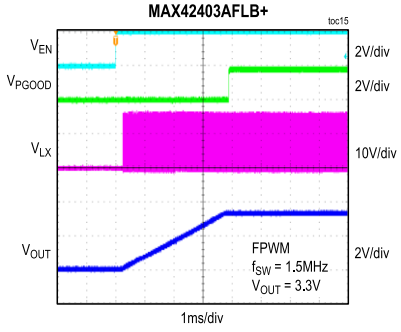
SHUTDOWN SUPPLY CURRENT
vs. SUPPLY VOLTAGE
MAX42403AFLB+



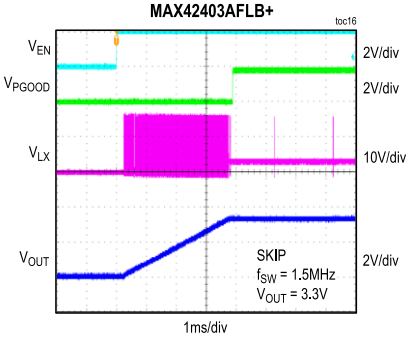
LOAD TRANSIENT RESPONSE
MAX42403AFLB+



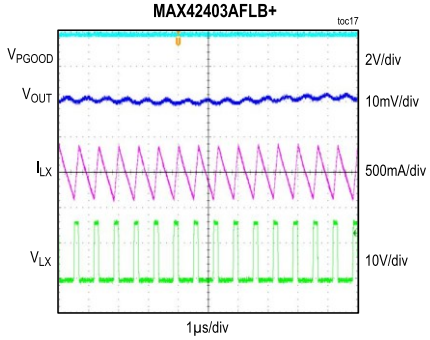
STARTUP INTO NO LOAD
MAX42403AFLB+



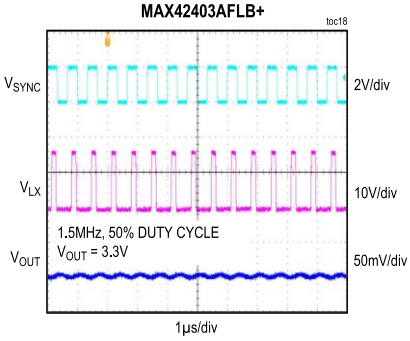
STARTUP INTO NO LOAD
MAX42403AFLB+



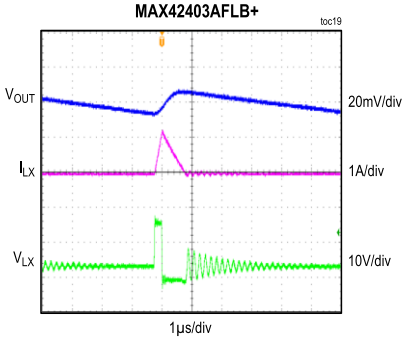
STEADY STATE SWITCHING WAVEFORM
MAX42403AFLB+



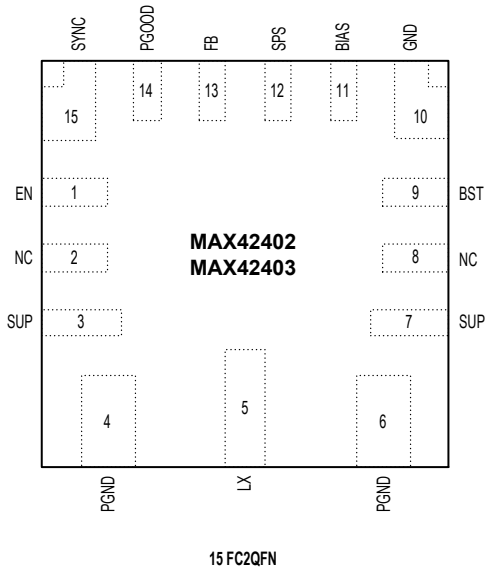
fSYNC SYNCHRONIZATION
MAX42403AFLB+



SKIP MODE OPERATION
MAX42403AFLB+



Pin Configurations



15 FC2QFN

Pin Descriptions

PIN	NAME	FUNCTION
1	EN	High-Voltage-Tolerant, Active-High Digital Enable Input. Drive EN high to enable buck converter.
2, 8	NC	Not Connected.
3, 7	SUP	Internal High-Side Supply Input. SUP provides power to the internal switch and LDO. Bypass SUP to PGND with 0.1µF and 2.2µF ceramic capacitors. Place the 0.1µF capacitor as close to the SUP and PGND pins as possible, followed by the 2.2µF capacitor.
4, 6	PGND	Power Ground.
5	LX	Inductor Connection. Connect LX to the switched side of the inductor.
9	BST	Boost Flying Capacitor Connection for High-Side FET Gate Voltage. Connect a 0.1µF ceramic capacitor between BST and LX.
10	GND	Quiet Analog Ground.
11	BIAS	1.8V Internal BIAS Supply. Connect a minimum of 2.2µF ceramic capacitor from BIAS to PGND.
12	SPS	Spread-Spectrum Enable. Connect to logic high to enable spread spectrum of the internal oscillator or logic low to disable spread spectrum.
13	FB	Feedback Input. It acts as an output voltage feedback input. Connect an external resistor-divider between the buck output, FB, and GND to set the output voltage.
14	PGOOD	Open-Drain Power-Good Output. Connect PGOOD to BIAS or an external positive power supply with a pullup resistor.
15	SYNC	External Clock Synchronization Input. Connect an external clock in the given frequency range to enable external clock synchronization. Connect SYNC to low to enable skip mode. Connect SYNC to high to enable FPWM mode.

Detailed Description

The MAX42402/MAX42403 are small, synchronous buck converters with integrated high-side and low-side switches. These devices are designed to deliver up to 2.5A/3.5A for input voltages of 4.5V to 36V. The MAX42402/MAX42403 offer adjustable output voltage options from 0.8V to 14V (up to 12V for 1.5MHz). Output voltage quality can be monitored by observing the PGOOD signal. The devices can operate in dropout by running at 99% duty cycle, which makes them ideal for industrial applications.

Frequency is internally fixed at 1.5MHz/400kHz, which allows for small external components and reduced output ripple. These converters automatically enter skip mode at light loads with ultra-low quiescent current of 27µA (typ) at no load when SYNC is pulled low. The MAX42402/MAX42403 feature spread-spectrum frequency modulation to minimize EMI-radiated emissions. The average current-mode architecture allows much better noise rejection of the current loop and very short minimum on-time.

Linear Regulator Output (BIAS)

The device includes a 1.8V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2uF ceramic capacitor from BIAS to GND.

System Enable (EN)

An enable control input (EN) activates the device from low-power shutdown mode. Drive EN high to turn on the internal linear BIAS LDO. Once V_{BIAS} is above the internal lockout threshold of 1.63V (typ), the converter is enabled, and the output voltage ramps up with the programmed soft-start time.

A logic-low at EN shuts down the device. During shutdown, the BIAS regulator and gate drivers turn off, and the quiescent current is reduced to 2.75µA (typ).

Synchronization Input (SYNC)

SYNC is a logic-level input used for operation-mode selection and frequency control. Connect SYNC to BIAS to enable forced fixed-frequency operation (FPWM) or to GND to enable automatic skip-mode operation for light load efficiency. SYNC can also be connected to an external clock, enabling forced-frequency operation. The device synchronizes to an external clock in two cycles, synchronizing at the rising edge of the signal applied. For more information, see the external clock frequency limits specified in the *Electrical Characteristics* table. When the external clock signal at SYNC is absent for more than two clock cycles, the IC switches to use the internal clock.

Soft-Start

The devices include a fixed, internal soft-start time dependent of the frequency. Soft-start time limits start-up inrush current by forcing the output voltage to ramp up towards its regulation point. The soft-start ramp rate is set at 2.5ms (typ) for 400kHz and 3.5ms (typ) for 1.5MHz.

Spread Spectrum

The devices feature a spread-spectrum option. When the SPS pin is pulled high, the spread-spectrum feature is enabled and the internal operating frequency is varied by ±6% relative to the internally generated operating frequency. The modulation signal is a triangular wave with a period of 300µs at 1.5MHz (1.25ms at 400kHz). Spread spectrum is disabled if the device is synchronized to an external clock.

Power-Good Output (PGOOD)

The MAX42402/MAX42403 feature an open-drain, power-good output (PGOOD) to monitor output voltage quality. PGOOD is an active-high output signal that pulls low when V_{OUT} falls below 93% (typ) of its nominal value or rises above 105% (typ) of its nominal value. Connect a 20kΩ (typ) pullup resistor to an external supply or to the on-chip BIAS output.

Overcurrent and Short-Circuit Protection

The devices feature a current limit that protects it against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side switch remains on until the inductor current reaches the specified LX current-limit threshold. The converter then turns the high-side switch off and the low-side switch on to allow the

inductor current to ramp down. Once the inductor current crosses below the low-side valley current-limit threshold, the converter turns on the high-side switch again. This cycle repeats until the short-circuit or overload condition is removed.

A short-circuit is detected when the output voltage falls below 50% of the regulation voltage while in current limit. If this occurs, hiccup mode activates, and the output turns off for 35ms (10 x 3.5ms, 1.5MHz) or 25ms (10 x 2.5ms, 400kHz) and then attempts to restart. This repeats indefinitely while the short-circuit condition is present. Hiccup mode is disabled during soft-start.

Thermal Shutdown

Thermal shutdown protects the devices from excessive operating temperature. When the junction temperature exceeds +175°C, an internal sensor shuts down the step-down converter, which allows the IC to cool. The sensor turns the IC on again after the junction temperature cools by 15°C.

Overvoltage Protection

The ICs feature overvoltage protection for the output. In case of an overvoltage event in skip mode, the high-side switch is turned OFF and the low-side switch is turned ON until the inductor current reaches a fixed negative value. Once this value is reached, the low-side switch is turned OFF and turns ON again in the next cycle until the output falls below the OV falling threshold. This way, the output is quickly discharged and brought back to regulation.

Applications Information

Setting the Output Voltage

The MAX42402/MAX42403 are available with adjustable-output-voltage. The output voltage can be adjusted between 0.8V and 14V (up to12V for 1.5MHz) using an external resistor-divider. Connect a resistor-divider from the buck output to FB to GND and a feed-forward capacitor from buck output to FB (see *Typical Application Circuits* section). Select $R_{FB2} \leq 50k\Omega$. Calculate R_{FB1} with the following equation:

Equation 1:

$$R_{FB1} = R_{FB2}\left[\left(\frac{V_{OUT}}{V_{FB}}\right) - 1\right]; \text{ where } V_{FB} = 0.8V$$

Table 1. Recommended Components for Adjustable Output

PART NUMBER	FREQUENCY	V_{OUT} (V)	INDUCTOR (µH)	EFFECTIVE C_{OUT} (µF)	CFF (pF)
MAX42402	400kHz	0.8 to 1.5	3.3	130	-
		1.5 to 3	4.7	63	33
		3 to 6	6.8	40	33
		6 to 10	8.2	30	22
		10 to 14	10	20	22
	1.5MHz	0.8 to 1.5	0.68	120	-
		1.5 to 3	1.5	55	47
		3 to 6	2.2	42	47
		6 to 12	4.7	25	82
MAX42403	400kHz	0.8 to 1.5	3.3	130	-
		1.5 to 3	3.3	70	33
		3 to 6	6.8	50	33
		6 to 10	8.2	40	22
		10 to 14	10	30	22
	1.5MHz	0.8 to 1.5	0.68	120	-
		1.5 to 3	1.0	74	47
		3 to 6	2.2	42	47
		6 to 12	3.3	25	82

Table 1 provides component selection recommendations for each output voltage range. The feed-forward capacitor (CFF) is recommended based on $R_{FB1} = 50k\Omega$.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The MAX42402/MAX42403 incorporate a symmetrical pinout to improve EMI performance. It is recommended to split the input capacitors symmetrically between the two SUP pins. Connect a 2.2µF (min) ceramic capacitor on each SUP pin for low-input voltage ripple. For additional noise immunity, a high-frequency 0603 or smaller capacitor with recommended value of 0.1µF can be added on each SUP pin.

A bulk capacitor with higher equivalent series resistance (ESR), such as an electrolytic capacitor, is normally required as well to lower the Q of the front-end circuit and provide the remaining capacitance needed to minimize input-voltage ripple.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

Equation 2:

$$I_{RMS} = I_{LOAD(MAX)} \times \left(\frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}} \right)$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability. The input-voltage ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge is equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

Equation 3:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \Delta I_L / 2}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUP}}$$

where:

I_{OUT} = maximum output current

D = duty cycle

Output Capacitor

The output capacitor is selected to meet output voltage ripple, load-transient response, and loop stability requirements. During a load step, the output current changes almost instantaneously, whereas the inductor is slow to react. During this transition time, the load-change requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. Output capacitance also affects the control-loop stability. For recommended output capacitor values, see *Table 1*.

The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 4 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output-ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 4:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_L}$$

$$C_{OUT} = \frac{\Delta I_L}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_L is the peak-to-peak inductor current and f_{SW} is the converter's switching frequency.

The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 5:

$$C_{OUT} = \frac{\Delta I}{\Delta V \times 2\pi \times f_C}$$

Where ΔI is the load change, ΔV is the allowed voltage droop, and f_C is the loop crossover frequency, which can be assumed to be the lesser of $f_{SW}/10$ or 100kHz. Any calculations involving C_{OUT} should consider capacitance tolerance, temperature, and voltage derating. *Table 1* shows the recommended output capacitor values according to switching frequency and output voltage.

Inductor Selection

Inductor design is a compromise between the size, efficiency, control-loop bandwidth, and stability of the converter. Insufficient inductance value increases the inductor current ripple, which causes higher conduction losses and higher output voltage ripple. Since the slope compensation is fixed internally for the MAX42402/MAX42403, it might also cause current-mode-control instability. A large inductor reduces the ripple but increases the size and cost of the solution and slows the response. *Table 2* provides optimized inductor values for the respective switching frequency and output voltage.

Table 2. Recommended Inductor Values

PART NUMBER	FREQUENCY	V_{OUT} (V)	INDUCTOR (µH)		
			MIN	TYP	MAX
MAX42402	400kHz	3.3	4.7	6.8	8.2
		5	6.8	8.2	10
		12	10	12	15
		14	12	15	18
	1.5MHz	3.3	1.5	2.2	2.8
		5	1.8	2.2	3.3
		12	3.3	4.7	5.6
MAX42403	400kHz	3.3	4.7	6.8	8.2
		5	4.7	6.8	8.2
		12	8.2	10	12
		14	8.2	10	12
	1.5MHz	3.3	1.0	2.2	2.8
		5	1.5	2.2	3.3
		12	3.3	4.7	5.6

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching-power losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. The package for the MAX42402/MAX42403 offer a unique symmetrical design, which helps to cancel the magnetic field generated in the opposite direction. See *Figure 1* for an example layout figure and the following guidelines for good PCB layout:

1. Place as many copper planes as possible under the IC footprint to ensure efficient heat transfer.
2. Place the input capacitors in a symmetrical configuration, with a 2.2µF (min) input capacitor on each SUP pin, close to the device. For additional noise immunity, when adding a high-frequency ceramic input-bypass capacitor (CBP) on each SUP pin, first place the high-frequency capacitor as close to the pin as possible, followed by the 2.2µF capacitor. Place the ceramic capacitors as close as possible to the SUP and PGND pins on both sides of the IC. Use low-impedance connections (no vias or other discontinuities) between the capacitors and IC pins. The CBP should be located closest to the IC and should have very good high-frequency performance (small package size and high capacitance). This provides the best EMI rejection and minimize internal noise on the device, which can degrade performance.
3. Connect PGND and GND pins directly under the IC. This ensures the shortest connection path between GND and PGND.
4. Place the BIAS capacitor as close to the IC BIAS pin as possible to reduce the bias current loop. This helps to reduce noise on BIAS for smooth operation.
5. Place the bootstrap capacitor CBST close to the IC and use short, wide traces to minimize the loop area to minimize the parasitic inductance. Use the nearest layer for a return trace (CBST to LX) to minimize the inductance further. For optimum design, refer to the layout in the MAX42402/MAX42403 EV kit. High parasitic inductance can impact switching speed (increase switching losses) and cause high dv/dt noise.
6. Place the inductor as close to the IC LX pin as possible and minimize the area of the LX node.
7. Place the output capacitors in a symmetrical configuration on opposite sides of the inductor for best noise immunity. Place the output capacitors (C_{OUT}) near the inductor so that the ground side of C_{OUT} is near the C_{IN} ground connection to minimize the current-loop area. Add vias on the capacitor ground to minimize the inductance. For additional noise immunity, place a high-frequency capacitor on each side of the inductor, followed by the output capacitors to further reduce the radiated noise.
8. Place the inductor, output capacitors, bootstrap capacitor, and BIAS capacitor in such a way as to minimize the area enclosed by the current loops. Keep the power traces and load connections short. This practice is essential for high efficiency. Use a thick copper PCB to enhance full-load efficiency and power-dissipation capability.
9. Use internal PCB layers as ground planes to help improve the EMI, as ground planes act as a shield against radiated noise. Spread multiple vias around the board, especially near the ground connections.
10. Use a continuous copper GND plane on the layer next to the IC to shield the entire circuit. The GND should also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect GND planes/areas for low impedance and maximum heat dissipation. Place vias at the GND terminals of the IC and input/output/bypass capacitors. Do not separate or isolate PGND and GND connections with separate planes or areas.
11. Place the feedback resistor-divider near the IC and route the feedback connection away from the inductor and LX node and other noisy signals.

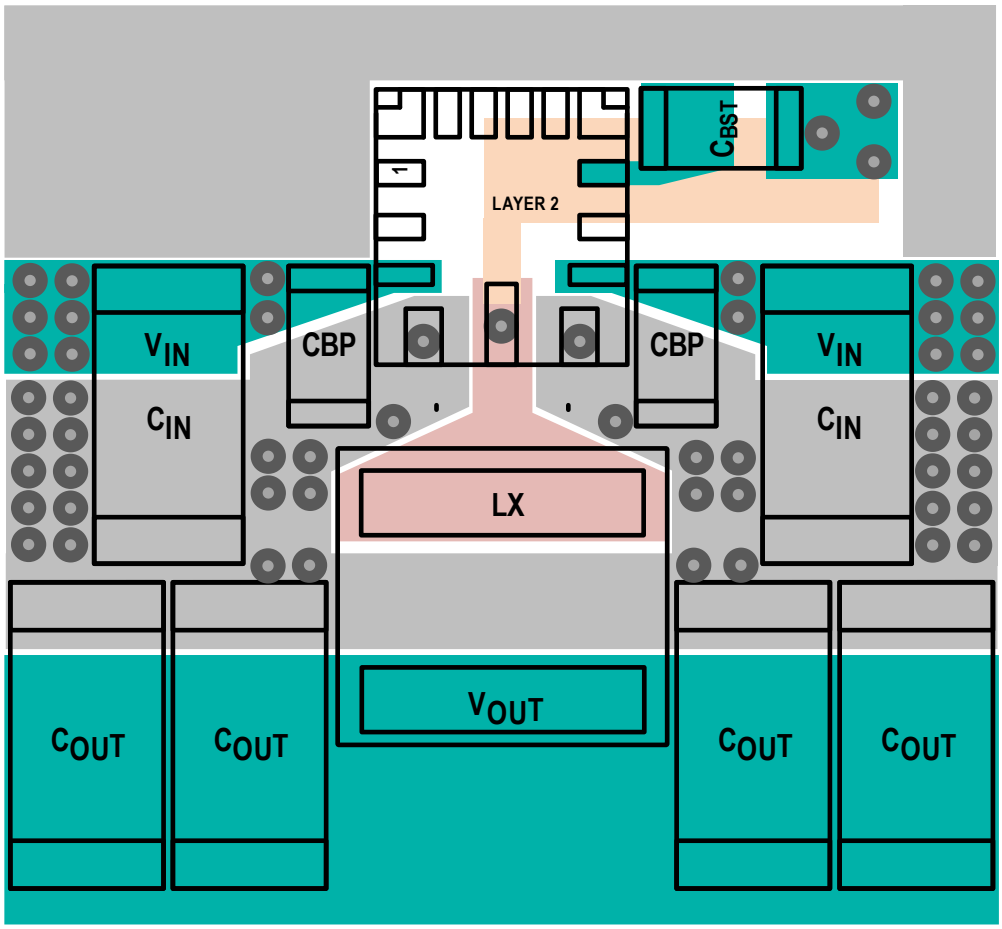
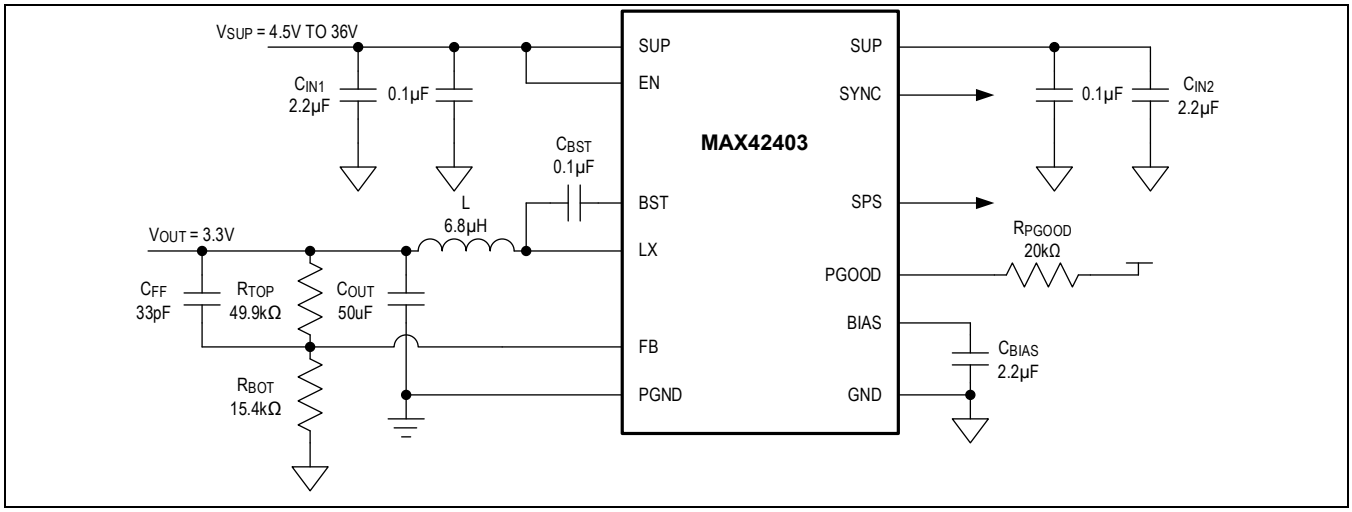


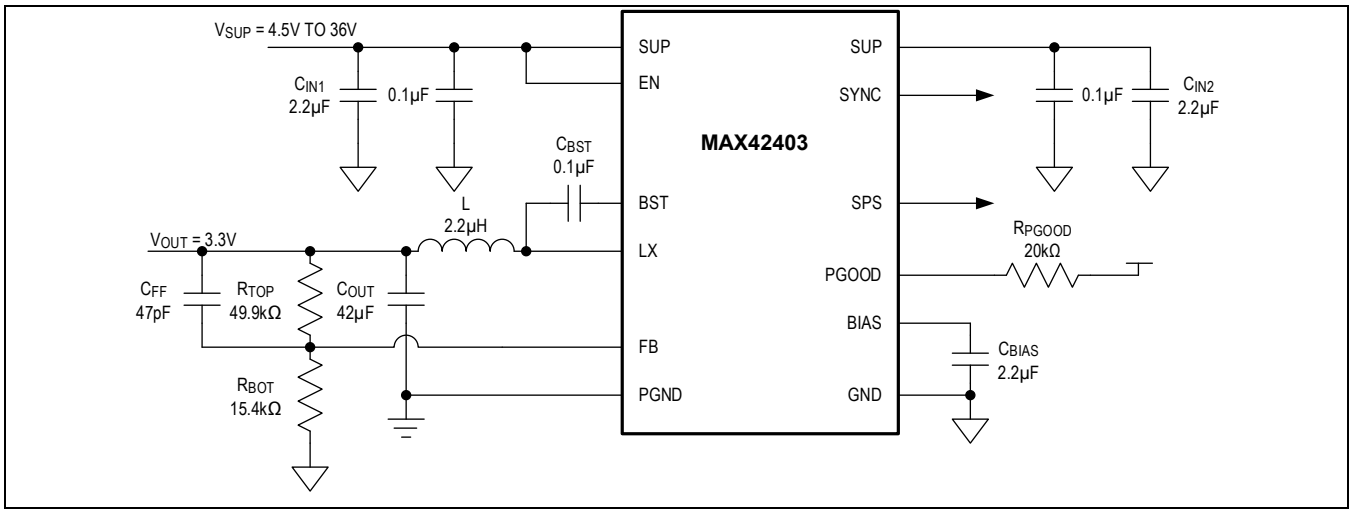
Figure 1. PCB Layout Example

Typical Application Circuits

400kHz



1.5MHz



Ordering Information

PART NUMBER	V_{OUT} (V)	MAXIMUM LOAD CURRENT (A)	SWITCHING FREQUENCY	SPREAD SPECTRUM (%)
MAX42402AFLA+	Adjustable 0.8V to 14V	2.5	400kHz	±6
MAX42402AFLB+	Adjustable 0.8V to 12V	2.5	1.5MHz	±6
MAX42403AFLA+	Adjustable 0.8V to 14V	3.5	400kHz	±6
MAX42403AFLB+	Adjustable 0.8V to 12V	3.5	1.5MHz	±6

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/23	Release for market intro	—
1	10/23	Updated Absolute Maximum Ratings and Electrical Characteristics section	3, 4, 5, 6
2	9/24	Updated Simplified Block Diagram, Typical Operating Characteristics, and Applications Information section	2, 8, 9, 10, 17, 18, 19
3	3/25	Updated Benefits and Features, Simplified Block Diagram, Electrical Characteristics, Applications Information, Table 2, Typical Application Circuits, and Ordering Information sections.	1, 2, 4, 12, 15 18