Fixed Frequency, 99% Duty Cycle Peak Current Mode Notebook System Power Controller

FEATURES

- Input Voltage Range: 4.5 V to 28 V
- Output Voltage Range: 1 V to 12 V
- Selectable Light Load Operation (Continuous / Auto Skip / Out-Of-Audio™ Skip)
- Programmable Droop Compensation
- Voltage Servo Adjustable Soft Start
- 200 kHz to 1 MHz Fixed Frequency PWM
- Current Mode Architecture
- 180° Phase Shift Between Channels
- Resistor or Inductor DCR Current Sensing
- Powergood Output for each channel
- OCL/OVP/UVP/UVLO protections
- Current Monitor Output for CH1
- Thermal Shutdown (Non-latch)
- Output Discharge Function (Disable option)
- Integrated Boot Strap MOSFET Switch
- QFN32 (RTV)

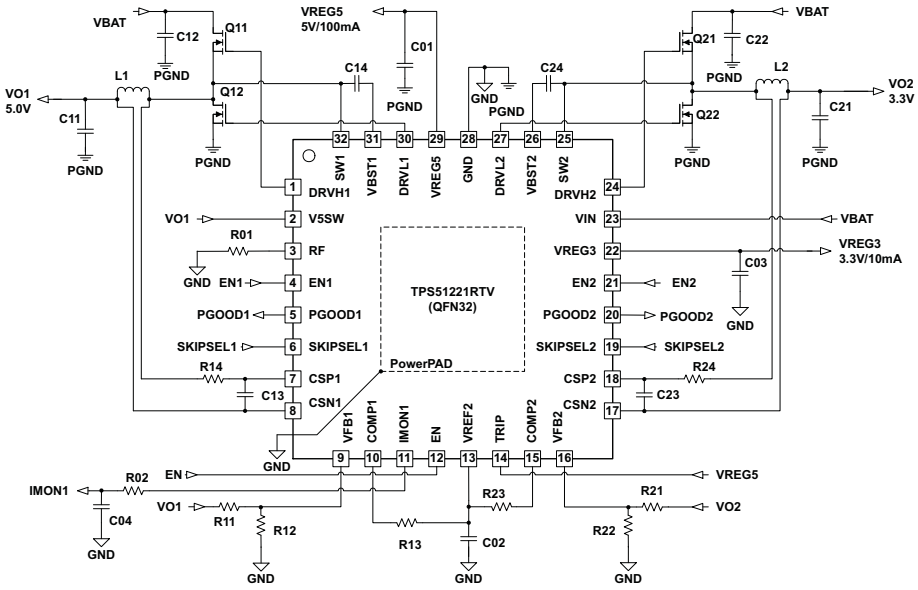
APPLICATIONS

- Notebook Computer System and I/O Bus
- Point of load in LCD TV, MFP

DESCRIPTION

The TPS51221 is a dual synchronous buck regulator controller with 2 LDOs. It is optimized for 5-V/3.3-V system controller, enabling designers to cost effectively complete 2-cell to 4-cell notebook system power supply. The TPS51221 supports high efficiency, fast transient response and 99% duty cycle operation. It supports supply input voltage ranging from 4.5 V to 28 V, and output voltages from 1 V to 12 V. Peak current mode supports stability operation with lower ESR capacitor and output accuracy. The high duty (99%) operation and wide input/ output voltage range supports flexible design for small mobile PCs and a wide variety of other applications. The fixed frequency can be adjusted from 200 kHz to 1MHz by a resistor, and each channel runs 180° out of phase. The TPS51221 can also synchronize to the external clock, and the interleaving ratio can be adjusted by its duty. The TPS51221 is available in the 32-pin 5×5 QFN package and is specified from –40°C to 85°C.

TYPICAL APPLICATION CIRCUIT



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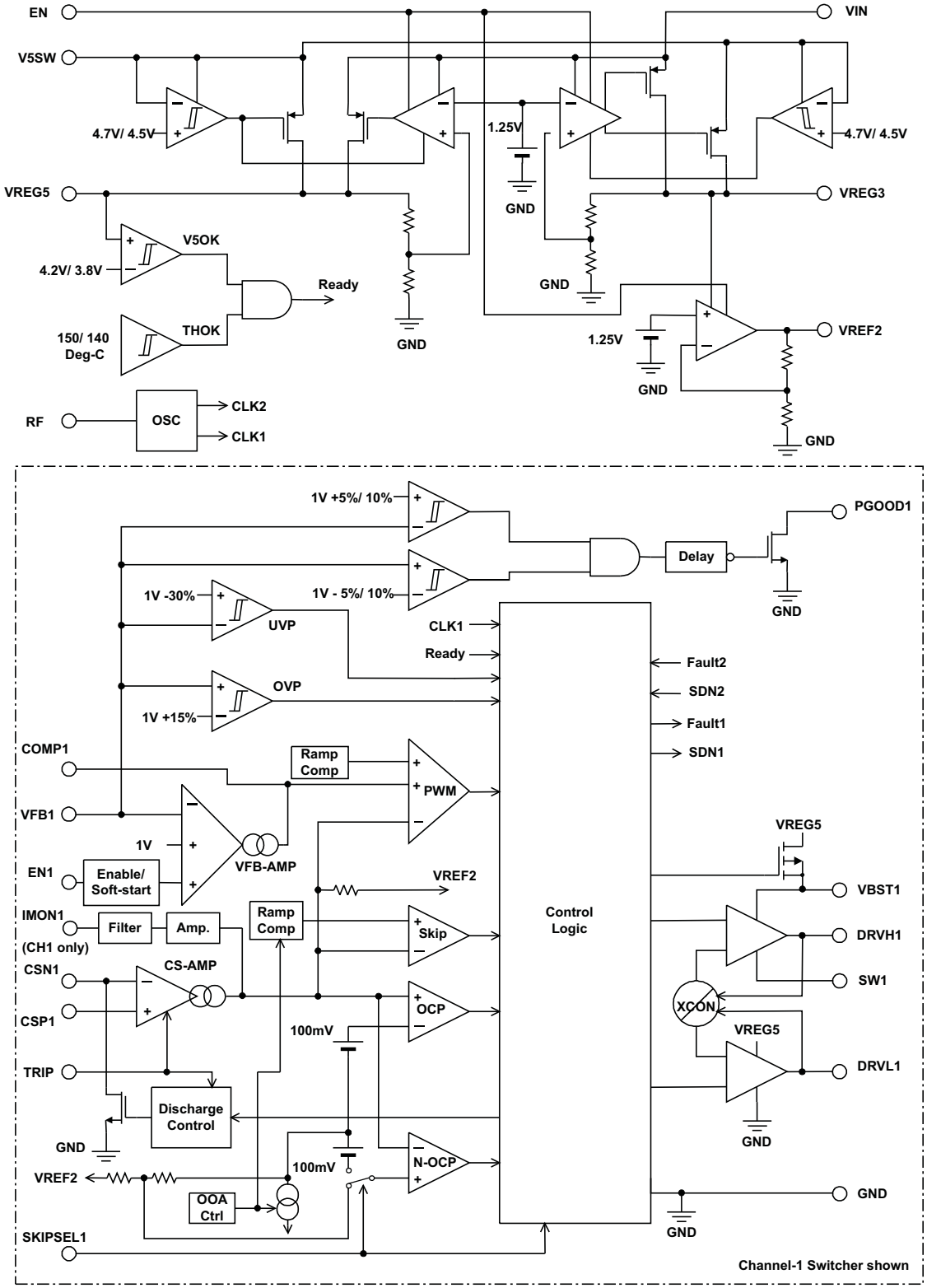
FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER	PINS	OUTPUT SUPPLY	MINIMUM ORDER QUANTITY	ECO PLAN
–40°C to 85°C	PLASTIC QUAD FLAT PACK (QFN)	TPS51221RTVT	32	Tape and reel	250	Green (RoHS and no Sb/Br)
		TPS51221RTVR		Tape and reel	3000	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage range (2)	VIN	–0.3 to 30	V
	VBST1, VBST2	–0.3 to 35	V
	VBST1, VBST2(3)	–0.3 to 7	V
	SW1, SW2	–5 to 30	V
	CSP1, CSP2, CSN1, CSN2	–1 to 13.5	V
	EN, EN1, EN2, VFB1, VFB2, TRIP, SKIPSEL1, SKIPSEL2	–0.3 to 7	V
	V5SW	–1 to 7	V
	V5SW (to VREG5)(4)	–7 to 7	V
Output voltage range(2)	DRVH1, DRVH2	–5 to 35	V
	DRVH1, DRVH2(3)	–0.3 to 7	V
	DRVL1, DRVL2, COMP1, COMP2, VREG5, RF, VREF2, IMON1 PGOOD1, PGOOD2	–0.3 to 7	V
	VREG3	–0.3 to 3.6	V
Operating junction temperature range, T_J		–40 to 125	°C
Storage temperature, T_{st}		–55 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the corresponding SW terminal.
(4) When EN is high and V5SW is grounded, or voltage is applied to V5SW when EN is low.

DISSIPATION RATINGS (2 oz Trace and Copper Pad with Solder)

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
32 pin RTV	1.7 W	17 mW/°C	0.7 W

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage	VIN	4.5		28	V
	V5SW	–0.8		6	
I/O voltage	VBST1, VBST2	–0.1		33	V
	DRVH1, DRVH2	–4.0		33	
	DRVH1, DRVH2 (wrt SW1, 2)	–0.1		6	
	SW1, SW2	–4.0		28	
	CSP1, CSP2, CSN1, CSN2	–0.8		13	
	EN, EN1, EN2, VFB1, VFB2, TRIP, DRVL1, DRVL2, COMP1, COMP2, VREG5, RF, VREF2, PGOOD1, PGOOD2, SKIPSEL1, SKIPSEL2, IMON1	–0.1		6	
	VREG3	–0.1		3.5	
Operating free-air temperature, T_A		–40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, EN=3.3V, VIN=12V, V5SW=5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VINSDN}	VIN shutdown current	VIN shutdown current, T_A = 25°C, No Load, EN = 0V, V5SW = 0 V			7	15	µA
$I_{VINSTBY1}$	VIN standby current 1	VIN standby current, T_A = 25°C, No Load, EN1=EN2=V5SW = 0 V			80	120	µA
$I_{VBATSTBY}$	Vbat standby current	Vbat standby current, T_A = 25°C, No Load SKIPSEL2=2V, EN2=open, EN1=V5SW=0V(1)			500		µA
I_{V5SW}	V5SW supply current	V5SW current, T_A = 25°C, No Load, ENx=5V, VFBx=1.05 V	TRIP = 5 V		1.2		mA
			TRIP = 0 V		1.4		mA
VREF2 OUTPUT							
V_{VREF2}	VREF2 output voltage	I_{VREF2} < ±10 µA, T_A = 25°C		1.98	2.00	2.02	V
		I_{VREF2} < ±100 µA, 4.5V < VIN < 25 V		1.97	2.00	2.03	
VREG3 OUTPUT							
V_{VREG3}	VREG3 output voltage	V5SW = 0 V, I_{VREG3} = 0 mA, T_A = 25°C		3.279	3.313	3.347	V
		V5SW = 0 V, 0 mA < I_{VREG3} <10 mA, 5.5 V <VIN<25 V		3.135	3.300	3.400	
I_{VREG3}	VREG3 output current	VREG3 = 3 V		10	15	20	mA
VREG5 OUTPUT							
V_{VREG5}	VREG5 output voltage	V5SW = 0 V, I_{VREG5} = 0 mA, T_A = 25°C		4.99	5.04	5.09	V
		V5SW = 0 V, 0 mA < I_{VREG5} <100 mA, 6 V <VIN<25 V		4.90	5.03	5.15	
		V5SW = 0 V, 0 mA < I_{VREG5} <100 mA, 5.5 V <VIN<25 V		4.50	5.03	5.15	V
I_{VREG5}	VREG5 output current	V5SW = 0 V, VREG5 = 4.5 V		100	150	200	mA
		V5SW = 5 V, VREG5 = 4.5 V		200	300	400	
V_{THV5SW}	Switchover threshold	Turning on		4.55	4.7	4.8	V
		Hysteresis		0.15	0.20	0.25	
td_{V5SW}	Switchover delay	Turning on			7.7		ms
R_{V5SW}	5V SW On-resistance	I_{VREG5} = 100 mA			0.5		Ω
OUTPUT							
V_{VFB}	VFB regulation voltage tolerance	T_A = 25°C, No Load		0.9925	1.000	1.0075	V
		T_A = –40°C to 85°C , No Load		0.990	1.000	1.010	
I_{VFB}	VFB input current	IVFB VFBx = 1.05 V, COMPx = 1.8 V, T_A = 25°C		–50		50	nA
R_{Dischg}	CSNx discharge resistance	ENx = 0 V, CSNx = 0.5 V, T_A = 25°C			20	40	Ω
VOLTAGE TRANSCONDUCTANCE AMPLIFIER							
Gm_V	Gain	T_A = 25°C			500		µS
Vind	Differential input voltage range			–30		30	mV
$I_{COMPSNK}$	COMP maximum sink current	COMPx = 1.8 V			33		µA
$I_{COMPSRC}$	COMP maximum source current	COMPx = 1.8 V			–33		µA

(1) Specified by design. Detailed external condition follows the application circuit of Figure 51

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, EN=3.3V, VIN=12V, V5SW=5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT AMPLIFIER						
G_C	Gain	TRIP = 0V/2V, CSN = 5V, T_A = 25°C(2)		3.333		
		TRIP=3.3V/5V, CSN=5V, T_A = 25°C(2)		1.667		
V_{IC}	Common mode input voltage range		0		13	V
V_{ID}	Differential input voltage range	T_A = 25°C	–75		75	mV
POWERGOOD						
V_{THPG}	PG threshold	PG in from lower	92.5%	95%	97.5%	
		PG in from higher	102.5%	105%	107.5%	
		PG hysteresis		5%		
I_{PG}	PG sink current	PGOOD = 0.5 V		5		mA
t_{PGDLY}	PGOOD Delay	Delay for PG in	0.8	1	1.2	ms
SOFTSTART						
t_{SSDYL}	Soft start delay	Delay for Soft Start, ENx=Hi to SS-ramp starts		200		µs
t_{SS}	Soft start time	Internal soft start		960		µs
FREQUENCY AND DUTY CONTROL						
f_{SW}	Switching frequency	Rf = 330 kΩ	273	303	333	kHz
V_{THRF}	RF threshold	Lo to Hi	0.7	1.3	2.0	V
		Hysteresis		0.2		V
f_{SYNC}	Sync input frequency range	Specified by design	200		1000	kHz
t_{ONMIN}	Minimum on-time	V_{DRVH} = 90% to 10%, No Load		120	150	ns
t_{OFFMIN}	Minimum off-time	V_{DRVH} = 10% to 90%, No Load		290	440	ns
t_D	Dead time	DRVH-off to DRVL-on	10	30	50	ns
		DRVL-off to DRVH-on	30	40	70	ns
V_{DTH}	DRVH-off threshold	DRVH to GND (2)		1.0		V
V_{DTL}	DRVL-off threshold	DRVL to GND(2)		1.0		V
OUTPUT DRIVERS						
R_{DRVH}	DRVH resistance	Source, $V_{VBST-DRVH}$ = 0.1 V		1.7	5.0	Ω
		Sink, $V_{DRVH-SW}$ = 0.1 V		1.0	3.0	
R_{DRVL}	DRVL resistance	Source, $V_{V5IN-DRVL}$ = 0.1 V		1.3	4.0	Ω
		Sink, $V_{DRVL-PGND}$ = 0.1 V		0.7	2.0	
CURRENT SENSE						
$V_{OCL-ULV}$	Current limit threshold (Ultra low voltage)	TRIP = 0V/2V, T_A = 25°C	27	31	35	mV
		TRIP = 0V/2V	25	31	37	
V_{OCL-LV}	Current limit threshold (low voltage)	TRIP = 3.3V/5V, T_A = 25°C	56	60	64	mV
		TRIP = 3.3V/5V	54	60	66	
V_{ZC}	Zero cross detection comparator offset	0.95V < CSNx < 12.6V	–4	0	4	mV
$V_{OCLN-ULV}$	Negative current limit threshold (ULV)	TRIP = 0V/2V, T_A = 25°C	–24	–31	–38	mV
		TRIP = 0V/2V	–22	–31	–40	
$V_{OCLN-LV}$	Negative current limit threshold (LV)	TRIP = 3.3V/5V, T_A = 25°C	–51	–60	–69	mV
		TRIP = 3.3V/5V	–49	–60	–71	

(2) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, EN=3.3V, VIN=12V, V5SW=5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVP, OVP AND UVLO						
V_{OVP}	OVP trip threshold	OVP detect	110%	115%	120%	
t_{OVPDLY}	OVP prop delay			1.5		µs
V_{UVP}	UVP trip threshold	UVP detect	65%	70%	73%	
t_{UVPDLY}	UVP delay		0.8	1	1.2	ms
V_{UVREF2}	VREF2 UVLO threshold	Wake up	1.7	1.8	1.9	V
		Hysteresis	75	100	125	mV
V_{UVREG3}	VREG3 UVLO threshold	Wake up	3.0	3.1	3.2	V
		Hysteresis	0.10	0.15	0.20	
V_{UVREG5}	VREG5 UVLO threshold	Wake up	4.1	4.2	4.3	V
		Hysteresis	0.35	0.40	0.44	V
INTERFACE AND LOGIC THRESHOLD						
V_{EN}	EN threshold	Wake up	0.8	1.0	1.2	V
		Hysteresis	0.1	0.2	0.3	
V_{EN12}	EN1/EN2 threshold	Wake up	0.45	0.50	0.55	V
		Hysteresis	0.1	0.2	0.3	
V_{EN12SS}	EN1/EN2 SS start threshold	SS-ramp start threshold at external soft start		1.0		V
$V_{EN12SSEND}$	EN1/EN2 SS end threshold	SS-End threshold at external soft start		2.0		V
I_{EN12}	EN1/EN2 source current	$V_{EN1/EN2}$ = 0V	1.5	2.0	2.6	µA
$V_{SKIPSEL}$	SKIPSEL1/SKIPSEL2 logic setting voltage	Continuous			1.5	V
		Auto Skip	1.9		2.1	
		OOA Skip (min 1/8 Fsw)	3.2		3.4	
		OOA Skip (min 1/16 Fsw)	3.8			
V_{TRIP}	TRIP logic setting voltage	$V_{OCL-ULV}$, Discharge ON			1.5	V
		$V_{OCL-ULV}$, Discharge OFF	1.9		2.1	
		V_{OCL-LV}, Discharge OFF	3.2		3.4	
		V_{OCL-LV}, Discharge ON	3.8			
I_{TRIP}	TRIP input current	TRIP = 0V	–1		1	µA
		TRIP =5V	–1		1	
$I_{SKIPSEL}$	SKIPSEL input current	SKIPSELx = 0 V	–0.5		0.5	µA
		SKIPSELx = 5 V	–0.5		0.5	
BOOT STRAP SW						
V_{FBST}	Forward voltage	$V_{VREG5-VBST}$, I_F = 10 mA, T_A = 25°C		0.10	0.20	V
I_{BSTLK}	VBST leakage current	VBST = 30 V, SW = 25 V		0.01	1.5	µA
THERMAL SHUTDOWN						
T_{SDN}	Thermal SDN threshold	Shutdown temperature(3)		150		°C
		Hysteresis(3)		10		

(3) Specified by design.

ELECTRICAL CHARACTERISTICS (continued)

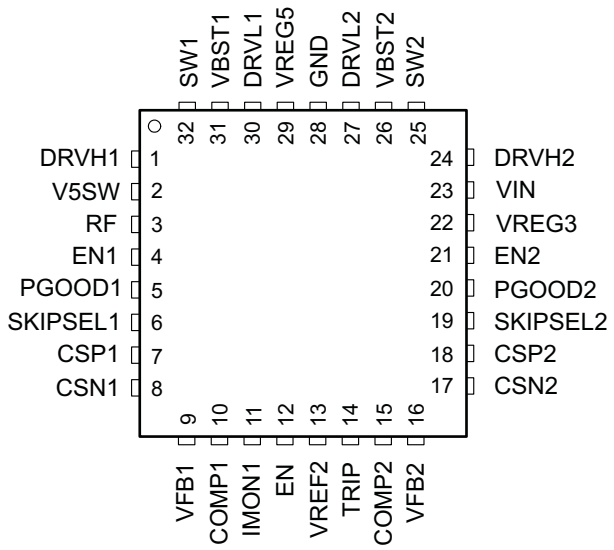
over operating free-air temperature range, EN=3.3V, VIN=12V, V5SW=5V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT MONITOR						
G_{IMON}	Current monitor gain	TRIP = 0V/2V		100		
		TRIP = 3.3V/5V		50		
V_{IMON}	Current monitor output	TRIP = 0V/2V, $V_{CSPx-CSNx}$ = 30 mV, 0.95V<CNSx<12.6V, T_A = 25°C	2.65	2.95	3.25	V
		TRIP = 3.3V/5V, $V_{CSPx-CSNx}$ = 60 mV, 0.95V<CNSx<12.6V, T_A = 25°C	2.75	3.0	3.25	
$V_{IMON-OFF}$	Current monitor output offset	TRIP = 0V/2V, $V_{CSPx-CSNx}$ = 0 V, 0.95V<CNSx<12.6V, T_A = 25°C	–300		300	mV
		TRIP = 3.3V/5V, $V_{CSPx-CSNx}$ = 0 V, 0.95V<CNSx<12.6V, T_A = 25°C	–200		200	

DEVICE INFORMATION

PINOUT

RTV PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DRVH1	1	O	High-side MOSFET gate driver outputs. Source 1.7 Ω, sink 1.0 Ω, SW-node referenced floating driver. Drive voltage corresponds to VBST to SW voltage.
DRVH2	24		
SW2	25	I/O	High-side MOSFET gate driver returns.
SW1	32		
VREG3	22	O	Always alive 3.3-V, 10-mA low dropout linear regulator output. Bypass to (signal) GND by more than 1-µF ceramic capacitor. Runs from VIN supply or from VREG5 when it is switched over to V5SW input.
EN1	4	I	Channel 1 and Channel 2 SMPS enable pins. When turning on, apply greater than 0.55 V and less than 6 V, or leave floating. Connect to GND to disable. Adjustable soft-start capacitance to be attached here.
EN2	21		
PGOOD1	5	O	Power good window comparator outputs for channel 1 and 2. The applied voltage should be less than 6V and recommended pull-up resistance value is from 100 kΩ to 1 MΩ.
PGOOD2	20		
SKIPSEL1	6	I	Skip Mode Selection pin. GND: Continuous Conduction Mode VREF2: Auto Skip VREG3: OOA Auto Skip, maximum 7 skips (use with < 400 kHz) VREG5: OOA Auto Skip, maximum 15 skips (use with more than 400 kHz)
SKIPSEL2	19		
CSP1	7	I/O	Current sense comparator inputs (+). An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. 0.1 µF is a good value to start design. Refer to current sensing scheme section for more details.
CSP2	18		
CSN1	8	I	Current sense comparator inputs (–). (See the current sensing scheme section.) Used as power supply for the current sense circuit for 5 V or higher output voltage setting. Also, used for output discharge.
CSN2	17		
VFB1	9	I	SMPS feedback inputs. Connect the feedback resistor divider and should refer to (signal) GND.
VFB2	16		
COMP1	10	I	Loop compensation pin (error amplifier output). Connect R (and C if required) from this pin to VREF2 for proper loop compensation with current mode operation.
COMP2	15		
RF	3	I/O	Frequency setting pin. Connect a frequency setting resistor to (signal) GND. Connect to an external clock for synchronization.
IMON1	11	O	Current monitor outputs for CH1. Adding RC filter is recommended.
VREF2	13	O	2-V reference output. Bypass to (signal) GND by 0.22-µF ceramic capacitor.
TRIP	14	I	Over current trip level and discharge mode selection pin. GND: $V_{OCL-ULV}$, Discharge on VREF2: $V_{OCL-ULV}$, Discharge off VREG3: V_{OCL-LV}, Discharge off VREG5: V_{OCL-LV}, Discharge on
EN	12	I	VREF2 and VREG5 Linear Regulators Enable Pin. When turning on, apply greater than 1.2 V and less than 6 V. Connect to GND to Disable.
VBST1	31	I	Supply inputs for high-side N-channel FET driver (boot strap terminal). Connect a capacitor (0.1 µF or greater is recommended) from this pin to respective SW terminal. Additional SB diode from VREG5 to this pin is an optional.
VBST2	26		
DRVL1	30	O	Low-side MOSFET gate driver outputs. Source 1.3 Ω, sink 0.7 Ω, GND referenced driver.
DRVL2	27		
V5SW	2	I	VREG5 switchover power supply input pin. When EN1 is high, PGOOD1 indicates *GOOD* and V5SW voltage is higher than 4.8 V, the switchover function is enabled. (Note: when switchover is enabled, VREG5 output voltage is approximately the same as the V5SW input voltage.)
VREG5	29	O	5-V, 100-mA low dropout linear regulator output. Bypass to (power) GND using a 10 µF ceramic capacitor. Runs from VIN supply. Internally connected to VBST and DRVL. Shuts off with EN. Switches over to V5SW when 4.8V or above is provided. (Note: when switch-over (see V5SW description above) is enabled, VREG5 output voltage is approximately the same as V5SW input voltage.)
VIN	23	I	Supply Input for 5-V and 3.3-V linear regulator. Typically connected to VBAT.
GND	28	—	Ground

TYPICAL CHARACTERISTICS

VIN SHUTDOWN CURRENT
vs
INPUT VOLTAGE

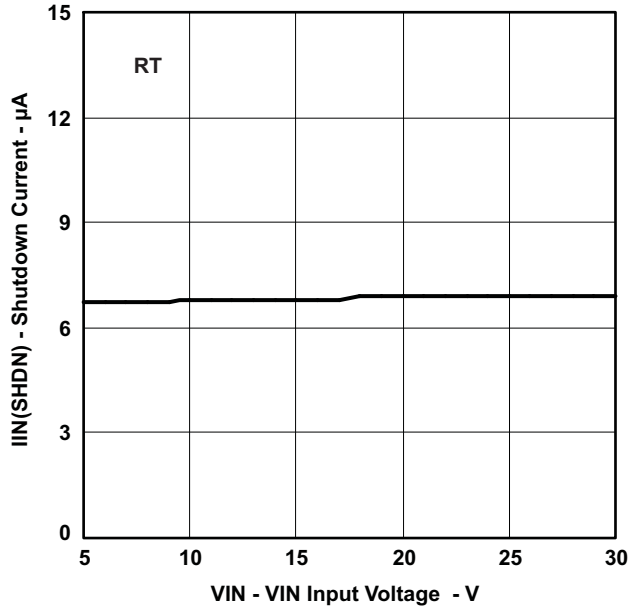


Figure 1.

VIN SHUTDOWN CURRENT
vs
JUNCTION TEMPERATURE

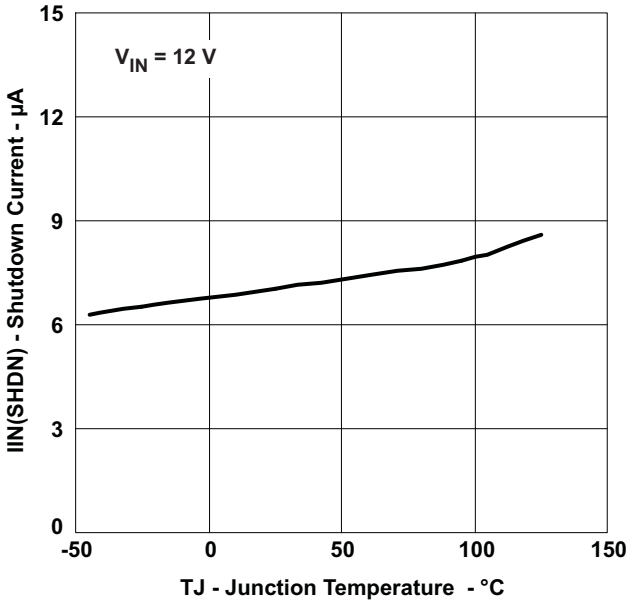


Figure 2.

VIN STANDBY CURRENT
vs
JUNCTION TEMPERATURE

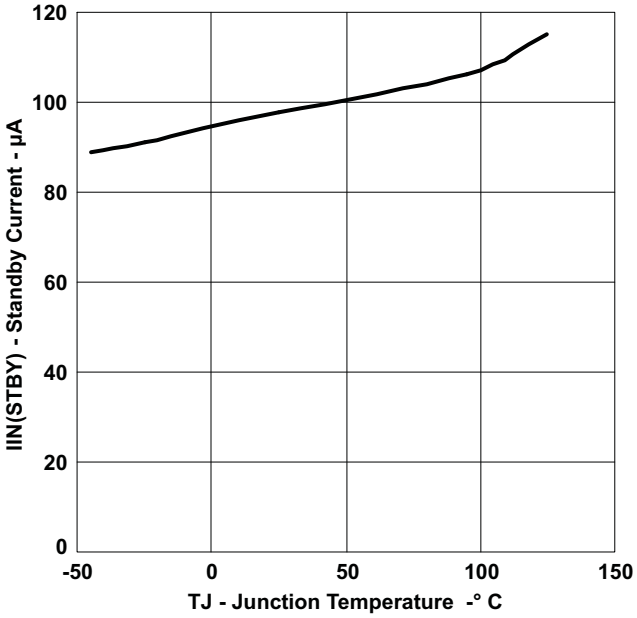


Figure 3.

VIN STANDBY CURRENT
vs
INPUT VOLTAGE

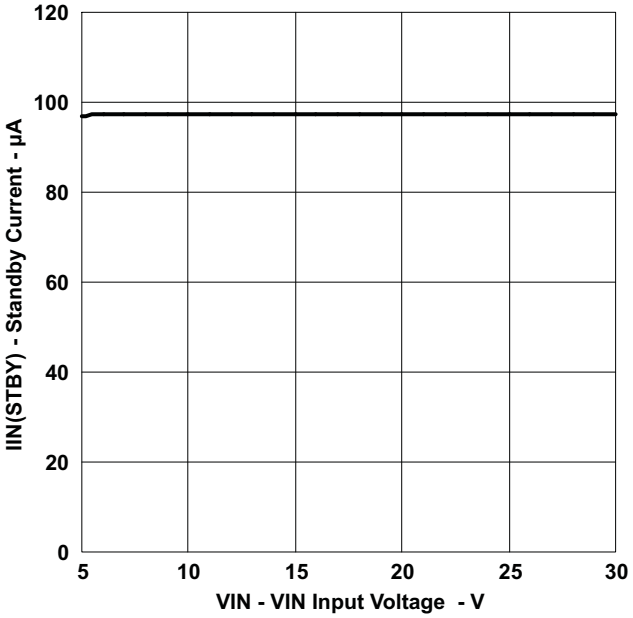


Figure 4.

TYPICAL CHARACTERISTICS (continued)

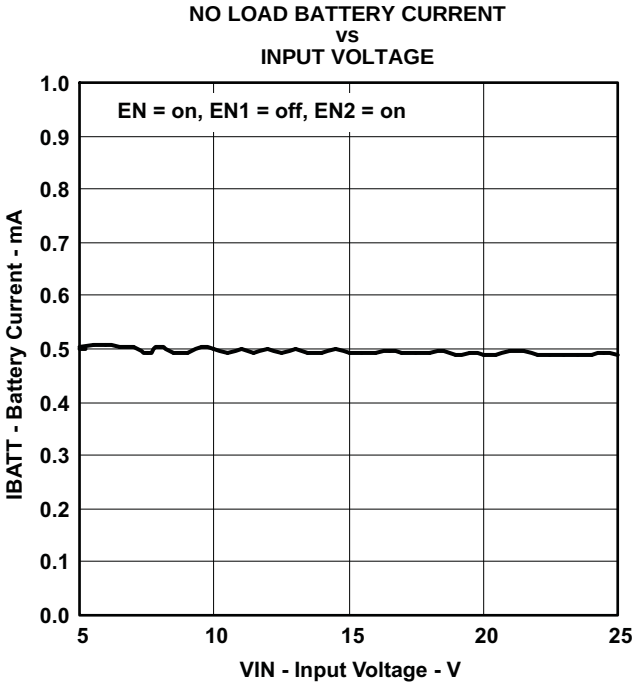


Figure 5.

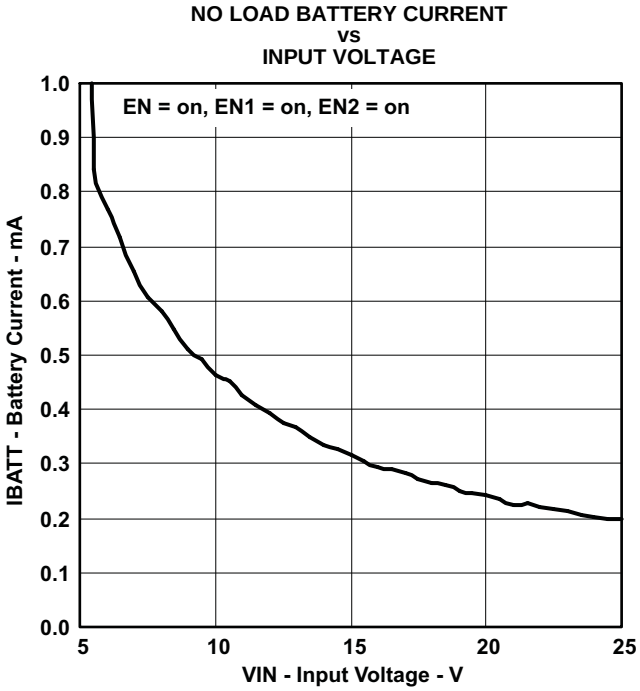


Figure 6.

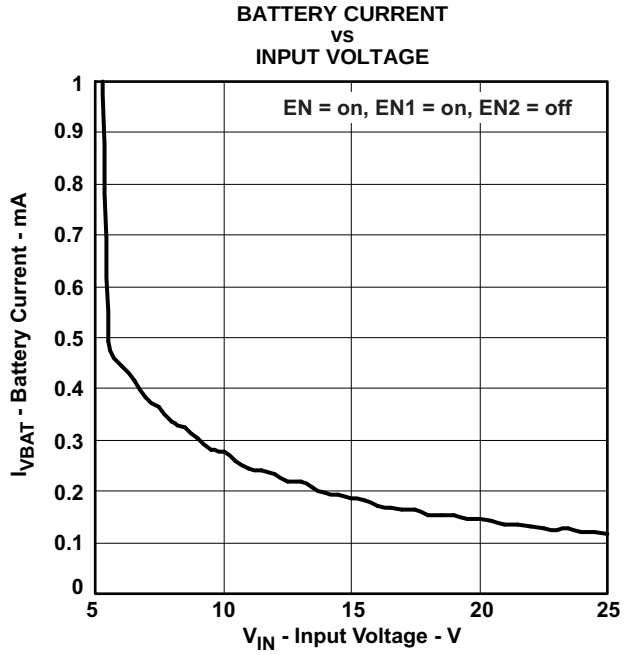


Figure 7.

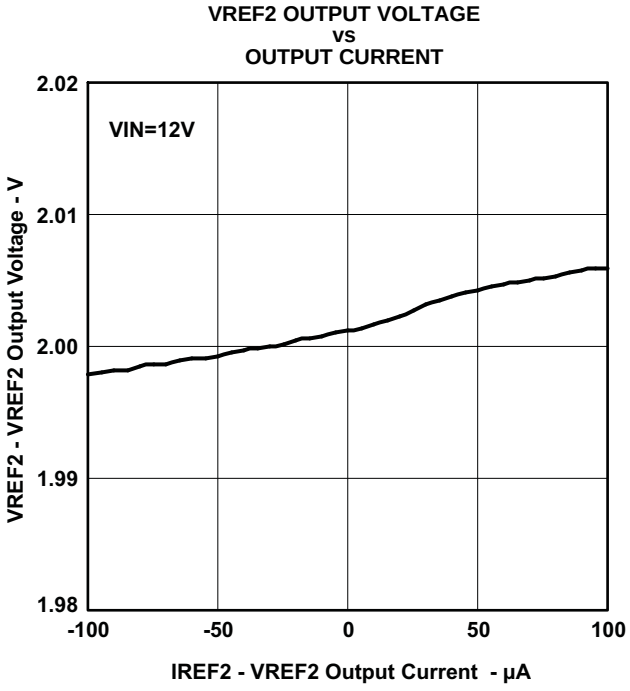


Figure 8.

TYPICAL CHARACTERISTICS (continued)

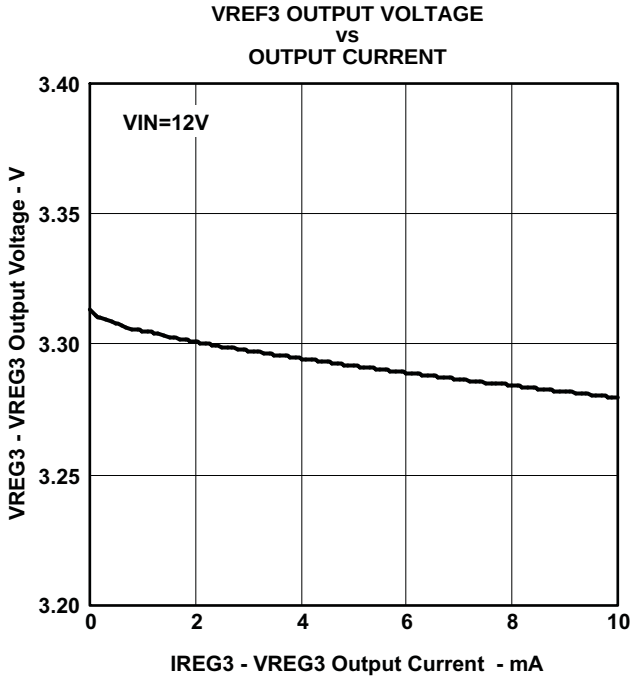


Figure 9.

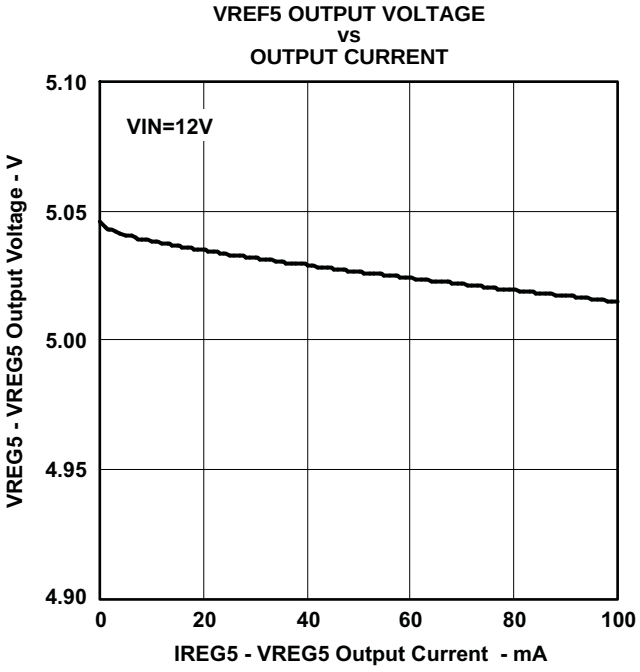


Figure 10.

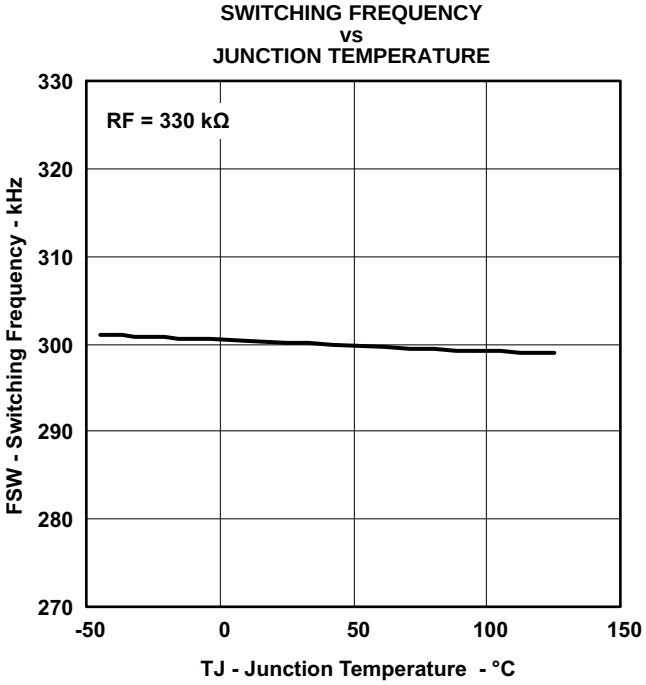


Figure 11.

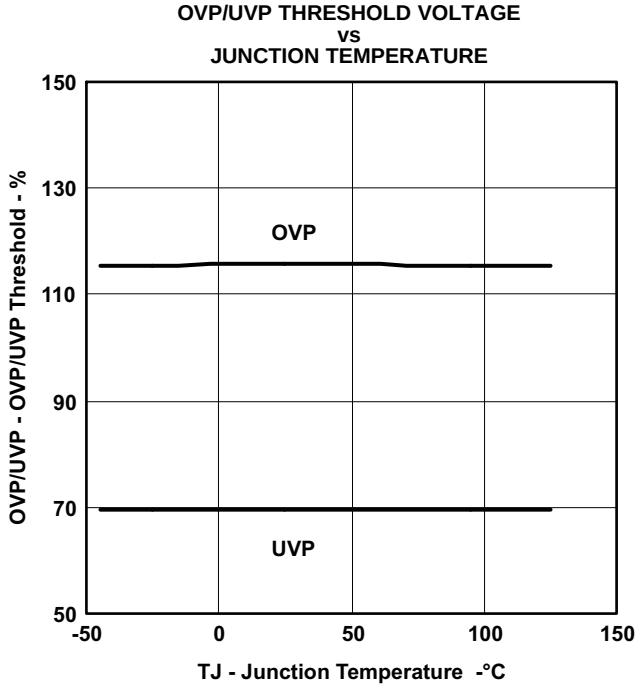


Figure 12.

TYPICAL CHARACTERISTICS (continued)

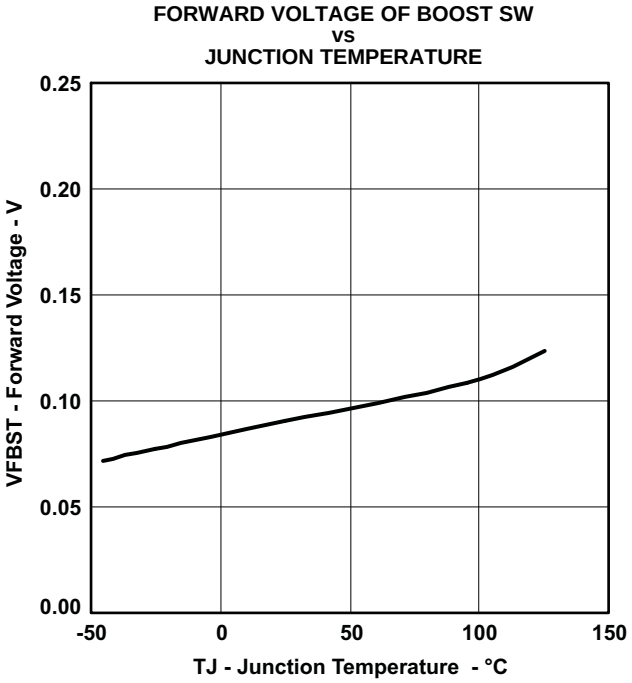
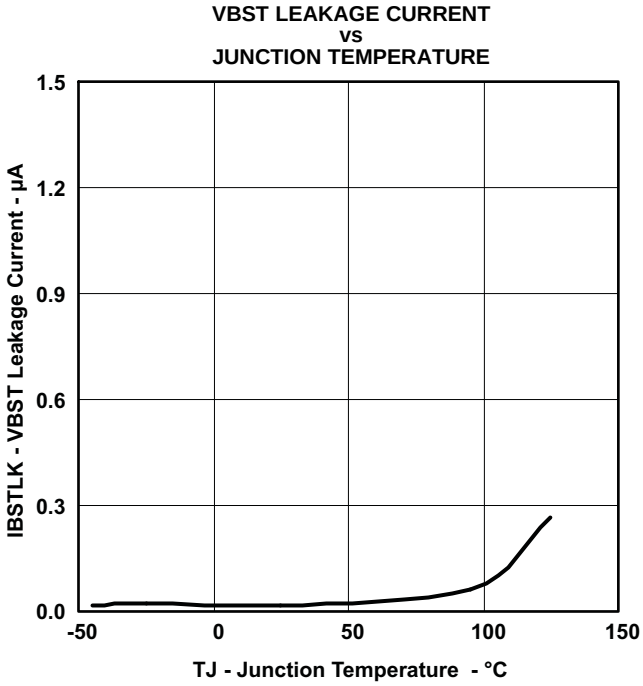


Figure 13.



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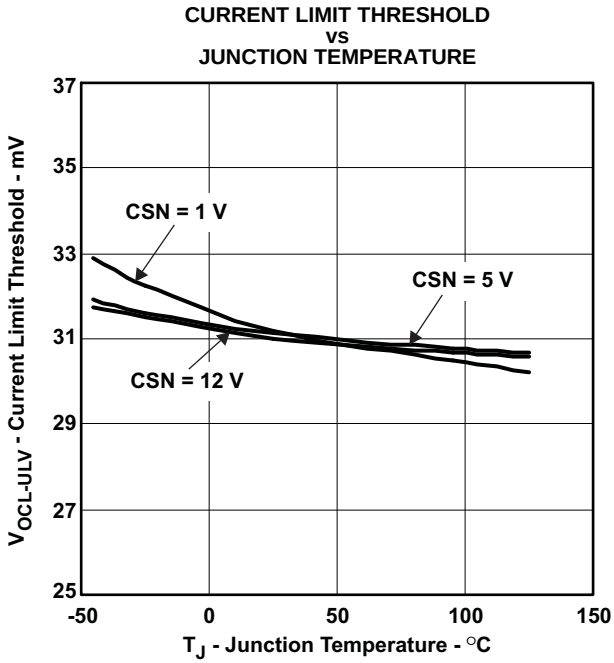

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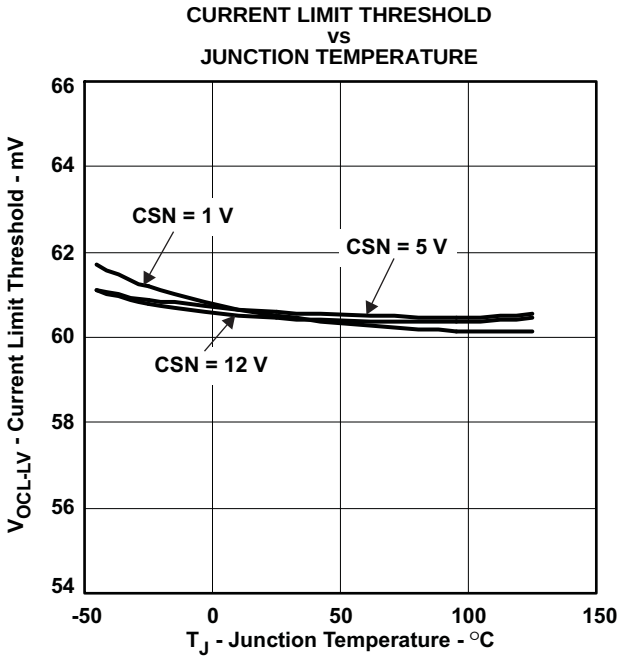
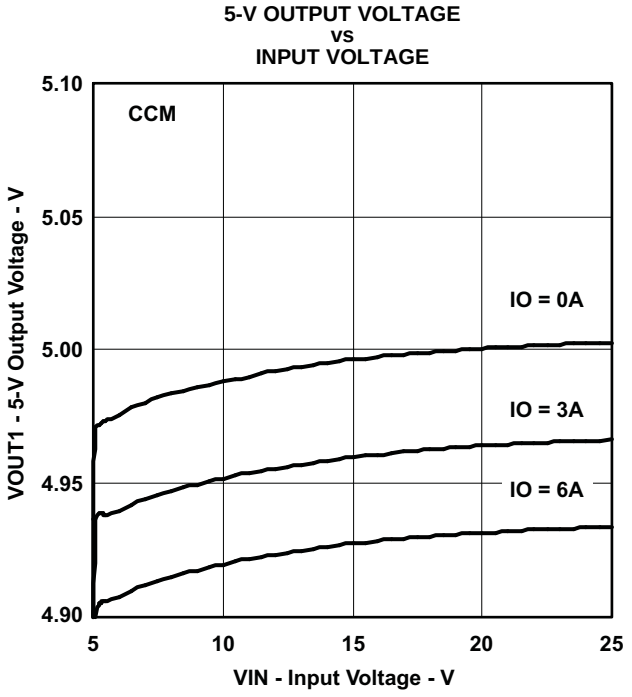


Figure 16.

TYPICAL CHARACTERISTICS (continued)



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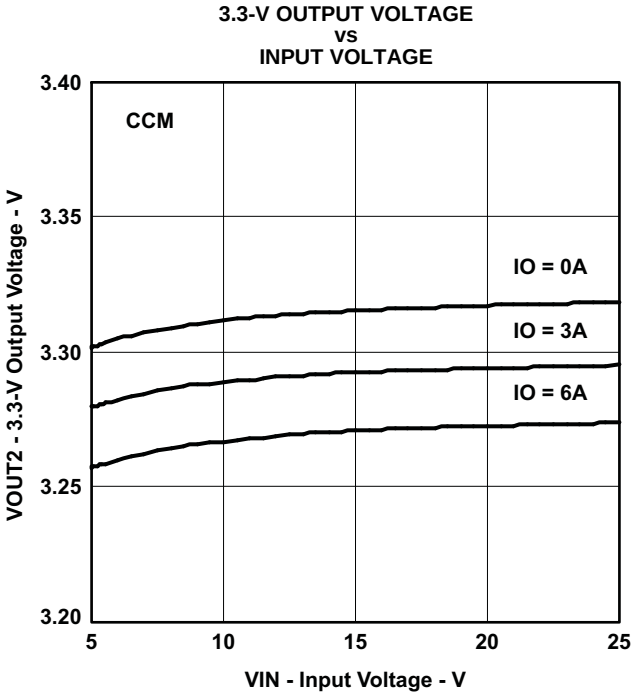


Figure 18.

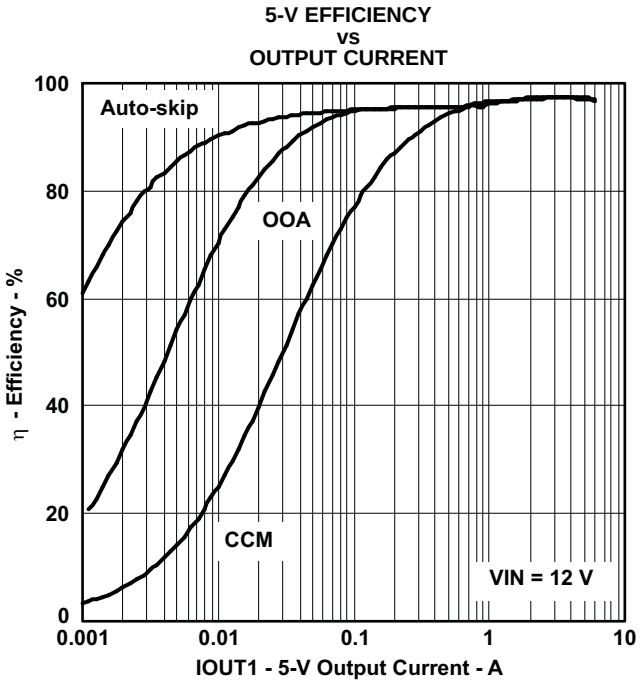


Figure 19.

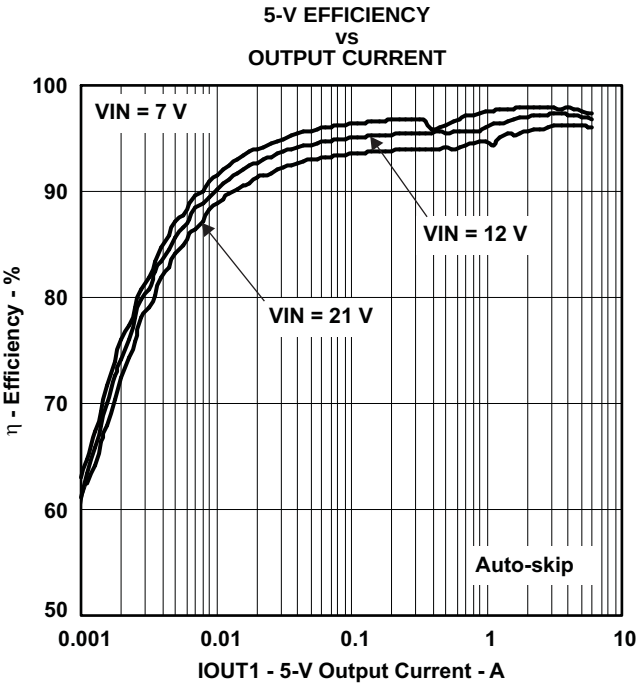


Figure 20.

TYPICAL CHARACTERISTICS (continued)

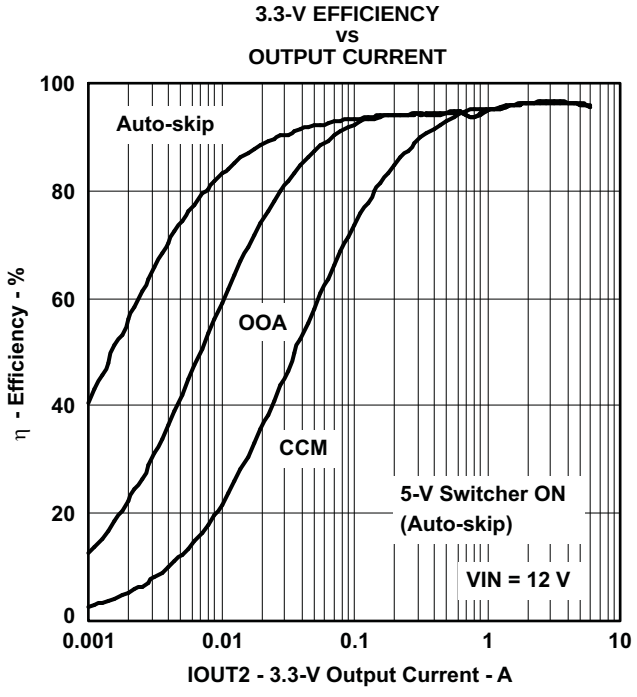
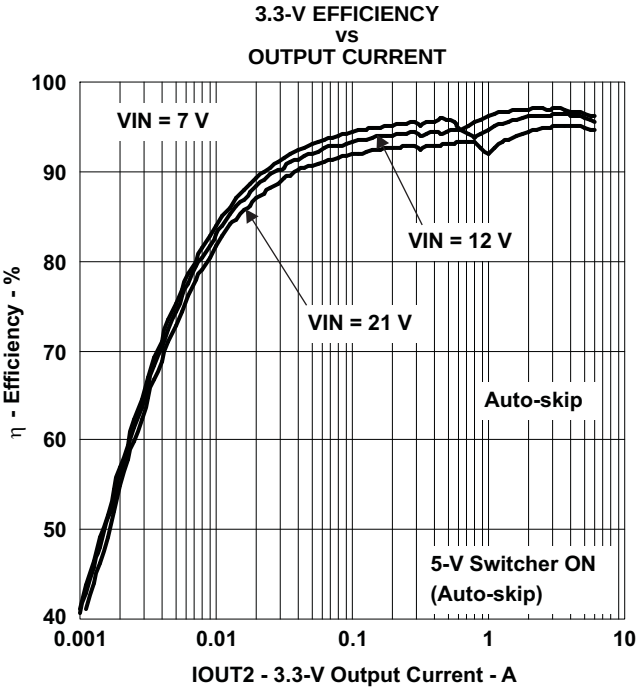


Figure 21.



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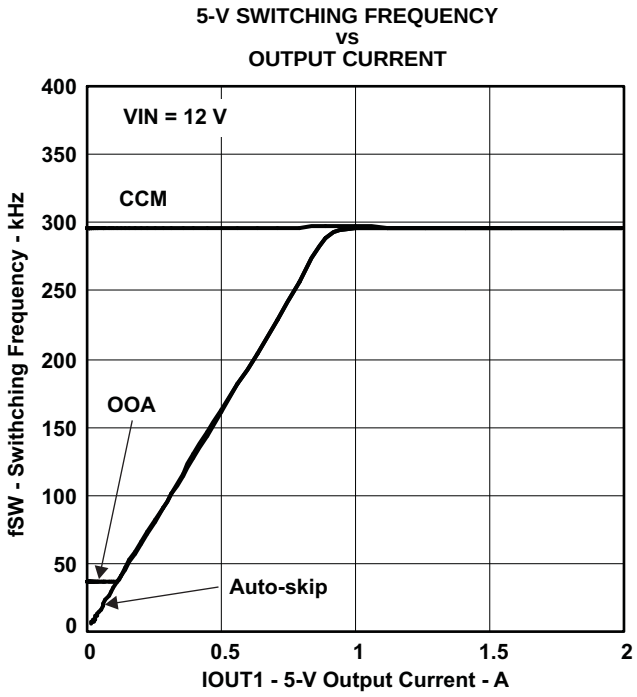


Figure 23.

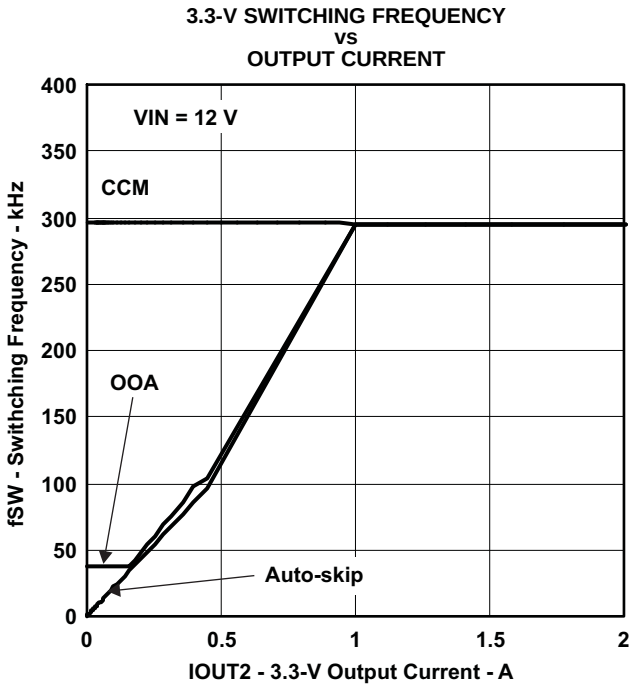


Figure 24.

TYPICAL CHARACTERISTICS (continued)

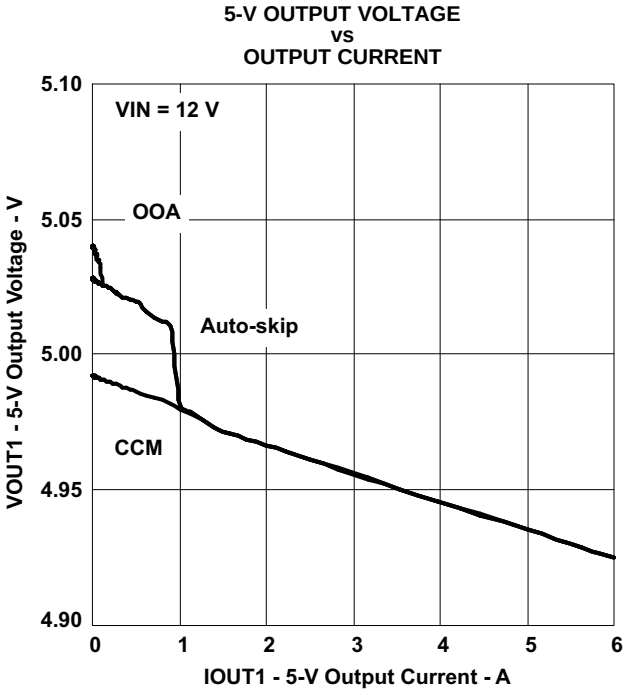
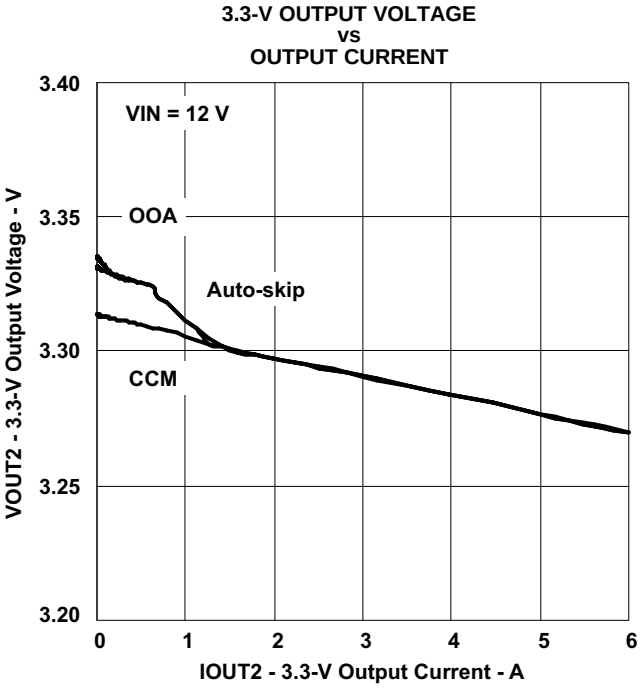


Figure 25.



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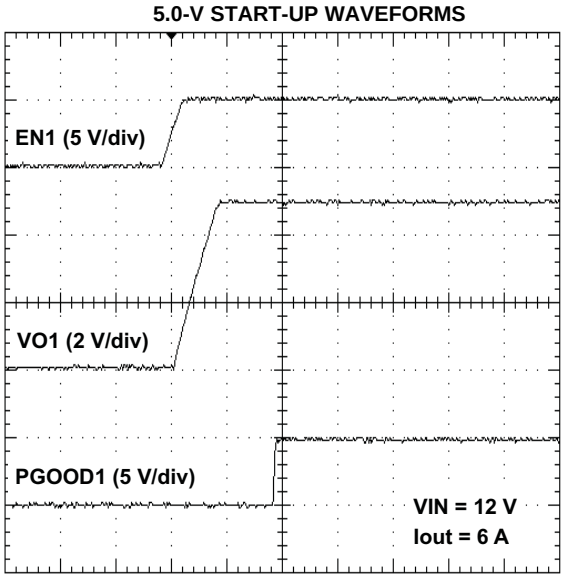


Figure 27.

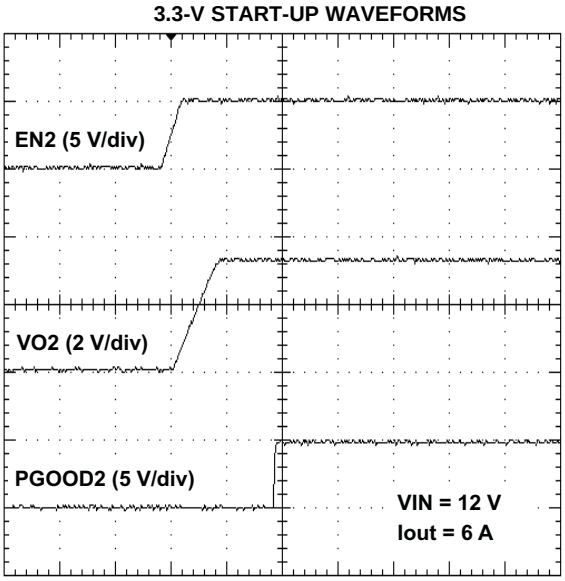
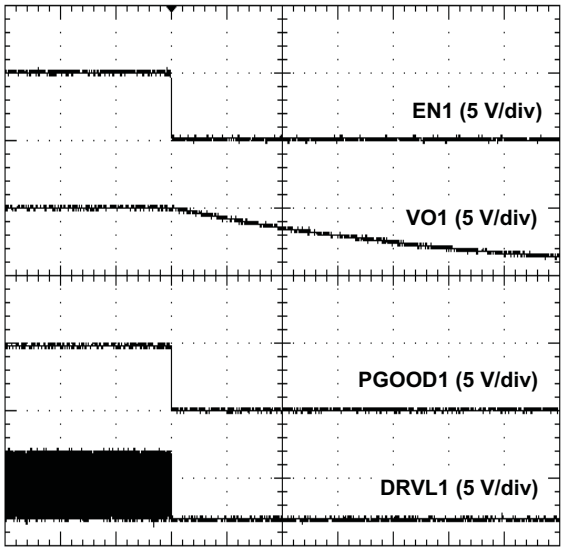


Figure 28.

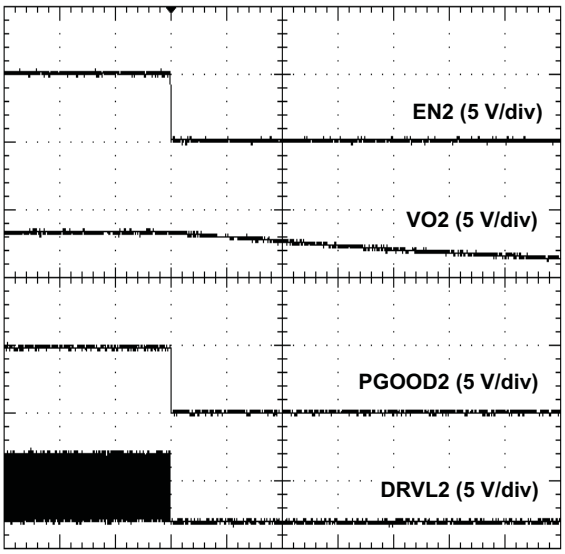
TYPICAL CHARACTERISTICS (continued)

5.0-V SOFT-STOP WAVEFORMS



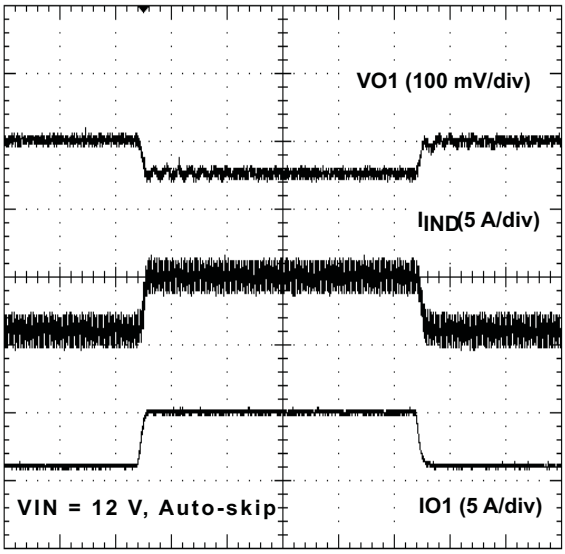
t - Time - 1 ms/div
Figure 29.

3.3-V SOFT-STOP WAVEFORMS



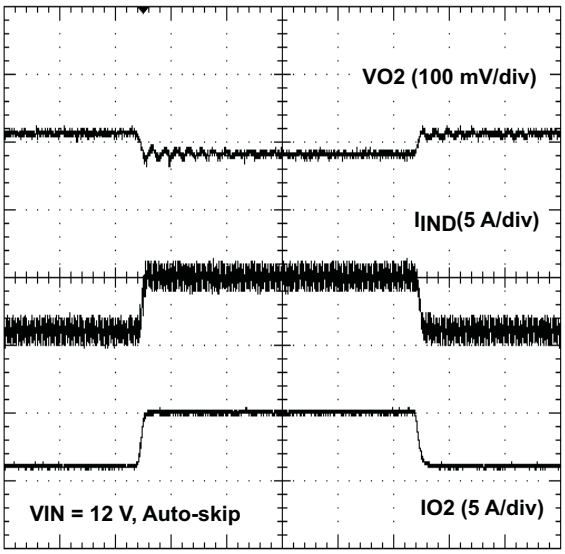
t - Time - 1 ms/div
Figure 30.

5.0-V LOAD TRANSIENT RESPONSSE



t - Time - 100 ms/div
Figure 31.

3.3-V LOAD TRANSIENT RESPONSSE



t - Time - 100 ms/div
Figure 32.

TYPICAL CHARACTERISTICS (continued)

5.0-V BODE-PLOT GAIN AND PHASE
vs
FREQUENCY

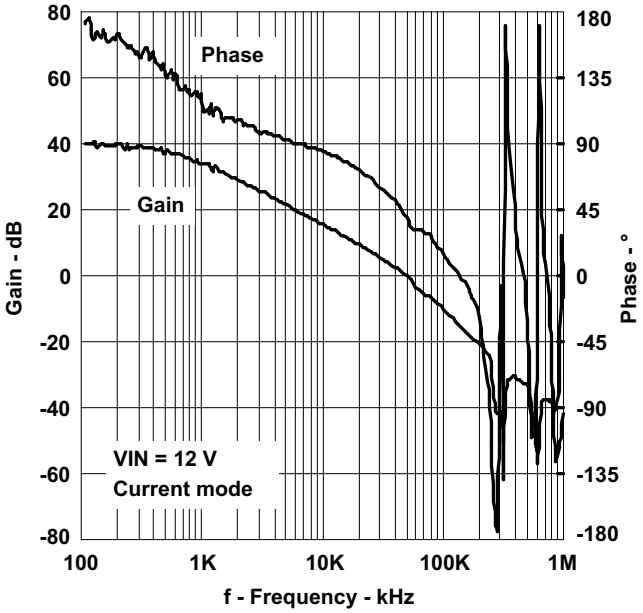


Figure 33.

3.3-V BODE-PLOT GAIN AND PHASE
vs
FREQUENCY

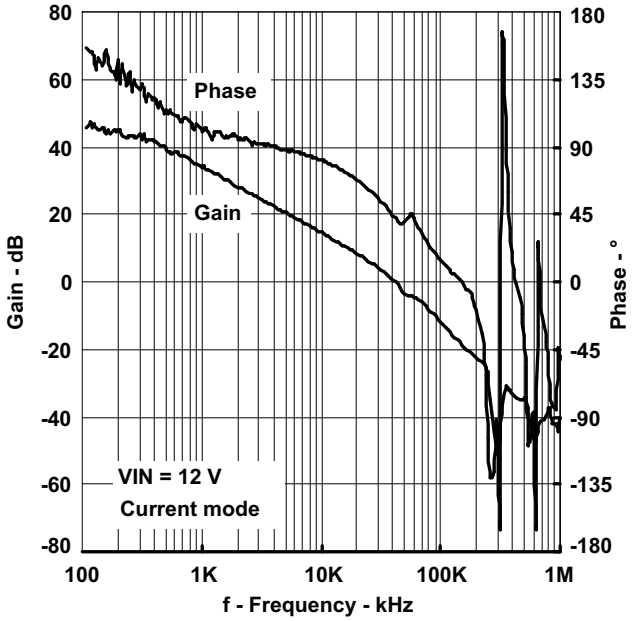


Figure 34.

IMON1 VOLTAGE
vs
OUTPUT CURRENT

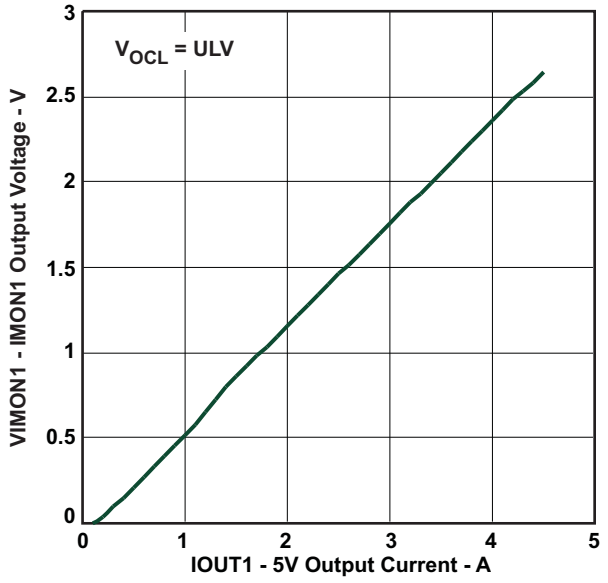


Figure 35.

IMON1 VOLTAGE
vs
OUTPUT CURRENT

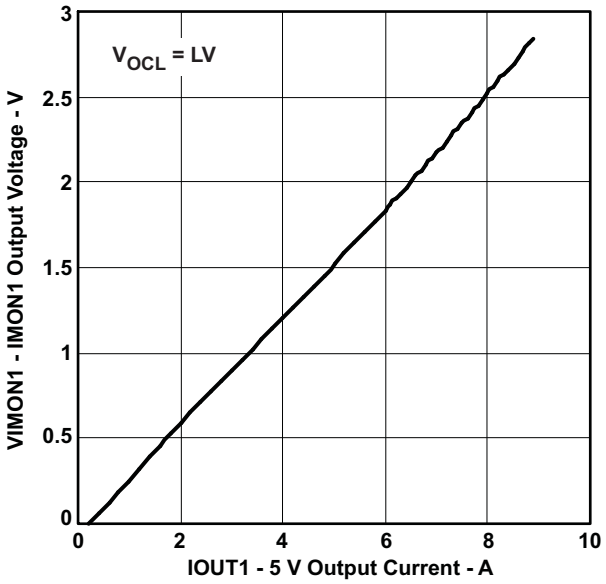
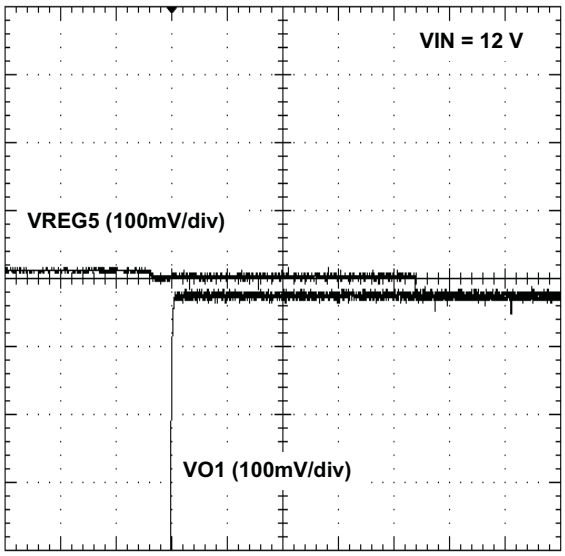


Figure 36.

TYPICAL CHARACTERISTICS (continued)

5.0-V SWITCH-OVER WAVEFORMS



t - Time - 2 ms/div

Figure 37.

DETAILED DESCRIPTION

ENABLE AND SOFT START

When EN is *Low*, the TPS51221 is in the shutdown state; only the 3.3-V LDO stays alive, and consumes 7μA (typically). When EN becomes *High*, the TPS51221 is in the standby state. The 2-V reference and the 5-V LDO become enabled, consume about 80 μA with no load condition, and are ready to turn on SMPS channels. Each SMPS channel is turned on when ENx becomes *High*. After ENx is set to high, the TPS51221 begins softstart, and ramps up the output voltage from zero to the target voltage with 0.96 ms. However, if a slower soft-start is required, an external capacitor can be tied from the ENx pin to GND. In this case, the TPS51221 charges the external capacitor with the integrated 2-μA current source. An approximate external soft-start time would be $t_{EX\text{-}SS}=C_{EX} / I_{EN12}$, it means the time from ENx=1V to ENx=2V. Recommend capacitance is more than 2.2nF.

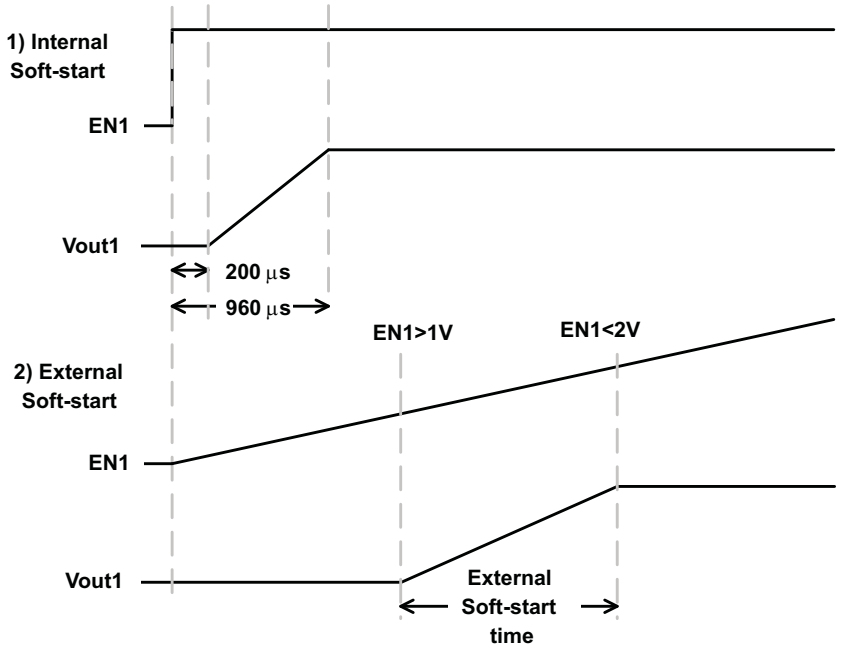


Figure 38. Enable and Soft-Start Timing

Table 1. Enable Logic States

EN	EN1	EN2	VREG3	VREF2	VREG5	CH1	CH2
GND	Don't Care	Don't Care	**ON**	Off	Off	Off	Off
Hi	Lo	Lo	**ON**	**ON**	**ON**	Off	Off
Hi	Hi	Lo	**ON**	**ON**	**ON**	**ON**	Off
Hi	Lo	Hi	**ON**	**ON**	**ON**	Off	**ON**
Hi	Hi	Hi	**ON**	**ON**	**ON**	**ON**	**ON**

PRE-BIASED START-UP

The TPS51221 supports a pre-biased start up by preventing negative inductor current during soft-start when the output capacitor holds some charge. The initial DRHV signal waits until the voltage feedback signal becomes greater than the internal reference ramping up by the soft-start function. After that, the start-up occurs the same way the the soft-start condition fully discharges, regardless of the SKIPSELx selection.

3.3 V, 10 mA LDO (VREG3)

A 3.3-V, 10mA, linear regulator is integrated in the TPS51221. This LDO services some of the analog supply rail for the IC and provides a handy standby supply for 3.3-V *Always On* voltage in the notebook system. Apply a 2.2-μF (at least 1-μF), high quality X5R or X7R ceramic capacitor from VREG3 to (signal) GND, adjacent to the IC.

2.0-V, 100 μA Sink/ Source Reference (VREF2)

This voltage is used for the reference of the loop compensation network. Apply a 0.22-μF (at least 0.1-μF), high quality X5R or X7R ceramic capacitor from VREF2 to (signal) GND, adjacent to the IC.

5.0-V, 100 mA LDO (VREG5)

A 5.0-V, 100-mA linear regulator is integrated in the TPS51221. This LDO services the main analog supply rail for the IC and provides current for gate drivers until switch-over function becomes enabled. Apply 10-μF (at least 4.7-μF), high quality X5R or X7R ceramic capacitor from VREG5 to (power) GND, adjacent to the IC.

VREG5 SWITCHOVER

When EN1 is high, PGOOD1 indicates *GOOD* and more than 4.7-V voltage is applied to V5SW, the internal 5V-LDO is shut off and the VREG5 is shorted to V5SW by an internal MOSFET after A 7.7ms delay. When the V5SW voltage becomes lower than 4.5 V, EN1 becomes low, or PGOOD1 indicates *BAD*, the internal switch is turned off and the internal 5V-LDO resumes immediately.

BASIC PWM OPERATIONS

The main control loop of the SMPS is designed as a fixed-frequency, peak current mode pulse width modulation (PWM) controller. It can achieve stable operation in any type of capacitors, including low ESR capacitor(s) such as ceramic or specialty polymer capacitors.

The TPS51221 SMPS uses the output voltage information and the inductor current information to regulate the output voltage. The output voltage information is sensed by VFBx pin. The signal is compared with the internal 1-V reference and the voltage difference is amplified by a transconductance amplifier (VFB-AMP). The inductor current information is sensed by CSPx and CSNx pins. The voltage difference is amplified by another transconductance amplifier (CS-AMP). The output of the VFB-AMP indicates the target peak inductor current. If the output voltage goes down, the TPS51221 increases the target inductor current to raise the output voltage. On the other hand, if the output voltage goes up the TPS51221 decreases the target inductor current to reduce the output voltage.

At the beginning of each clock cycle, the high-side MOSFET is turned on, or becomes *ON* state. The high-side MOSFET is turned off, or becomes *OFF* state, after the inductor current reaches the target value—which is determined by the combination value of the output of the VFB-AMP and a ramp compensation signal. The ramp compensation signal is used to prevent sub-harmonic oscillation of the inductor current control loop. The high-side MOSFET is turned on again at the next clock cycle. By repeating the operation in this manner, the controller regulates the output voltage. The synchronous low-side or the *rectifying* MOSFET is turned on each *OFF* state to keep the conduction loss minimum.

PWM FREQUENCY CONTROL

TPS51221 has a fixed frequency control scheme with 180° phase shift. The switching can be determined by an external resistor which is connected between RF pin and GND, and can be calculated using Equation 1:

$$f_{sw}[\text{kHz}] = \frac{1 \times 10^5}{\text{RF}[\text{k}\Omega]} \quad (1)$$

The TPS51221 can also synchronize to the external clock, of more than 2.5-V amplitude, by applying the signal to RF pin. The set timing of the channel-1 initiates at the raising edge (1.3V typ) of the clock, and channel-2 initiates at the falling edge (1.1V typ). Therefore, the 50% duty signal makes both channels 180° phase shift.

When the external clock synchronization is selected, the following conditions are required.

- Remove RF resistor
- Add clock signal before EN1 or EN2 turning on

The TPS51221 does NOT support switching frequency change on-the-fly. (neither from the switching frequency set by the RF resistor to the external clock, nor vice versa)

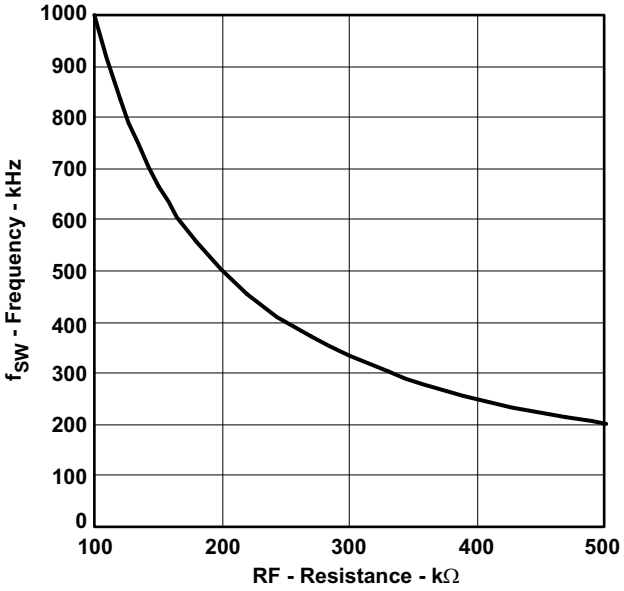


Figure 39. Switching Frequency vs RF

LIGHT LOAD OPERATION

The TPS51221 automatically reduces switching frequency at light load condition to maintain high efficiency if *Auto Skip* or *OOA* mode is selected by SKIPSELx. This reduction of frequency is achieved by skipping pulses. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its *peak* touches a predetermined current, $I_{LL(PEAK)}$, which indicates the boundary between heavy-load and light-load conditions. Once the top MOSFET is turned on, the TPS51221 does not allow turning it off until it touches $I_{LL(PEAK)}$. This eventually causes an over-voltage condition to the output, and pulse skipping. From the next pulse after zero-crossing is detected, $I_{LL(PEAK)}$ is limited by the ramp-down signal which starts from 25% of the over-current limit setting ($I_{OCL(PEAK)}$: see the CURRENT PROTECTION section) toward 5% of $I_{OCL(PEAK)}$, over one switching cycle to prevent causing a large ripple. The transition load point to the light load operation $I_{LL(DC)}$ can be calculated as follows;

$$I_{LL(DC)} = I_{LL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \quad (2)$$

$$I_{IND(RIPPLE)} = \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \quad (3)$$

where f_{SW} is the PWM switching frequency as determined by RF resistor setting or external clock. Switching frequency versus output current in the light load condition is a function of L, f, Vin and Vout; but it decreases almost proportional to the output current from the $I_{LL(DC)}$ given above however, as the switching is synchronized with clock. Due to the synchronization, the switching waveform in boundary load condition (close to $I_{LL(DC)}$), appears as a sub-harmonic oscillation; however, it is the intended operation.

If SKIPSELx is tied to GND, TPS51221 works at the constant frequency of fSW, regardless of its load current.

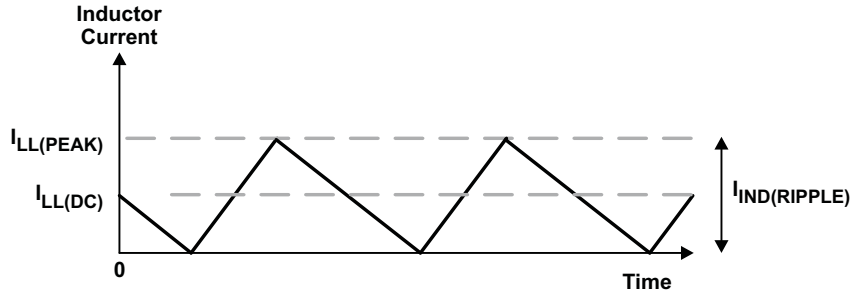


Figure 40. Boundary Between Pulse Skipping and CCM

$$I_{LL(PEAK)}Ramp = \left(0.25 - 0.2 \times \frac{V_{OUT}}{V_{IN}}\right) \times I_{OCL(PEAK)} \quad (4)$$

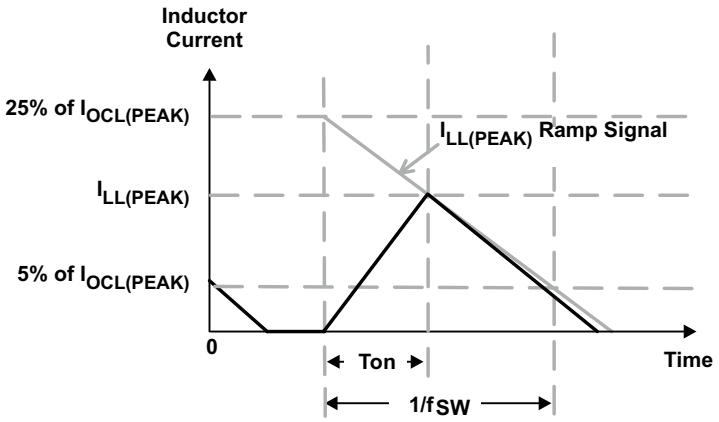


Figure 41. Inductor Current Limit at Pulse Skipping

Table 2. Skip Mode Selection

SKIPSELx	GND	VREF2	VREG3	VREG5
Operating Mode	Continuous Conduction	Auto Skip	OOA Skip (max 7 skips, for <400 kHz)	OOA Skip (max 15 skips, for equal to or greater than 400kHz)

OUT OF AUDIO SKIP OPERATION

Out-Of-Audio™ (OOA) light load mode is a unique control feature that keeps the switching frequency above acoustic audible frequencies toward virtually no-load condition while maintaining best-of-the-art high conversion efficiency. When OOA is selected, the switching frequency is kept higher than audible frequency range in any load condition. The TPS51221 automatically reduces the switching frequency at light-load conditions. OOA control circuit monitors the states of both MOSFETs and forces an *ON* state if a predetermined number of pulses are skipped. This means that the high-side MOSFET is turned on before the output voltage declines down to the target value, so that eventually an over-voltage condition is caused. The OOA control circuit detects this over-voltage condition and begins modulating the skip-mode on-time to keep the output voltage.

The TPS51221 supports a wide switching frequency range; therefore, OOA skip mode has two selections; see Table 2. When 300 kHz switching frequency is selected, max 7 skip (SKIPSEL=3.3V) makes lowest frequency at 37.5kHz. If max 15 skip is chosen, it becomes 18.8kHz; hence, max 7 skip is suitable for less than 400 kHz, and max 15 skip is for equal to or greater than 400 kHz.

99% DUTY CYCLE OPERATION

In a low-dropout condition such as 5-V input to 5-V output, the basic control loop attempts to maintain 100% of the high-side MOSFET *ON*. However, with the N-channel MOSFET used for the top switch, it is not possible to use the 100% on-cycle to charge the boot strap capacitor. When high duty is required, the TPS51221 extends the *ON* period (by skipping a maximum of three clock cycles and reducing the switching frequency to 25% of the steady state value) and asserts the *OFF* state after extended *ON.*

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current, low $r_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which is 1.7 Ω for VBSTx to DRVHx, and 1.0 Ω for DRVHx to SWx. When configured as a floating driver, 5V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by the flying capacitor between VBSTx and SWx pins. The average drive current is equal to the gate charge at Vgs=5V times the switching frequency. This gate drive current, as well as the low-side gate drive current times 5V, produces the driving power which needs to be dissipated from the TPS51221 package. A dead time to prevent shoot-through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on.

LOW-SIDE DRIVER

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance, which is 1.3Ω for VREG5 to DRVLx, and 0.7 Ω for DRVLx to GND. The 5-V bias voltage is delivered from VREG5 supply. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND. The average drive current is also calculated by the gate charge at Vgs=5V times switching frequency.

CURRENT SENSING SCHEME

In order to provide both good accuracy and cost effective solution, the TPS51221 supports external resistor sensing and inductor DCR sensing. An RC network with high quality X5R or X7R ceramic capacitor should be used to extract voltage drop across DCR. A value of 0.1µF is a good design start. CSPx and CSNx should be connected to positive and negative terminal of the sensing device, respectively. The TPS51221 has an internal current amplifier. The gain of the current amplifier, Gc, is selected by TRIP terminal. In any setting, the output signal of the current amplifier becomes 100mV at the OCL setting point. This means that the current sensing amplifier normalizes the current information signal based on the OCL setting. Attaching an RC network is recommended even with a resistor sensing scheme to get accurate current sensing; see section EXTERNAL PARTS SELECTION for detailed configurations.

CURRENT PROTECTION

The TPS51221 has cycle-by-cycle over-current limiting control. If the inductor current becomes larger than the over-current trip level, TPS51221 turns off the high-side MOSFET, turns on the low-side MOSFET and waits for the next clock cycle.

$I_{OCL(PEAK)}$ sets peak level of the inductor current. Thus, the DC load current at over-current threshold, $I_{OCL(DC)}$, can be calculated as follows;

$$I_{OCL(DC)} = I_{OCL(PEAK)} - 0.5 \times I_{IND(RIPPLE)} \quad (5)$$

$$I_{OCL(PEAK)} = \frac{V_{OCL}}{R_{SENSE}} \quad (6)$$

where

- where R_{SENSE} is resistance of the current-sensing device
- V_{OCL} is the over-current trip threshold voltage, as determined by TRIP pin voltages (shown in Table 3)

Table 3. OCL Trip and Discharge Selection

TRIP	GND	VREF2	VREG3	VREG5
V_{OCL} (OCL Trip voltage)	$V_{OCL-ULV}$ (Ultra Low Voltage)		V_{OCL-LV} (Low Voltage)	
Discharge	Enable	Disable	Disable	Enable

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus, the output voltage tends to fall down and ultimately crosses the under-voltage protection threshold, resulting in shutdown.

POWER GOOD

The TPS51221 has a power-good output for both switcher channels. The power-good function is activated after softstart has finished. If the output voltage comes within ±5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after 1ms internal delay. If the output voltage goes outside of ±10% of the target value, the power-good signal becomes low after 1.5µs internal delay. Voltage applied should be less than 6V and the recommended pull-up resistance value is from 100kΩ to 1MΩ.

OUTPUT DISCHARGE CONTROL

The TPS51221 discharges output when ENx is low. The TPS51221 discharges outputs using an internal MOSFET connected to CSNx and GND. The current capability of these MOSFETs is limited to discharge the output capacitor slowly. If ENx becomes high during discharge, the MOSFETs are turning off, and some output voltage remains. SMPS changes over to soft-start. PWM will begin after the target voltage overtakes the remaining output voltage. This function can be disabled as shown in Table 3.

CURRENT MONITOR

The TPS51221 monitors the output current as the voltage difference between CSPx and CSNx terminal. The transconductance amplifier (CS-AMP) amplifies this differential voltage 100 times when V_{OCL} is set V_{OCL_ULV}, 50 times when V_{OCL} is set V_{OCL_LV}, and sends out from IMON1 thermal. This function is only for the channel 1 output and adding an RC filter is recommended.

OVER/UNDER VOLTAGE PROTECTION

The TPS51221 monitors the output voltage to detect over- and under-voltage. When the output voltage becomes 15% higher than the target value, the OVP comparator output goes high, and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON, and shuts off another channel.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, the TPS51221 latches OFF both high-side and low-side MOSFETs, and shuts off another channel. This UVP function is enabled after soft start has completed. The procedures for restarting from these protection states are:

(1) toggle EN,
(2) toggle EN1 and EN2 or
(3) once be hit UVLO

UVLO PROTECTION

TPS51221 has under-voltage lock out protection (UVLO) for VREG5, VREG3 and VREF2. When the voltage is lower than UVLO threshold voltage, the TPS51221 shuts off each output as shown in Table 4. This is non-latch protection.

Table 4. UVLO Protection

	CH1/ CH2	VREG5	VREG3	VREF2
VREG5 UVLO	Off	—	On	On
VREG3 UVLO	Off	Off	—	Off
VREF2 UVLO	Off	Off	On	—

THERMAL SHUTDOWN

TPS51221 monitors the temperature of itself. If the temperature exceeds the threshold value TPS51221 shuts off both SMPS, 5V-LDO and decreases VREG3 current limitation to 5 mA (typically). This is non-latch protection.

APPLICATION INFORMATION

EXTERNAL PARTS SELECTION

A buck converter using TPS51221 consists of linear circuits and a switching modulator. Figure 42 shows basic scheme.

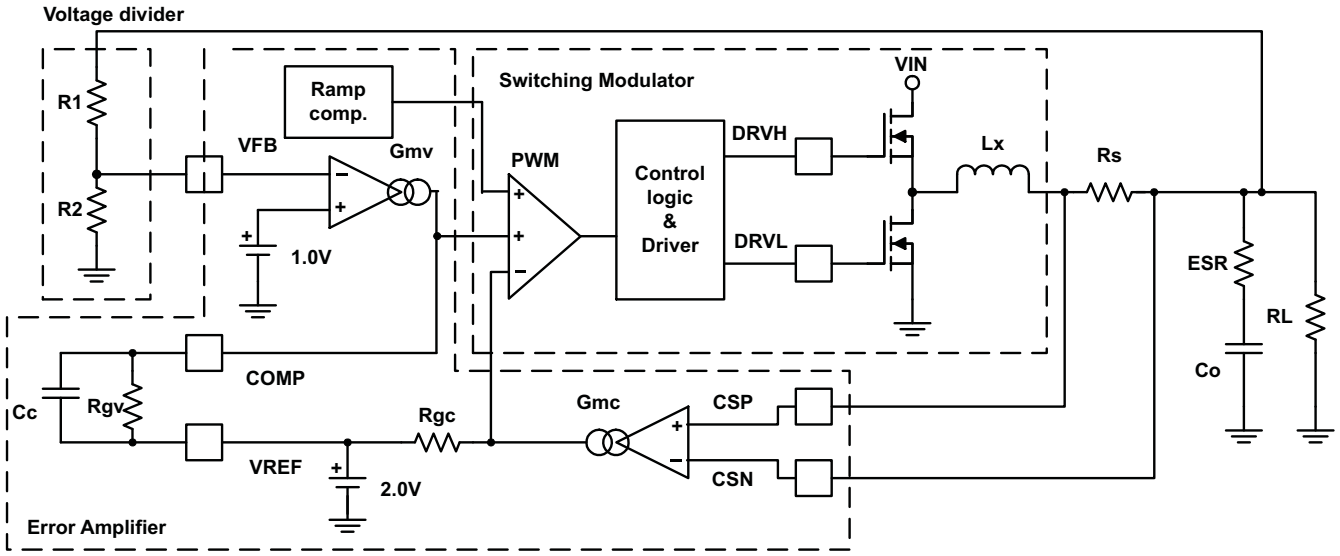


Figure 42. Simplified Current Mode Functional Blocks

The external components can be selected by following manner.

1. Determine output voltage dividing resistors (R1 and R2: shown in Figure 42) using the next equation

$$R1 = \left(V_{OUT} - 1.0\right) \times R2 \quad (7)$$

2. **Determine switching frequency.** Higher frequency allows smaller output capacitances; however, efficiency is degraded due to increase of switching loss. Frequency setting resistor for RF-pin can be calculated by;

$$RF[k\Omega] = \frac{1 \times 10^5}{f_{sw}\,[kHz]} \quad (8)$$

3. **Choose the inductor.** The inductance value should be determined to give the ripple current of approximately 25% to 50% of maximum output current. Recommended ripple current rate is about 30% to 40% at the typical input voltage condition. The next equation uses 33%.

$$L = \frac{1}{0.33 \times I_{OUT(MAX)} \times f_{SW}} \times \frac{\left(V_{IN(TYP)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(TYP)}} \quad (9)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

4. **Determine the OCL trip voltage threshold, V_{OCL}, and select the sensing resistor.** The OCL trip voltage threshold is determined by TRIP pin setting. Using a larger value improves the S/N ratio. Determine the sensing resistor using next equation. $I_{OCL(PEAK)}$ should be approximately 1.5 × $I_{OUT(MAX)}$ to 1.7 × $I_{OUT(MAX)}$.

$$R_{SENSE} = \frac{V_{OCL}}{I_{OCL(PEAK)}} \quad (10)$$

5. **Determine Rgv.** Rgv should be determined from preferable droop compensation value and is given by the next equation, based on the typical number of Gmv=500μS.

$$Rgv = 0.1 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times V_{OUT} \times \frac{1}{Gmv \times Vdroop} \quad (11)$$

$$Rgv[k\Omega] = 200 \times \frac{I_{OUT(MAX)}}{I_{OCL(PEAK)}} \times \frac{V_{OUT}[V]}{Vdroop[mV]} \quad (12)$$

6. Determine output capacitance C_o to achieve stable operation using the next equation. The 0 dB frequency; f_o should be kept under 1/3 of the switching frequency.

$$f_0 = \frac{5}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{Co} < \frac{fsw}{3} \quad (13)$$

$$Co > \frac{15}{\pi} \times I_{OCL(PEAK)} \times \frac{1}{V_{OUT}} \times \frac{Gmv \times Rgv}{fsw} \quad (14)$$

7. **Calculate Cc.** Purpose of this capacitance is to cancel zero caused by *ESR* of the output capacitor. When using ceramic capacitor(s), there is no need for Cc. If a combination of different capacitors are used, attaching an RC network circuit might be needed instead of single capacitance to cancel zeros and poles caused by the output capacitors. In the case of a single capacitance, Cc is given in Equation 15.

$$Cc = Co \times \frac{ESR}{Rgv} \quad (15)$$

8. **Choose MOSFETs.** Generally, the on resistance strongly affects efficiency at high load conditions as a conduction loss. In case of low output voltage application, the duty ratio is not so high so that the on resistance of high-side MOSFET does not greatly affect efficiency. However, switching speed (Tr and Tf) affects efficiency as a switching loss. As for low-side MOSFET, usually switching loss is not a main portion of the total loss.

RESISTOR CURRENT SENSING

For more accurate current sensing with an external resistor, the following technique is recommended. Adding RC filtering to cancel the parasitic inductance of the resistor; this filter value can be calculated using Equation 16.

$$Cx \times Rx = \frac{Lx}{Rs} \quad (16)$$

This equation means the time-constant of Cx and Rx should match the one of Lx (ESL) and Rs.

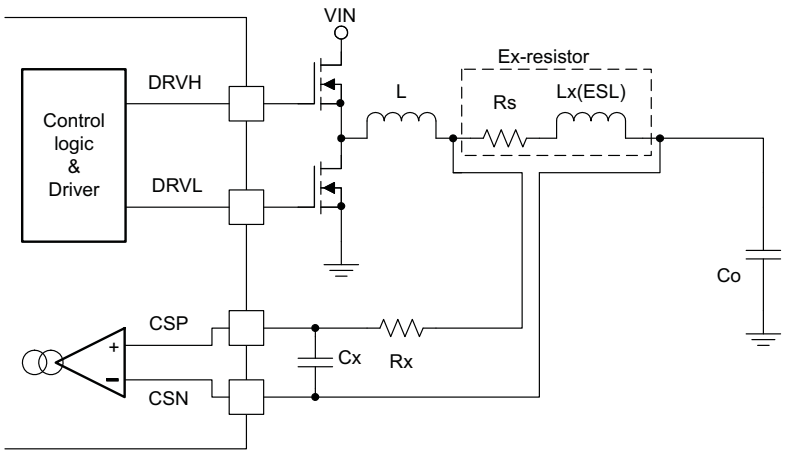


Figure 43. External Resistor Current Sensing

INDUCTOR DCR CURRENT SENSING

To use an inductor DCR as current sensing resistor (Rs), the configuration needs to change, as shown in Figure 44. However, the equation must be satisfied the same as the one using resistor sensing.

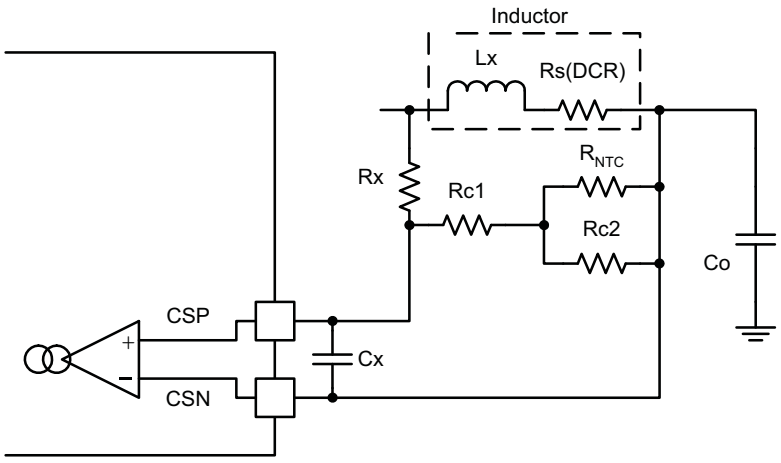


Figure 44. Inductor DCR Current Sensing

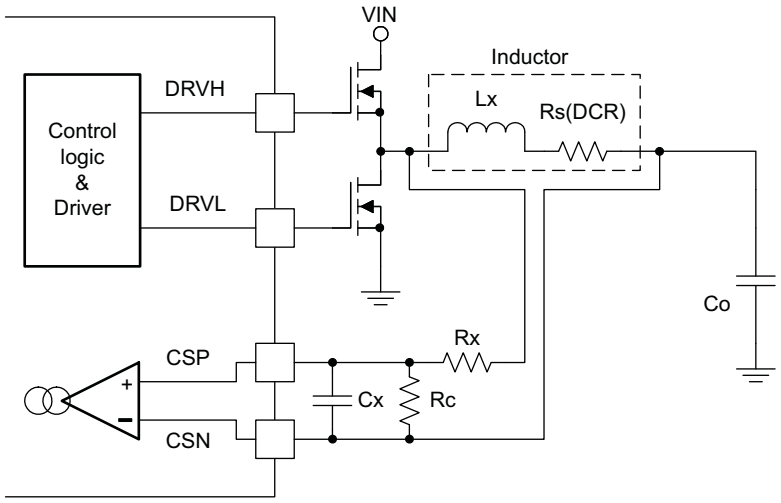


Figure 45. Inductor DCR Current Sensing With Voltage Divider

The TPS51221 has a fixed V_{OCL} point (60 mV or 30 mV). In order to adjust for DCR, a voltage divider can be configured as shown in Figure 45.

For Rx, Rc and Cx can be determined as below, and over-current limitation value can be calculated as follows.

$$Cx \times (Rx \,//\, Rc) = \frac{Lx}{Rs} \tag{17}$$

$$I_{OCL(PEAK)} = V_{OCL} \times \frac{1}{Rs} \times \frac{Rx + Rc}{Rc} \tag{18}$$

Figure 50 shows the compensation technique for the temperature drifts of the inductor DCR value. This scheme assumes the temperature rise at the thermistor (R_{NTC}) is directly proportional to the temperature rise at the inductor.

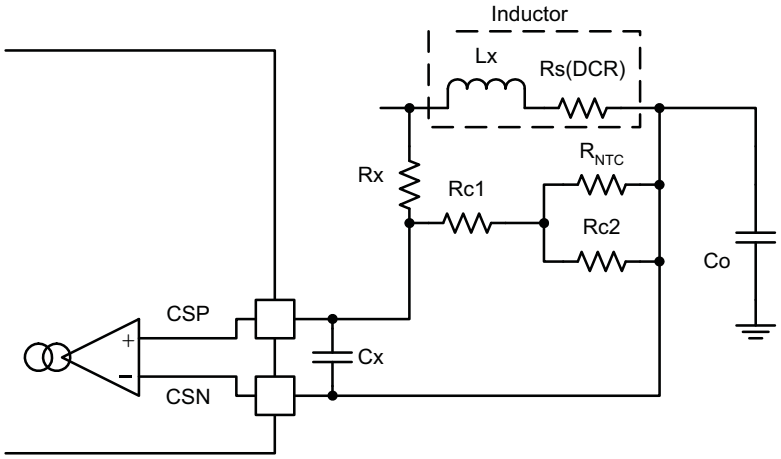


Figure 46. Inductor DCR Current Sensing With Temperature Compensation

LAYOUT CONSIDERATIONS

Certain points must be considered before starting a PCB layout work using the TPS51221.

Placement

- Place RC filters for CSP1 and CSP2 close to the IC pins.
- Place bypass capacitors for VREG5, VREG3 and VREF2 close to the IC pins.
- Place frequency-setting resistor close to the IC pin.
- Place the compensation circuits for COMP1 and COMP2 close to the IC pins.
- Place the voltage setting resistors close to the IC pins.

Routing (sensitive analog portion)

- Use separate traces for: (see Figure 47)
  - Output voltage sensing from current sensing (negative-side)
  - Output voltage sensing from V5SW input (when Vout=5V)
  - Current sensing (positive-side) from switch-node

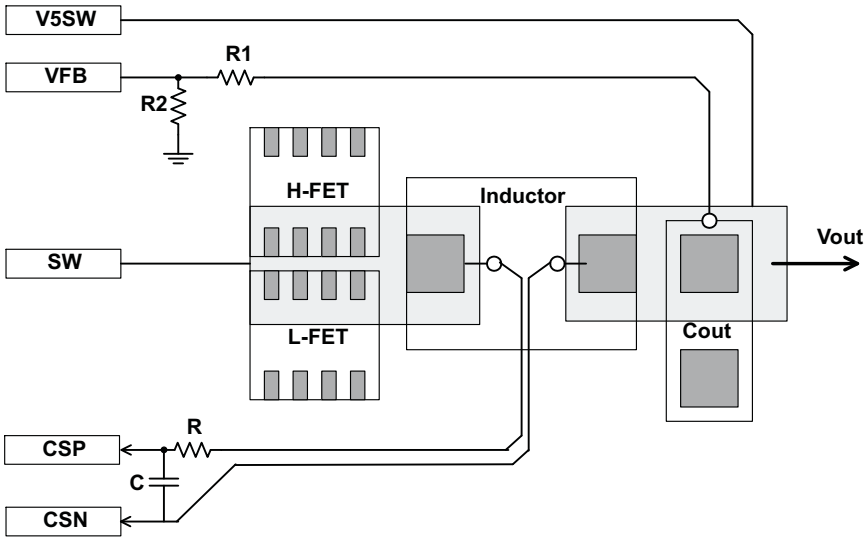


Figure 47. Sensing Trace Routings

- Use Kelvin sensing traces from the solder pads of the current sensing device (inductor or resistor) to current

sensing comparator inputs (CSPx and CSNx). (see Figure 48)

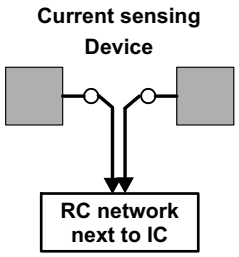


Figure 48. Current Sensing Traces

- Use small copper space for VFBx, in other words short and narrow traces to avoid noise coupling
- Connect VFB resistor trace to the positive node of the output capacitor.
- Use signal GND for VREF2 and VREG3 capacitors, RF and VFB resistors and the other sensitive analog components. Placing signal GND island (underneath the IC and fully covered peripheral components) on the internal layer for shielding purpose is recommended. (See Figure 49)
- Use thermal land for PowerPAD™. Five or more vias with 0.33-mm (13-mils) diameter connected from the thermal land to the internal GND plane should be used to help dissipation. Do NOT connect GND-pin to this thermal land on the surface layer, underneath the package.

Routing (power portion)

- Use wider/ shorter traces of DRVL for low-side gate drivers to reduce stray inductance.
- Use the parallel traces of SW and DRVH for high-side MOSFET gate drive and keep them away from DRVL.
- Connect SW trace to source terminal of the high-side MOSFET.
- Use power GND for VREG5, VIN and Vout capacitors and low-side MOSFETs. Power GND and signal GND should be connected near the IC GND terminal. (See Figure 49)

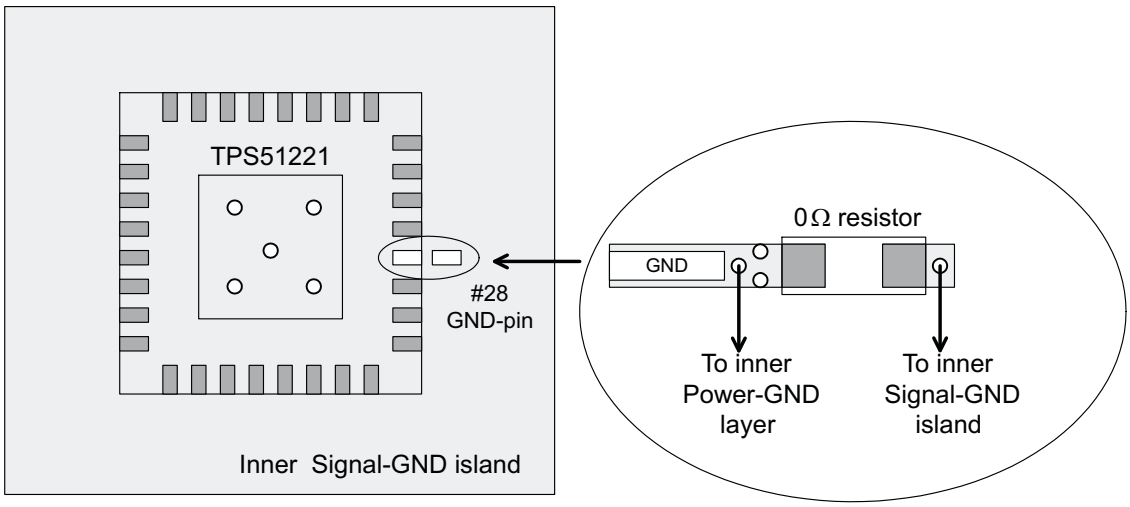


Figure 49. GND Layout Example

APPLICATION CIRCUITS

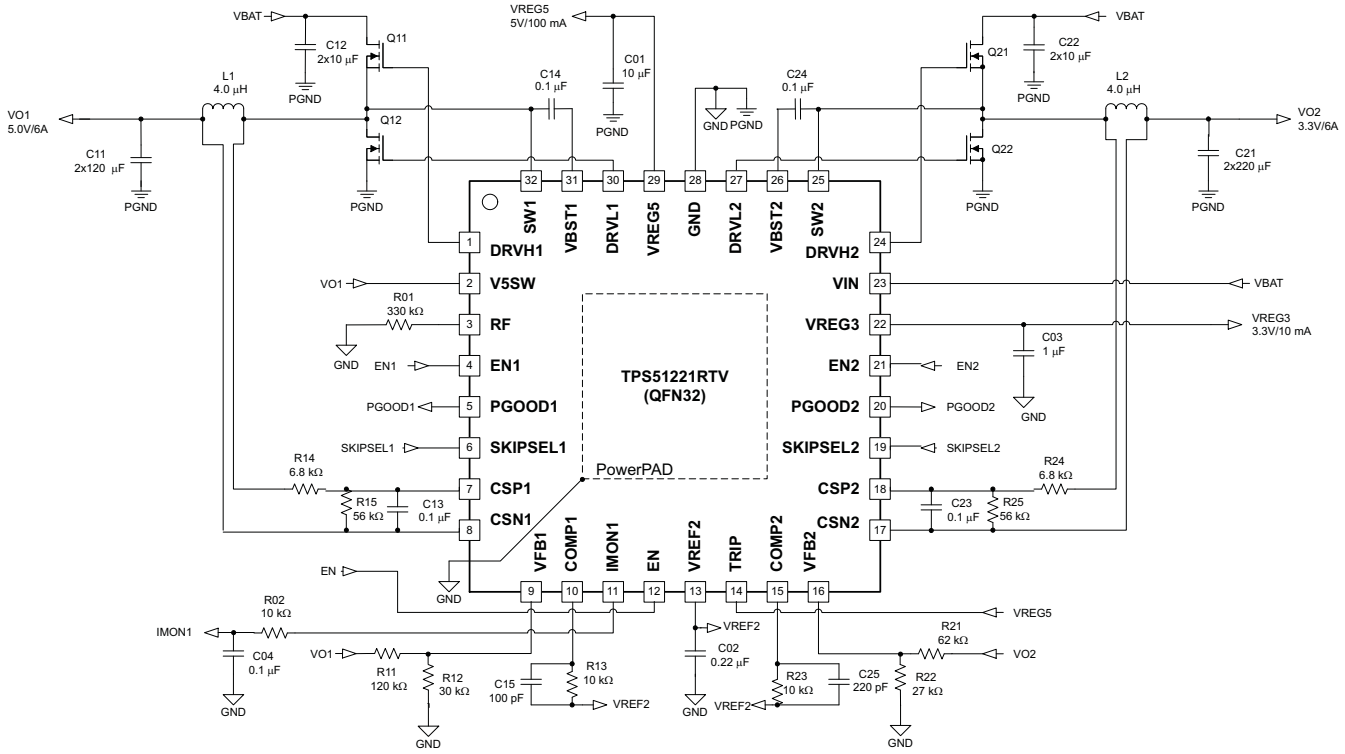


Figure 50. Current Mode, DCR Sensing, 5.0V/5A, 3.3V/5A, 300-kHz

Table 5. Current Mode, DCR Sensing, 5.0V/5A, 3.3V/5A, 300-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 × 120 µF/ 6.3 V/15-mΩ	Panasonic	EEFCX0J121R
C12	2 × 10 µF/ 25 V	Murata	GRM32DR71E106K
C21	2 × 220 µF/ 4.0 V/15-mΩ	Panasonic	EEFCX0G221R
C22	2 × 10 µF/ 25 V	Murata	GRM32DR71E106K
L1	4.0 µH, 10.3 A, 6.6-mΩ	Sumida	CEP125-4R0MC-H
L2	4.0 µH, 10.3A, 6.6-mΩ	Sumida	CEP125-4R0MC-H
Q11, Q21	30-V, 13.6-A, 9.5-mΩ	IR	IRF7821
Q12, Q22	30-V, 13.8-A, 5.8-mΩ	IR	IRF8113

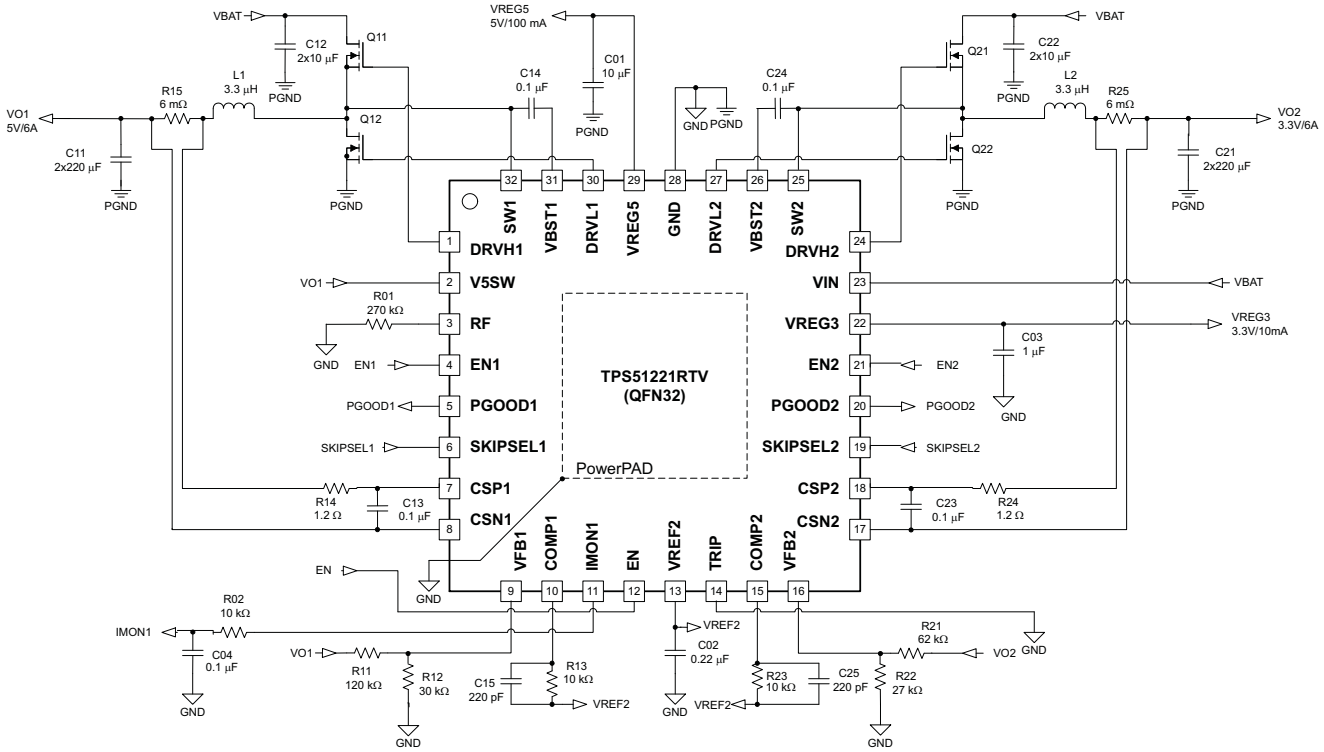


Figure 51. Current Mode, Ex-Resistor Sensing, 5.0V/5A, 3.3V/5A, 370-kHz

Table 6. Current Mode, DCR sensing, 5.0V/5A, 3.3V/5A, 370-kHz

SYMBOL	SPECIFICATION	MANUFACTURER	PART NUMBER
C11	2 x 220 µF/ 6.3 V/12-mΩ	Panasonic	EEFUE0J221R
C12	2 x 10 µF/ 25 V	Murata	GRM32DR71E106K
C21	2 x 220 µF/ 4.0 V/12-mΩ	Panasonic	EEFUE0G221R
C22	2 x 10 µF/ 25 V	Murata	GRM32DR71E106K
L1	3.3 µH, 10.3 A, 5.9-mΩ	TOKO	FDA1055-3R3M
L2	3.3 µH, 10.3 A, 5.9-mΩ	TOKO	FDA1055-3R3M
Q11, Q21	30-V, 13.6-A, 9.5-mΩ	IR	IRF7821
Q12, Q22	30-V, 13.8-A, 5.8-mΩ	IR	IRF8113

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS51221RTVR	Active	Production	WQFN (RTV) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51221
TPS51221RTVT	Active	Production	WQFN (RTV) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51221

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

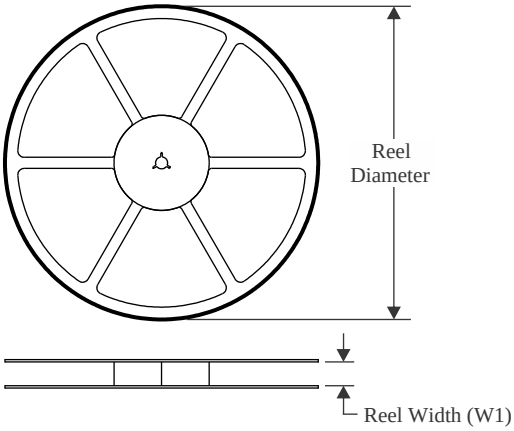
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

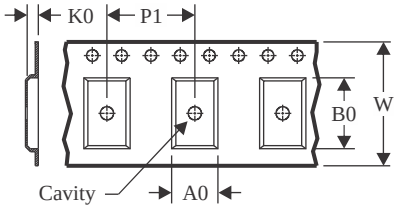
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

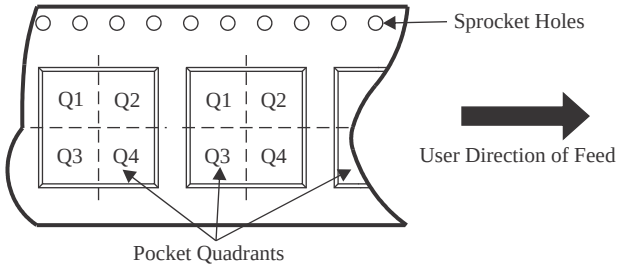


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

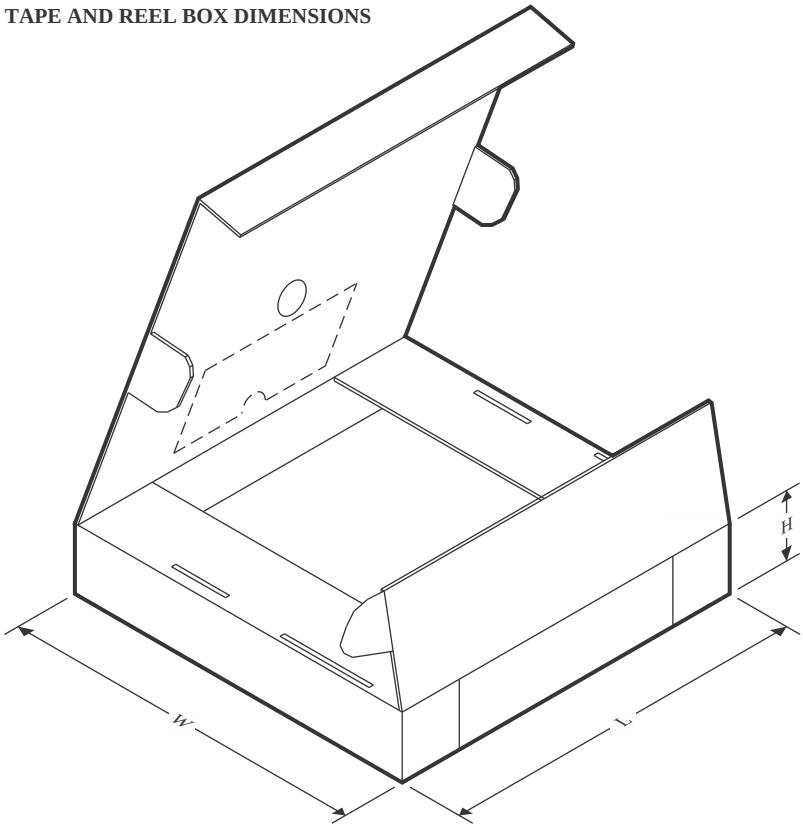
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51221RTVR	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS51221RTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

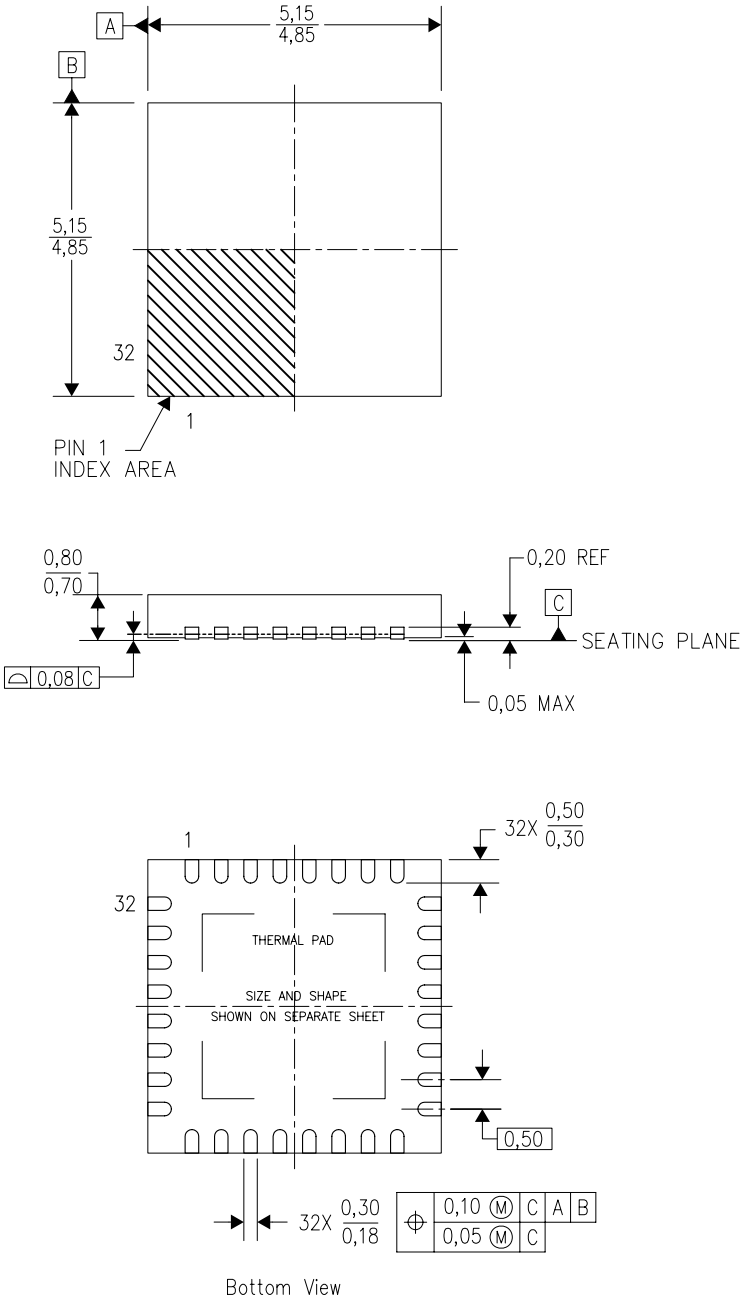
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51221RTVR	WQFN	RTV	32	3000	356.0	356.0	35.0
TPS51221RTVT	WQFN	RTV	32	250	210.0	185.0	35.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

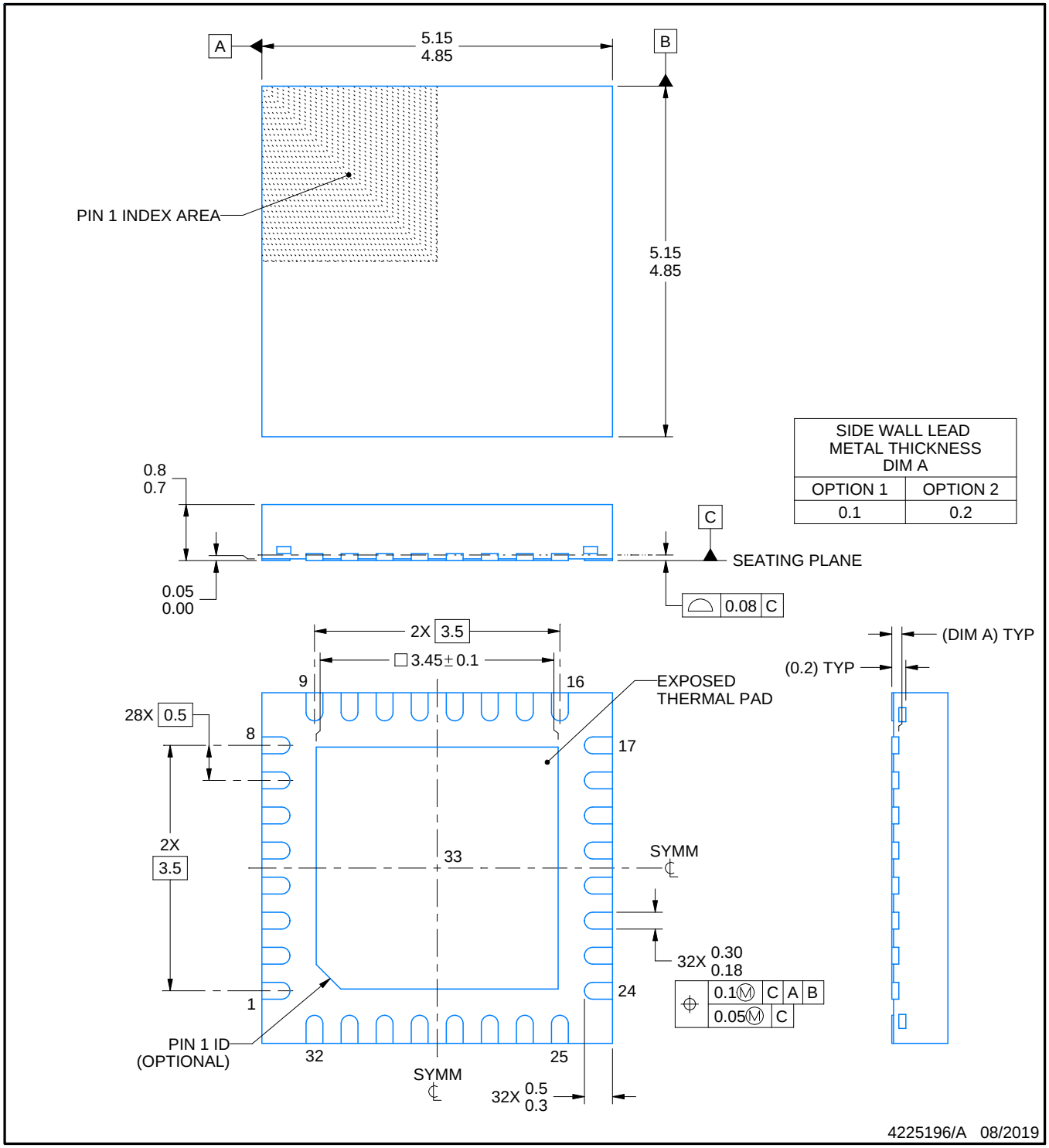
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

RTV0032E

PACKAGE OUTLINE

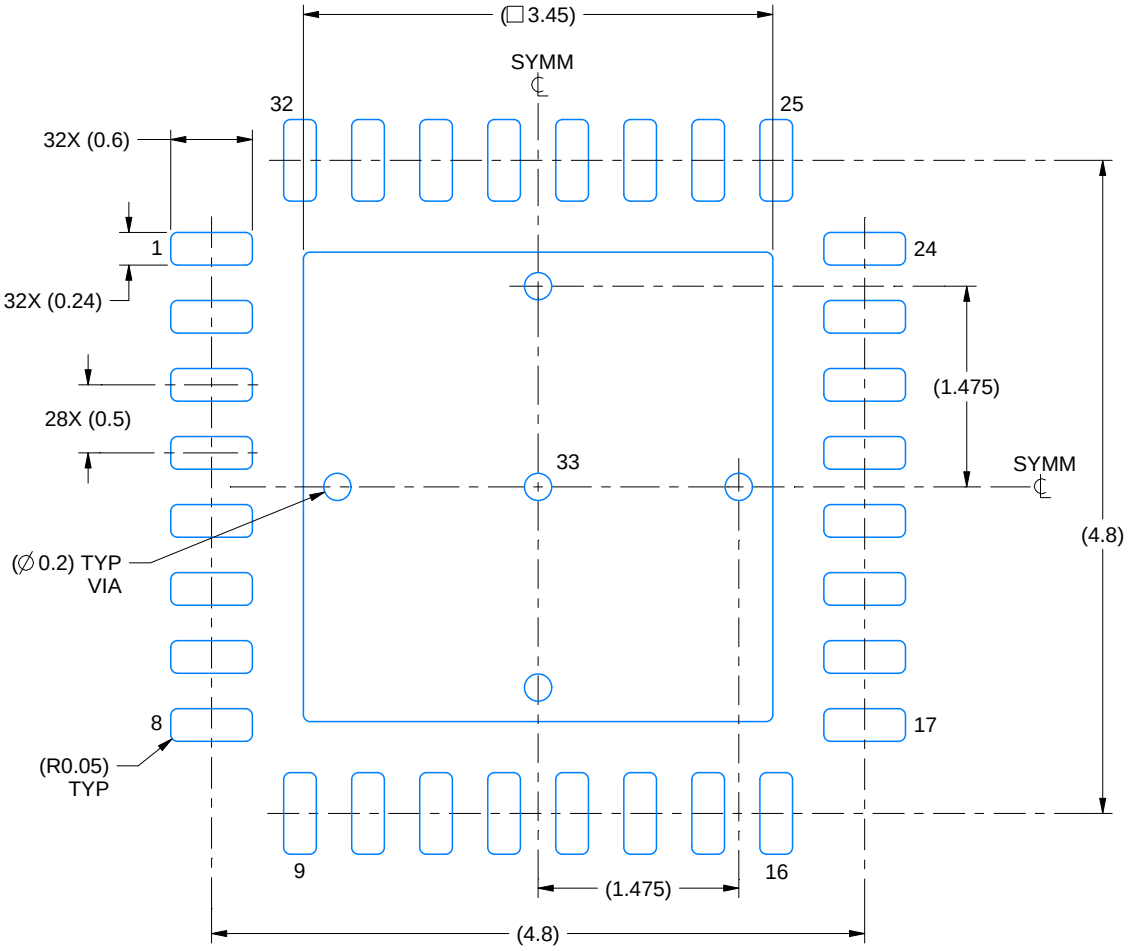
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



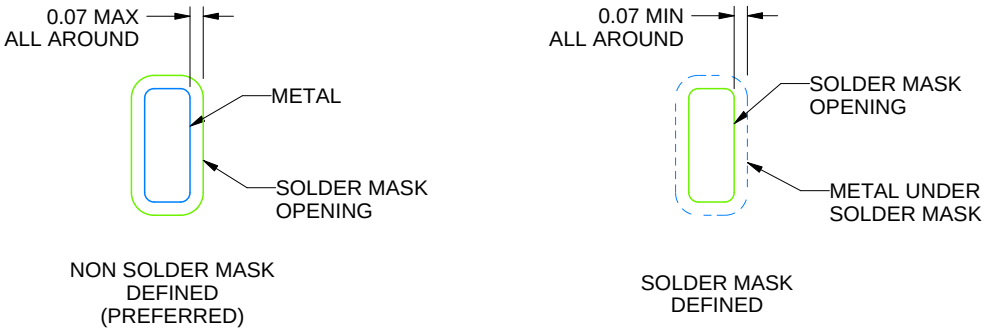
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE:18X



SOLDER MASK DETAILS

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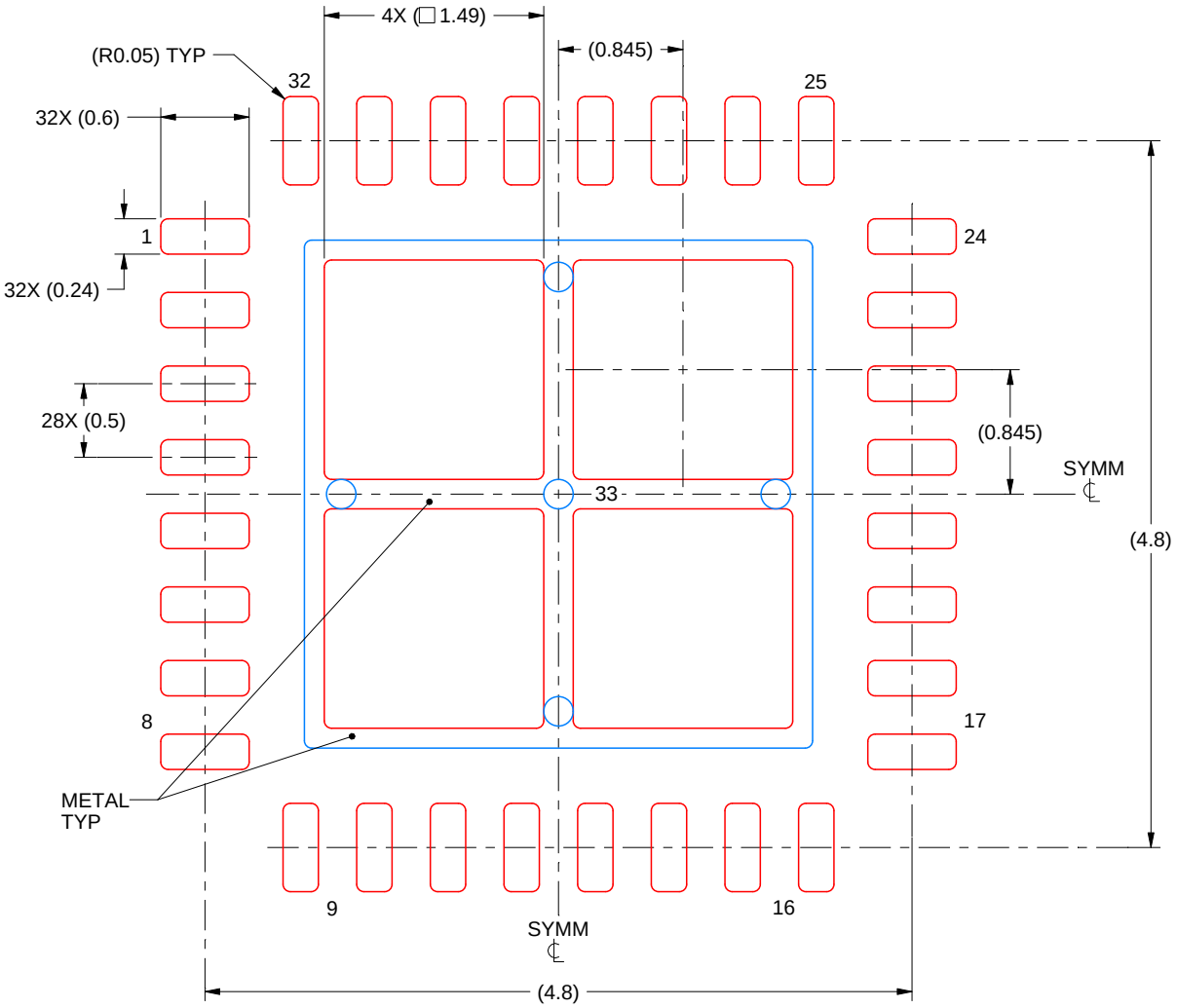
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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