

## Dual Inverter Gate

Check for Samples: [SN74LVC2GU04](#)

### FEATURES

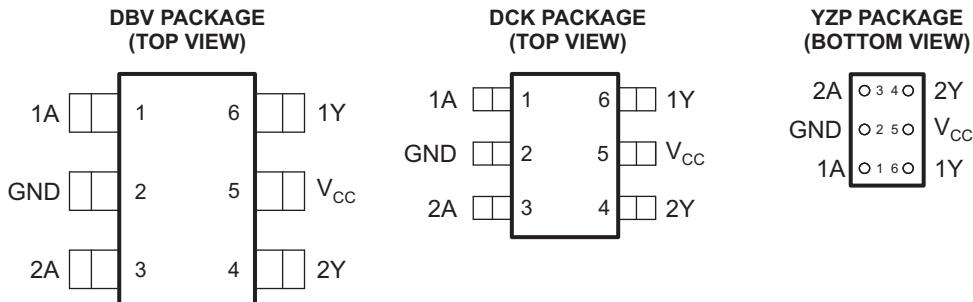
- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 3.7 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{cc}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Max of 5.5 V Down to the  $V_{CC}$  Level
- Unbuffered Outputs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### DESCRIPTION

This dual inverter is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2GU04 device contains two inverters with unbuffered outputs and performs the Boolean function  $Y = \bar{A}$ .

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.



See mechanical drawings for dimensions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

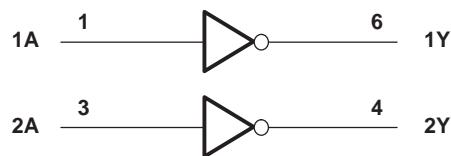


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Function Table (Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

### Logic Diagram (Positive Logic)



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DBV package	165	°C/W
		DCK package	259	
		YZP package	123	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		1.65	5.5	V
$V_{IH}$	High-level input voltage	$I_O = -100 \mu A$	$0.75 \times V_{CC}$		V
$V_{IL}$	Low-level input voltage	$I_O = 100 \mu A$		$0.25 \times V_{CC}$	V
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65 \text{ V}$		-4	mA
		$V_{CC} = 2.3 \text{ V}$		-8	
		$V_{CC} = 3 \text{ V}$		-16	
		$V_{CC} = 4.5 \text{ V}$		-24	
		$V_{CC} = 4.5 \text{ V}$		-32	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65 \text{ V}$		4	mA
		$V_{CC} = 2.3 \text{ V}$		8	
		$V_{CC} = 3 \text{ V}$		16	
		$V_{CC} = 4.5 \text{ V}$		24	
		$V_{CC} = 4.5 \text{ V}$		32	
$T_A$	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	-40°C to 85°C			-40°C to 125°C			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
$V_{OH}$	$V_{IL} = 0 \text{ V}$	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	$V_{CC} - 0.1$		$V_{CC} - 0.1$			V
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		1.2			
		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		1.9			
		$I_{OH} = -16 \text{ mA}$	3 V	2.4		2.4			
		$I_{OH} = -24 \text{ mA}$		2.3		2.3			
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		3.8			
$V_{OL}$	$V_{IH} = V_{CC}$	$I_{OL} = 100 \mu A$	1.65 V to 5.5 V		0.1		0.1		V
		$I_{OL} = 4 \text{ mA}$	1.65 V		0.45		0.45		
		$I_{OL} = 8 \text{ mA}$	2.3 V		0.3		0.3		
		$I_{OL} = 16 \text{ mA}$	3 V		0.4		0.4		
		$I_{OL} = 24 \text{ mA}$			0.55		0.55		
		$I_{OL} = 32 \text{ mA}$	4.5 V		0.55		0.55		
$I_I$	A inputs	$V_I = 5.5 \text{ V}$ or GND	0 to 5.5 V		$\pm 5$		$\pm 5$		μA
$I_{CC}$		$V_I = 5.5 \text{ V}$ or GND, $I_O = 0$	1.65 V to 5.5 V		10		10		μA
$C_I$		$V_I = V_{CC}$ or GND	3.3 V		7				pF

(1) All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**Switching Characteristics**

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC2GU04 -40°C to 85°C						UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	A	Y	1.2	5.5	1	4	1.1	3.7	1	3 ns

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

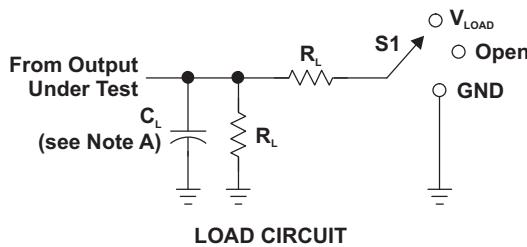
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC2GU04 –40°C to 125°C						UNIT	
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			
			MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>pd</sub>	A	Y	1.2	6.3	1	4.5	1.1	4.2	1	3.5
										ns

## Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C <sub>pd</sub> Power dissipation capacitance	f = 10 MHz	7	7	8	23	pF

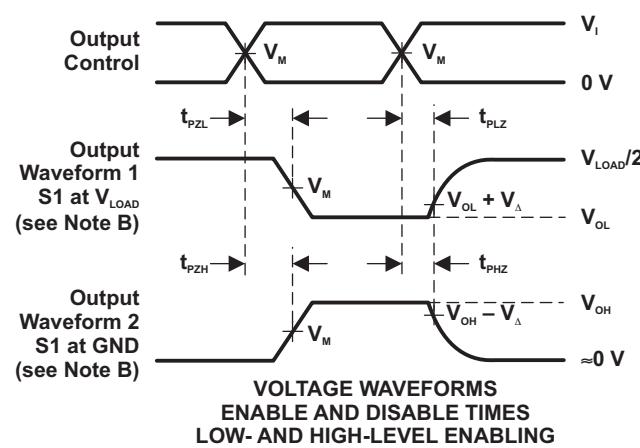
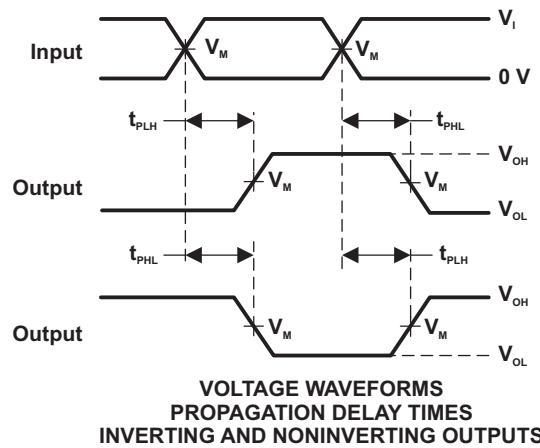
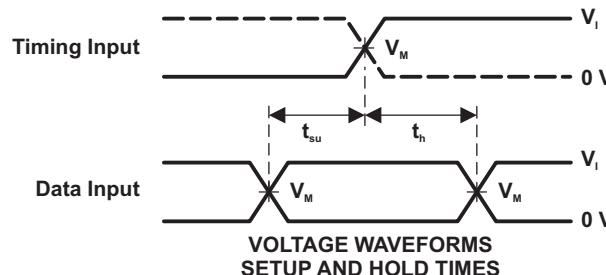
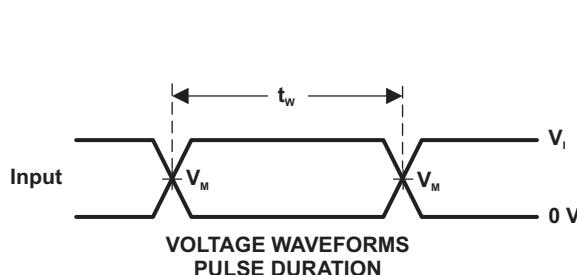
### Parameter Measurement Information



TEST	$S_1$
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

**LOAD CIRCUIT**

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_o = 50\text{ }\Omega$ .

D. The outputs are measured one at a time, with one transition per measurement.

E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## REVISION HISTORY

Changes from Revision M (February 2007) to Revision N	Page
• Updated document to new TI data sheet format. ....	1
• Removed ordering information. ....	1
• Updated Features. ....	1
• Added ESD warning. ....	2
• Updated operating temperature range. ....	3

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVC2GU04DBVRG4	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
<a href="#">74LVC2GU04DCKRG4</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD5
74LVC2GU04DCKRG4.B	Active	Production	null (null)	3000   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See 74LVC2GU04DCKRG4	CD5
<a href="#">74LVC2GU04DCKTG4</a>	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD5
74LVC2GU04DCKTG4.B	Active	Production	SC70 (DCK)   6	250   SMALL T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD5
<a href="#">SN74LVC2GU04DBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
SN74LVC2GU04DBVR.B	Active	Production	null (null)	3000   LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN74LVC2GU04DBVR	(CU45, CU4R)
<a href="#">SN74LVC2GU04DBVT</a>	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CU45, CU4R)
SN74LVC2GU04DBVT.B	Active	Production	null (null)	250   SMALL T&R	-	NIPDAU	Level-1-260C-UNLIM	See SN74LVC2GU04DBVT	(CU45, CU4R)
<a href="#">SN74LVC2GU04DCKR</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CD5, CDF, CDJ, CD K, CDR)
SN74LVC2GU04DCKR.B	Active	Production	null (null)	3000   LARGE T&R	-	SN	Level-1-260C-UNLIM	See SN74LVC2GU04DCKR	(CD5, CDF, CDJ, CD K, CDR)
<a href="#">SN74LVC2GU04DCKT</a>	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU   SN   NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CD5, CDF, CDJ, CD K, CDR)
SN74LVC2GU04DCKT.B	Active	Production	null (null)	250   SMALL T&R	-	SN	Level-1-260C-UNLIM	See SN74LVC2GU04DCKT	(CD5, CDF, CDJ, CD K, CDR)
<a href="#">SN74LVC2GU04YZPR</a>	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CDN
SN74LVC2GU04YZPR.B	Active	Production	null (null)	3000   LARGE T&R	-	SNAGCU	Level-1-260C-UNLIM	See SN74LVC2GU04YZPR	CDN

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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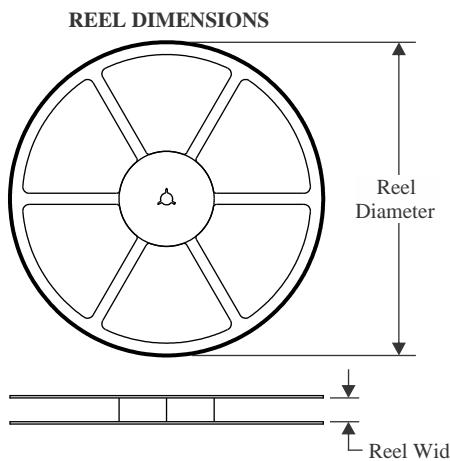
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC2GU04 :**

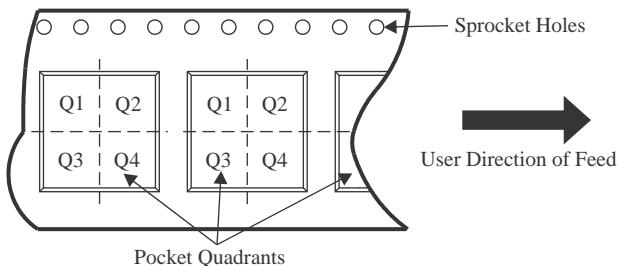
- Automotive : [SN74LVC2GU04-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

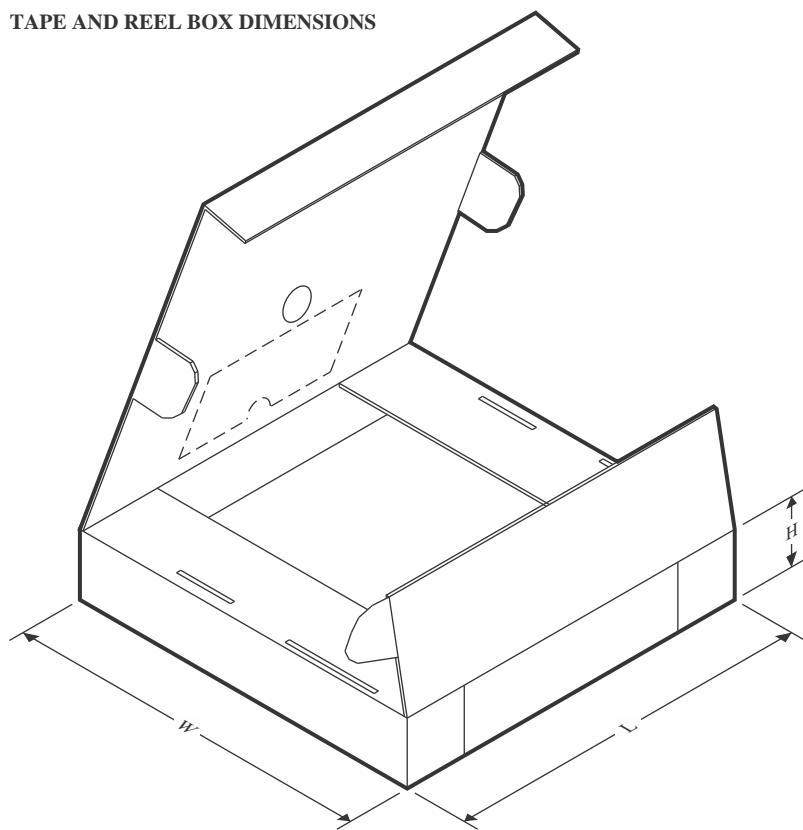
**TAPE AND REEL INFORMATION**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVC2GU04DCKRG4	SC70	DCK	6	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
74LVC2GU04DCKTG4	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC2GU04DBVR	SOT-23	DBV	6	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC2GU04DCKR	SC70	DCK	6	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC2GU04DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC2GU04DCKT	SC70	DCK	6	250	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74LVC2GU04YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVC2GU04DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0
74LVC2GU04DCKTG4	SC70	DCK	6	250	180.0	180.0	18.0
SN74LVC2GU04DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74LVC2GU04DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
SN74LVC2GU04DCKR	SC70	DCK	6	3000	210.0	185.0	35.0
SN74LVC2GU04DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
SN74LVC2GU04DCKT	SC70	DCK	6	250	210.0	185.0	35.0
SN74LVC2GU04YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

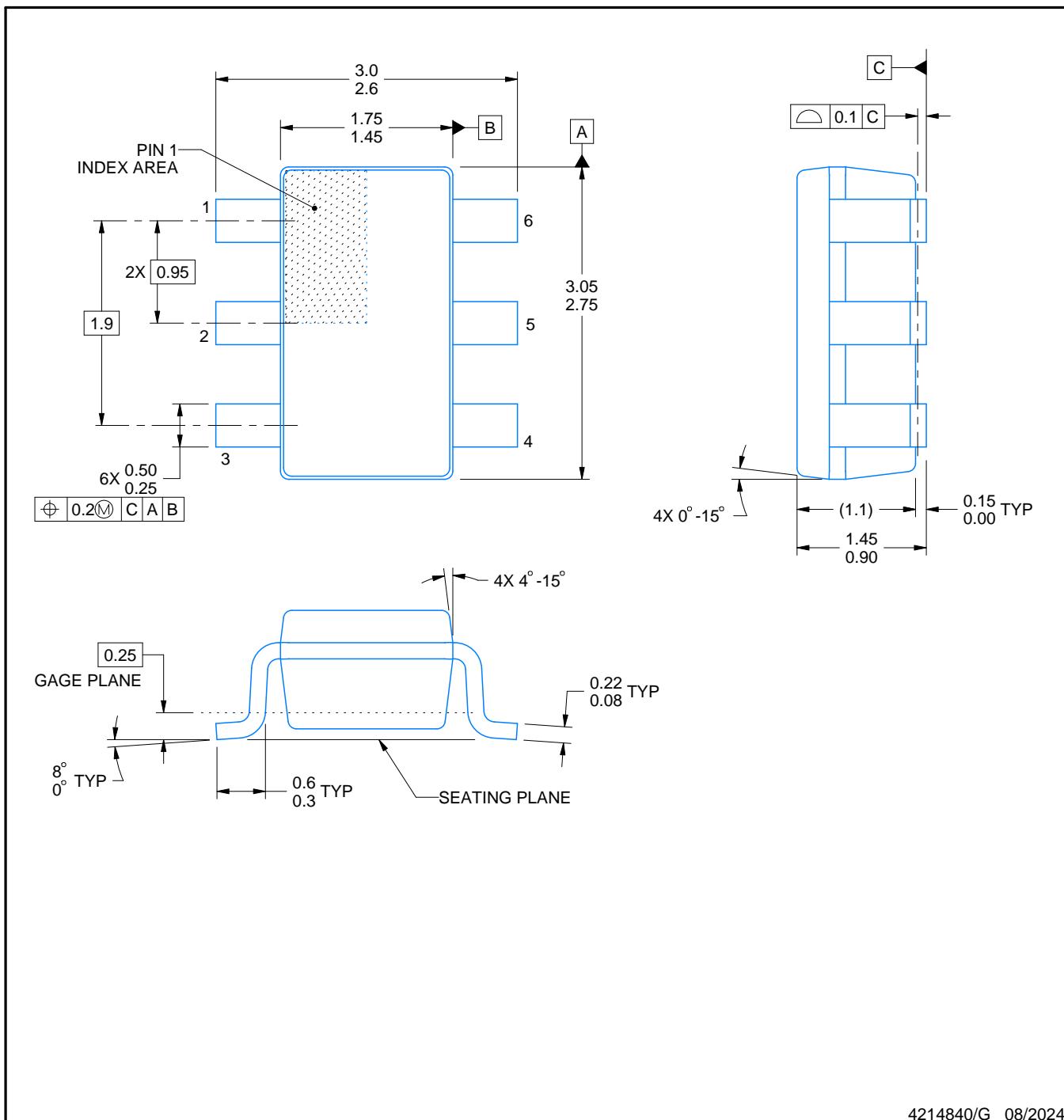
# PACKAGE OUTLINE

DBV0006A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



## NOTES:

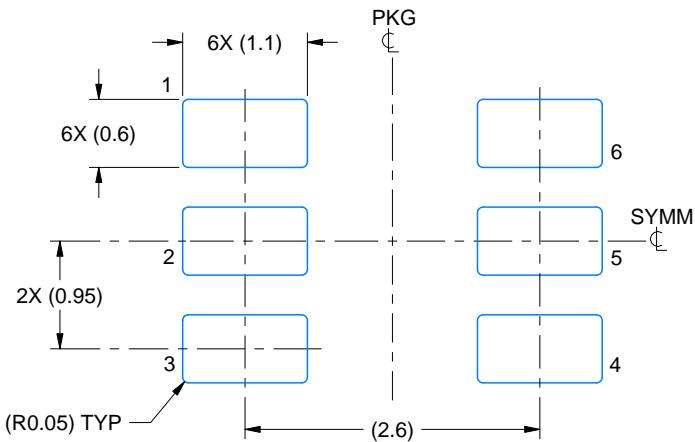
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

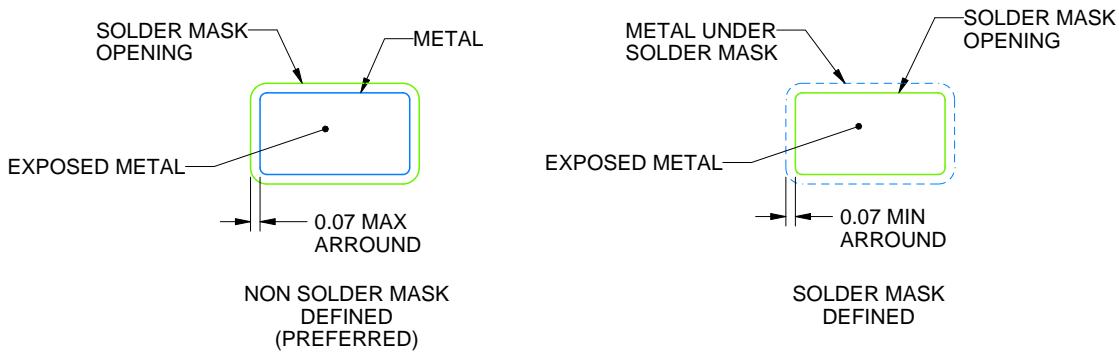
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

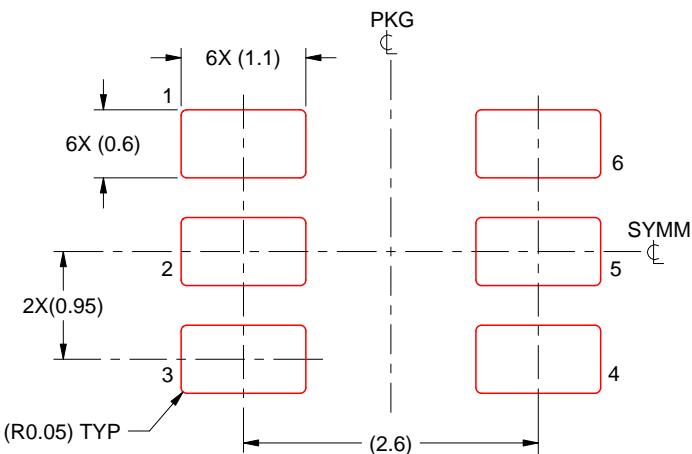
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

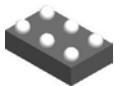


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

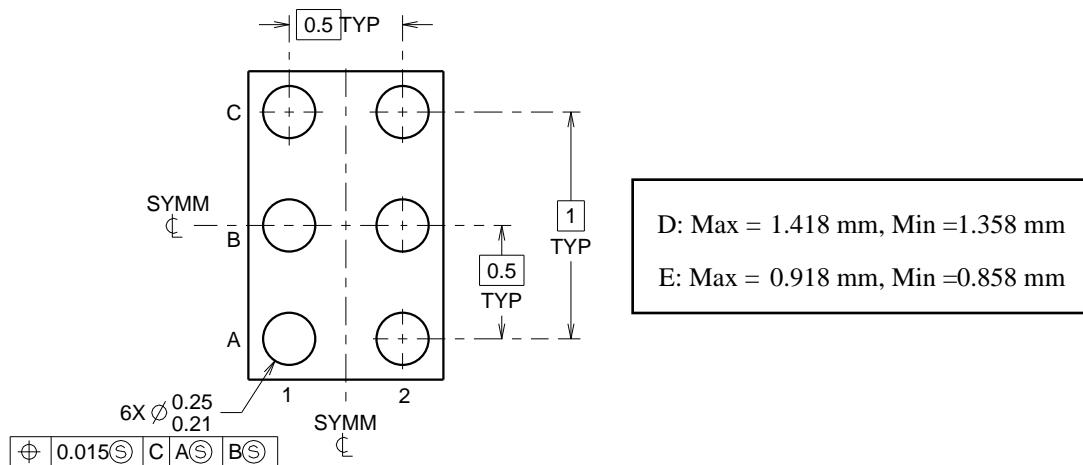
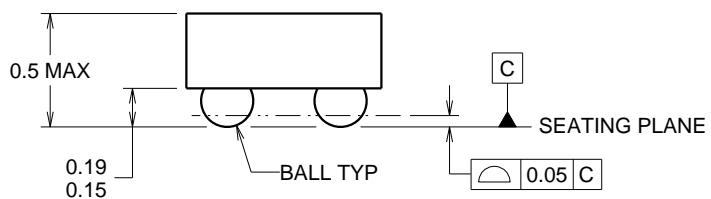
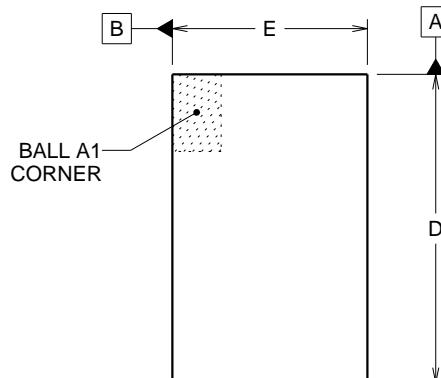


# PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree is a trademark of Texas Instruments.

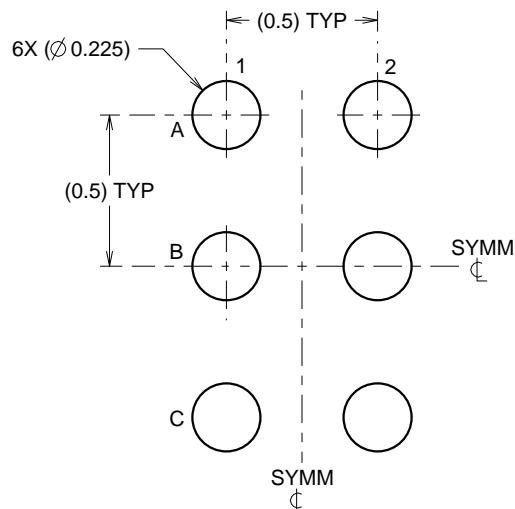
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

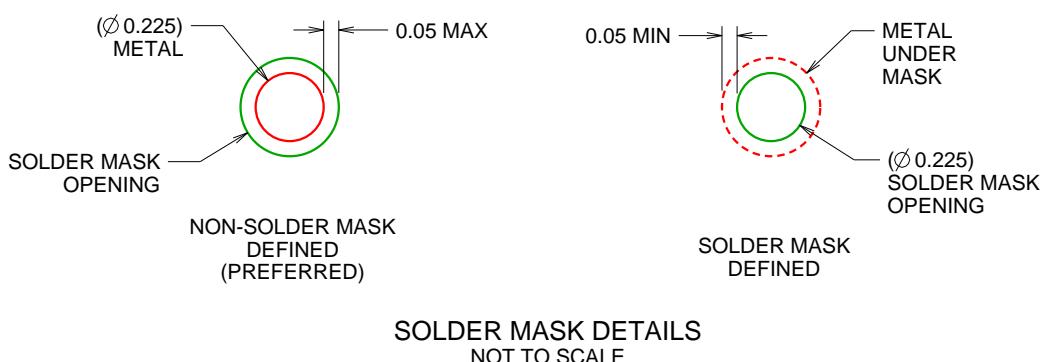
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

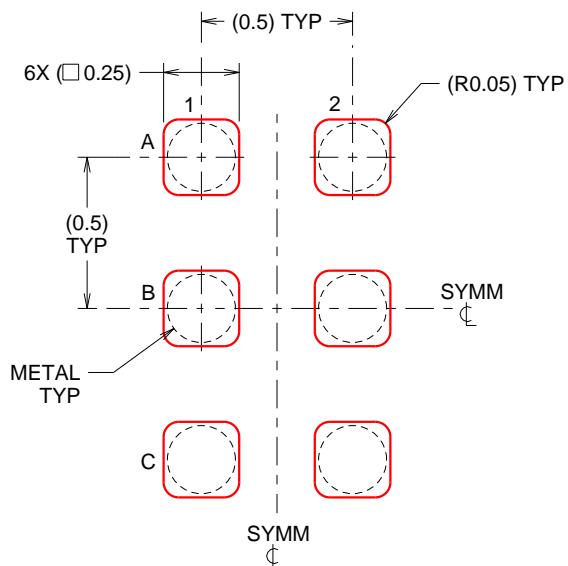
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

# EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

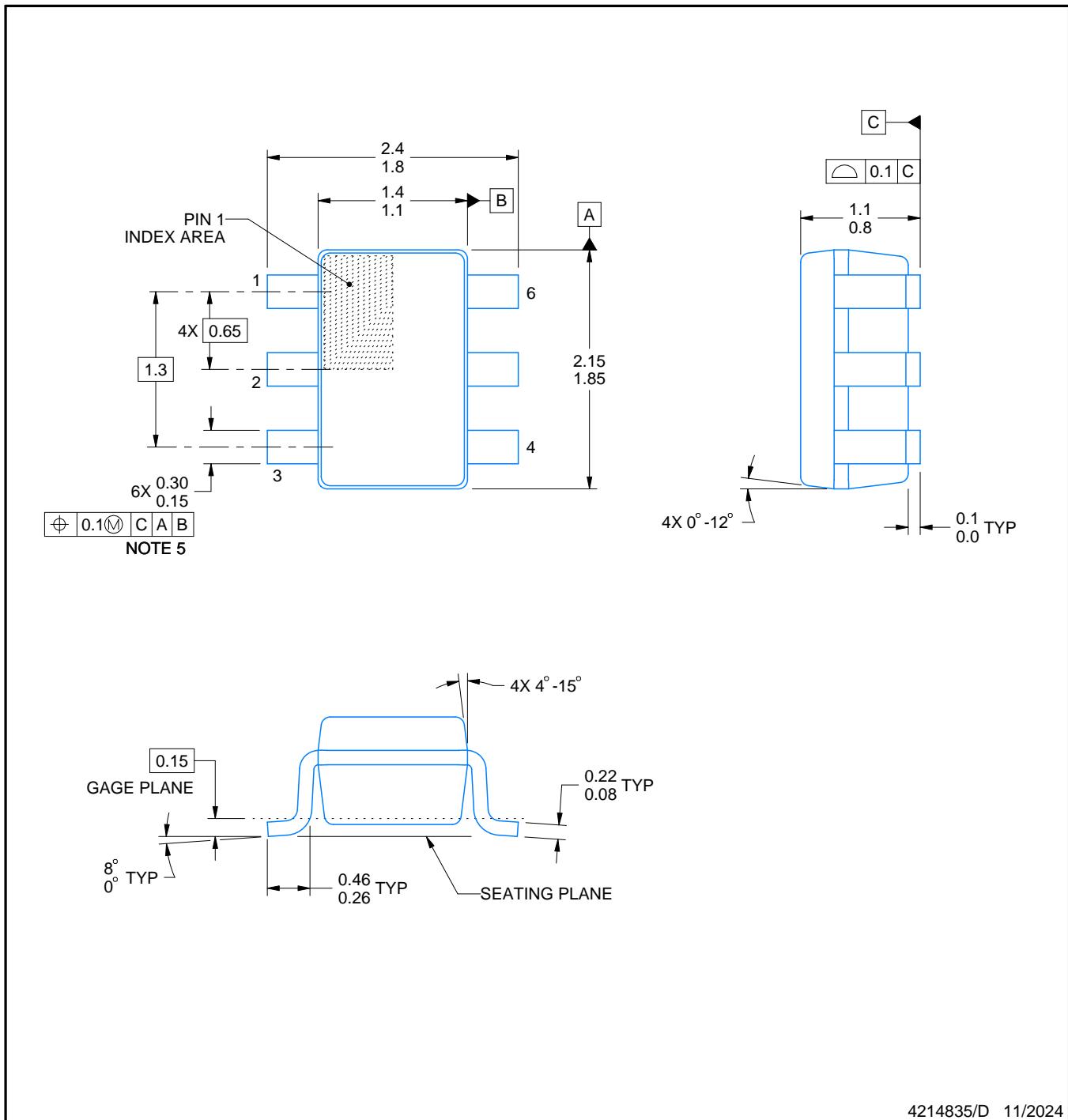
# PACKAGE OUTLINE

DCK0006A



SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



## NOTES:

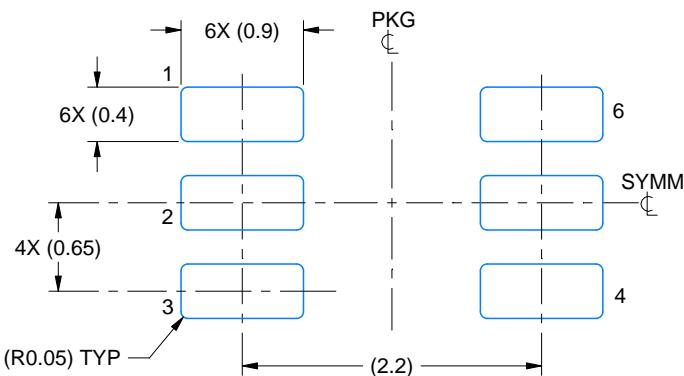
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

# EXAMPLE BOARD LAYOUT

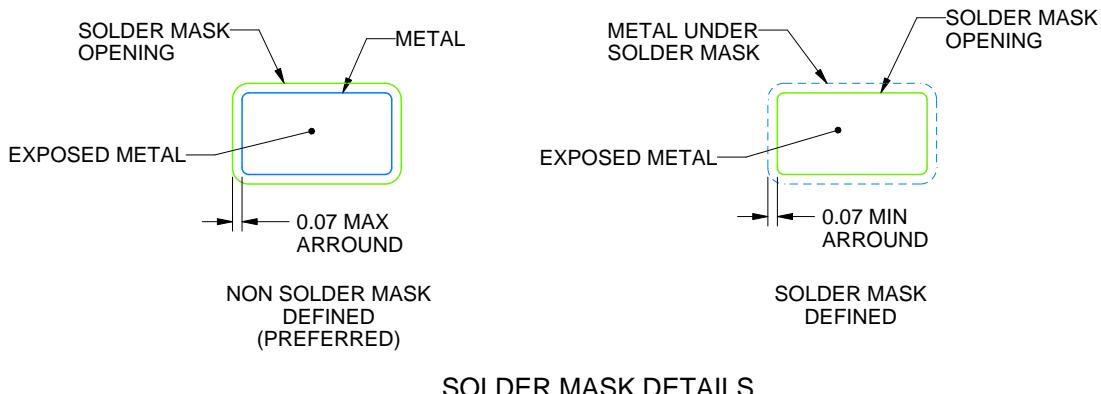
DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

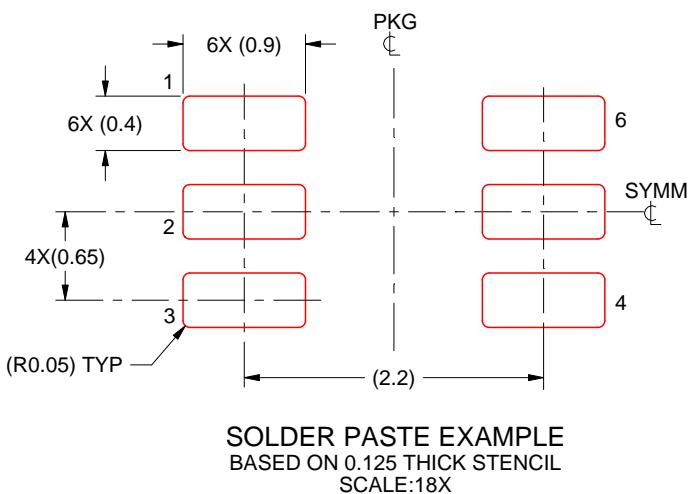
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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