

MOSFET – Single N-Channel, Logic Level, POWER trench[®]

30 V, 6.1 A, 27 mΩ

FDC855N

General Description

This N-Channel Logic Level MOSFET is an efficient solution for low voltage and battery powered applications. Utilizing onsemi's advanced POWER trench process, this device possesses minimized on-state resistance to optimize the power consumption. They are ideal for applications where in-line power loss is critical.

Features

- Max $r_{DS(on)}$ = 27 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 6.1\text{ A}$
- Max $r_{DS(on)}$ = 36 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 5.3\text{ A}$
- SUPERSOT™ –6 Package: Small Footprint (72% smaller than Standard SO–8) Low Profile (1 mm thick)
- This Device is Pb-Free and is RoHS Compliant

Application

- Power Management in Notebook, Hard Disk Drive

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

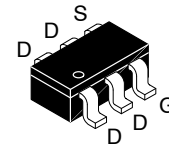
Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	Continuous (Note 1a)	6.1 A
		Pulsed	20 A
P_D	Power Dissipation (Steady State)	(Note 1a)	1.6 W
		(Note 1b)	0.8 W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

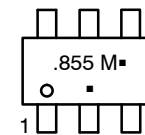
Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	30	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	$^\circ\text{C/W}$

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
30 V	27 mΩ @ 10 V	6.1 A
	36 mΩ @ 4.5 V	5.3 A



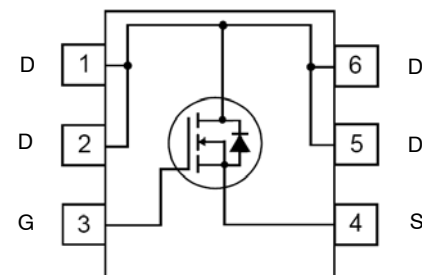
TSOT23 6-Lead
SUPERSOT™ –6
CASE 419BL

MARKING DIAGRAM



.855 = Specific Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDC855N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	24	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _C = 125°C	–	–	250	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–6	–	mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6.1 A	–	20.7	27.0	mΩ
		V _{GS} = 4.5 V, I _D = 5.3 A	–	28.2	36.0	
		V _{GS} = 10 V, I _D = 6.1 A, T _J = 125°C	–	30.1	39.3	
g _{FS}	Forward Transconductance	V _{DD} = 10 V, I _D = 6.1 A	–	20	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	–	493	655	pF
C _{oss}	Output Capacitance		–	108	145	pF
C _{rss}	Reverse Transfer Capacitance		–	62	95	pF
R _g	Gate Resistance	f = 1 MHz	–	1.0	–	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 15 V, I _D = 6.1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	6	12	ns
t _r	Rise Time		–	2	10	ns
t _{d(off)}	Turn-Off Delay Time		–	14	23	ns
t _f	Fall Time		–	2	10	ns
Q _g	Total Gate Charge at 10 V	V _{GS} = 0 V to 10 V, V _{DD} = 15 V, I _D = 6.1 A	–	9.2	13	nC
	Total Gate Charge at 5 V	V _{GS} = 0 V to 5 V, V _{DD} = 15 V, I _D = 6.1 A	–	4.9	7.0	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 15 V, I _D = 6.1 A	–	1.7	–	nC
Q _{gd}	Gate to Drain "Miller" Charge		–	3.1	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source-Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)	–	0.80	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 6.1 A, di/dt = 100 A/μs	–	17	31	ns
Q _{rr}	Reverse Recovery Charge		–	6	12	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 78°C/W when mounted on
a 1 in² pad of 2 oz. copper



b. 156°C/W when mounted on a
minimum pad of 2 oz. copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS

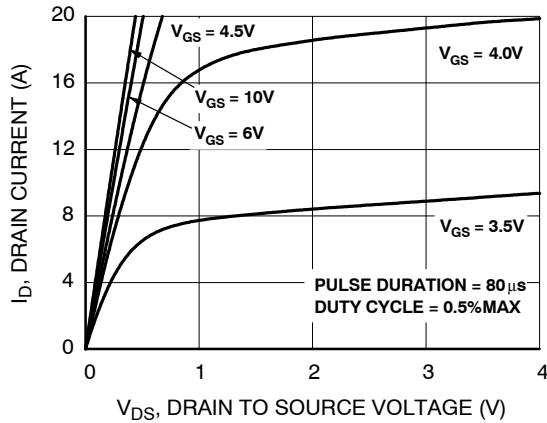
(T_J = 25°C unless otherwise noted)

Figure 1. On-Region Characteristics

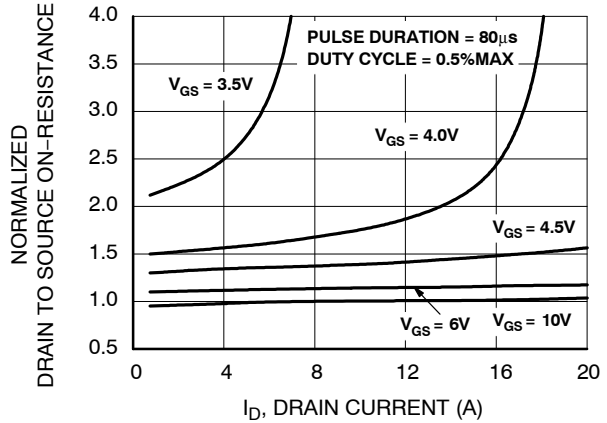


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

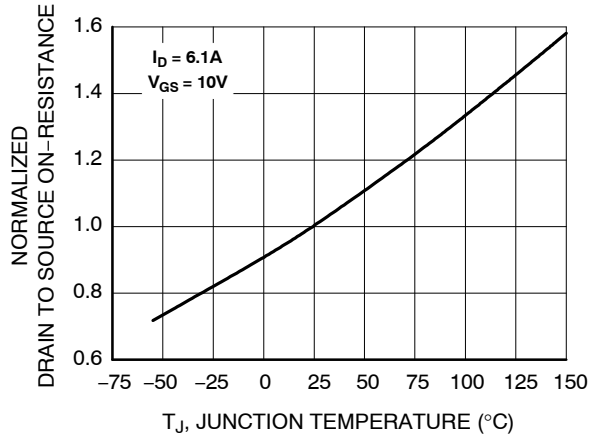


Figure 3. Normalized On-Resistance vs Junction Temperature

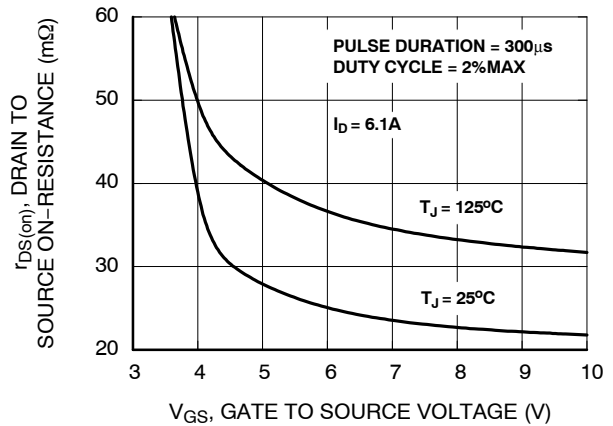


Figure 4. On-Resistance vs Gate to Source Voltage

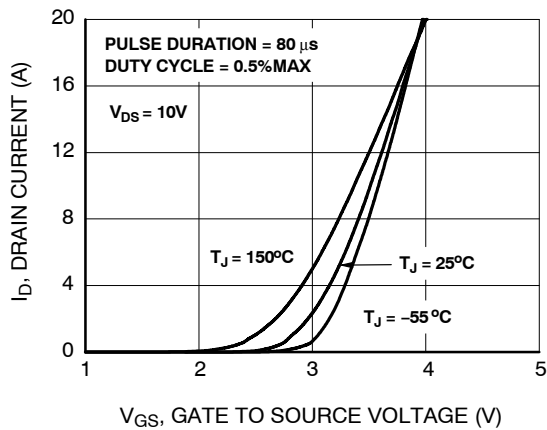


Figure 5. Transfer Characteristics

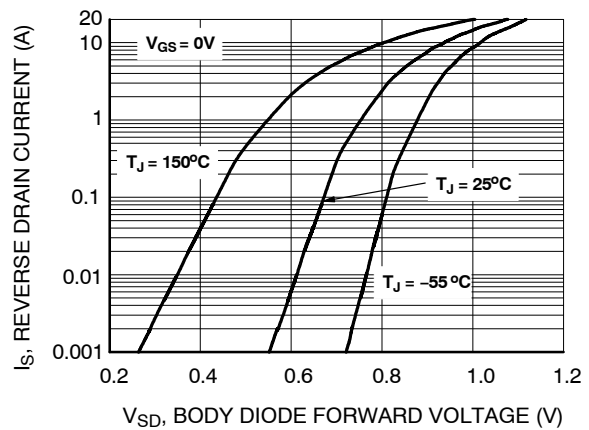


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

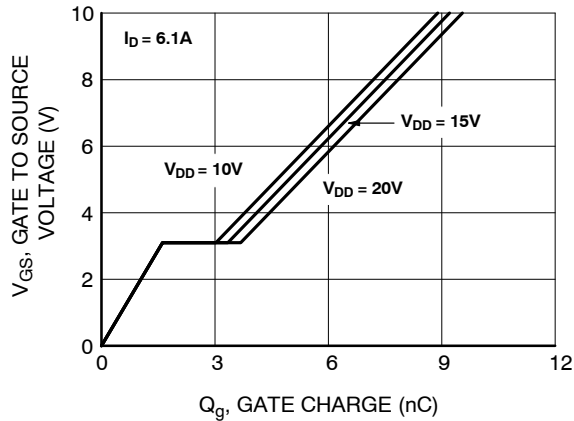


Figure 7. Gate Charge Characteristics

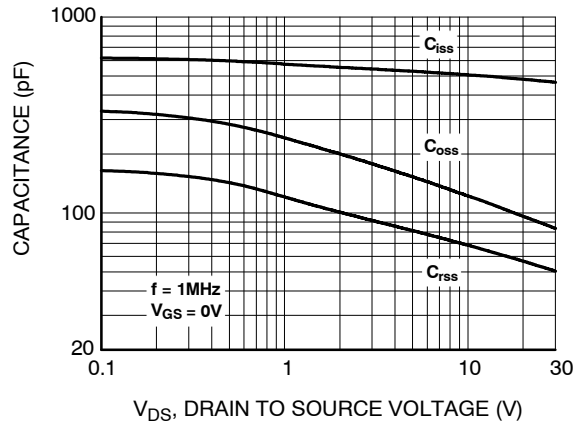


Figure 8. Capacitance vs Drain to Source Voltage

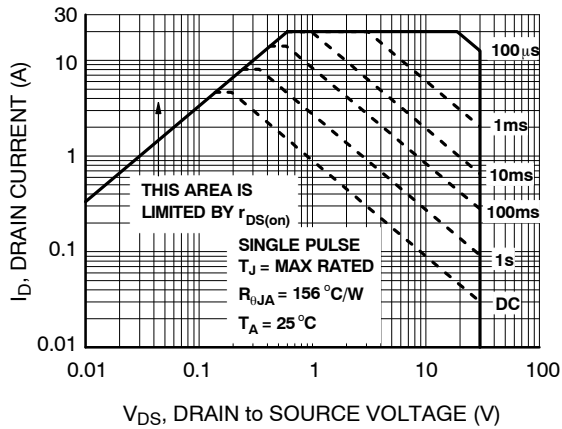


Figure 9. Forward Bias Safe Operating Area

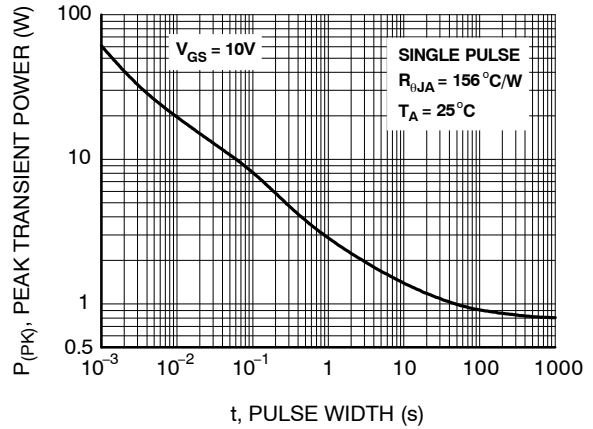


Figure 10. Single Pulse Maximum Power Dissipation

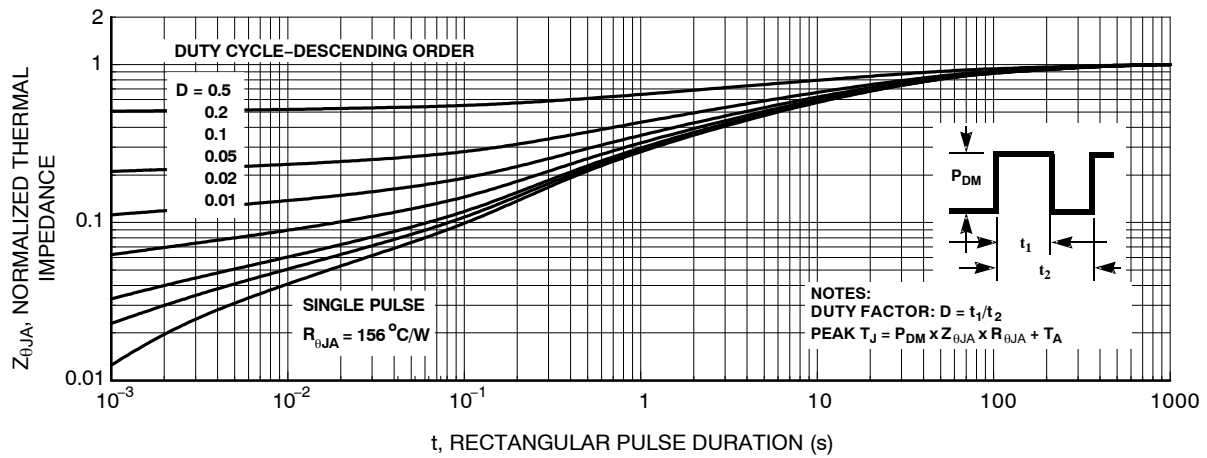


Figure 11. Transient Thermal Response Curve

FDC855N

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDC855N	.855	TSOT-23-6 (Pb-free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

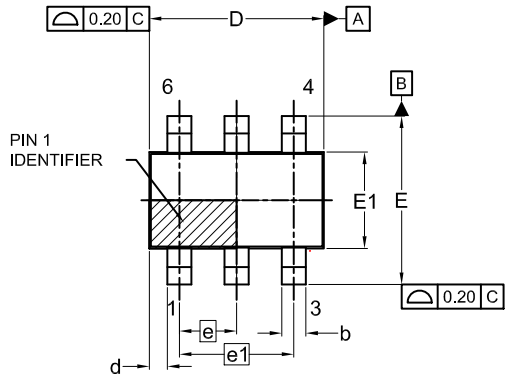
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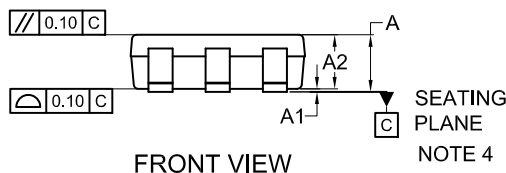
SCALE 2:1

TSOT23 6-Lead
CASE 419BL
ISSUE A

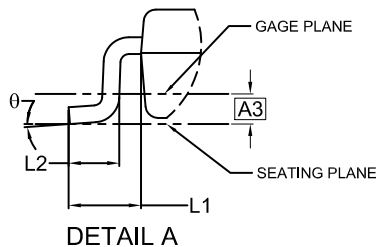
DATE 31 AUG 2020



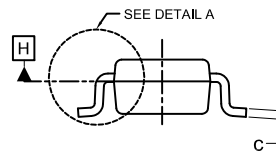
TOP VIEW



FRONT VIEW

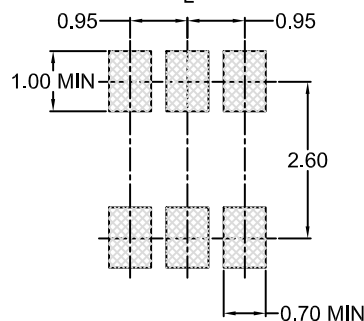


DETAIL A



SIDE VIEW

SYMM

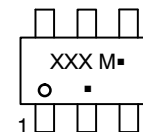

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS.
"A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
Θ	0°	—	10°

GENERIC
MARKING DIAGRAM*


XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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