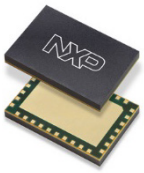
# A5M36SG239

## Airfast Power Amplifier Module with Autobias Control

**Rev. 0 — 10 October 2023** **Product data sheet**



## 1 General description

The A5M36SG239 is a fully integrated Doherty power amplifier module designed for wireless infrastructure applications that demand high performance in the smallest footprint. Ideal for applications in massive MIMO systems, outdoor small cells and low power remote radio heads. The field-proven LDMOS and GaN power amplifiers are designed for TDD LTE and 5G systems. The module includes an autobias feature that automatically sets the transistor bias upon power up and an integrated sensor that monitors the temperature. Communications to the module can be accomplished via either $I^2C$ or SPI.

## 2 Features and benefits

- 2-stage module solution that includes an LDMOS integrated circuit as a driver and a GaN final stage amplifier
- Advanced high performance in-package Doherty
- Fully matched (50 ohm input/output, DC blocked)
- Designed for low complexity digital linearization systems
- Reduced memory effects for improved linearized error vector magnitude
- Autobias on power up
- Temperature sensing
- Digital interface ($I^2C$ or SPI)
- Embedded registers and DACs for setting bias conditions
- Tx enable control pin for TDD operation

## 3 Typical LTE performance

**Table 1. Typical LTE Performance**

| Carrier Center Frequency | Gain (dB) | ACPR (dBc) | PAE (%) |
|---|---|---|---|
| **Typical LTE Performance** — 3400–3800 MHz ($P_{out}$ = 8 W Avg., $V_{DC1}$ = $V_{DP1}$ = 5 Vdc, $V_{DC2}$ = $V_{DP2}$ = 48 Vdc, 1 × 20 MHz LTE, Input Signal PAR = 8 dB @ 0.01% Probability on CCDF.)[1] | | | |
| 3410 MHz | 31.4 | –27.4 | 44.1 |
| 3500 MHz | 31.4 | –26.6 | 44.4 |
| 3600 MHz | 31.7 | –26.2 | 46.3 |
| 3700 MHz | 31.6 | –26.9 | 48.0 |
| 3790 MHz | 31.0 | –27.2 | 47.3 |

[1] All data measured with device soldered to NXP reference circuit.

# 4 Functional block diagram

## 4.1 Functional block diagram

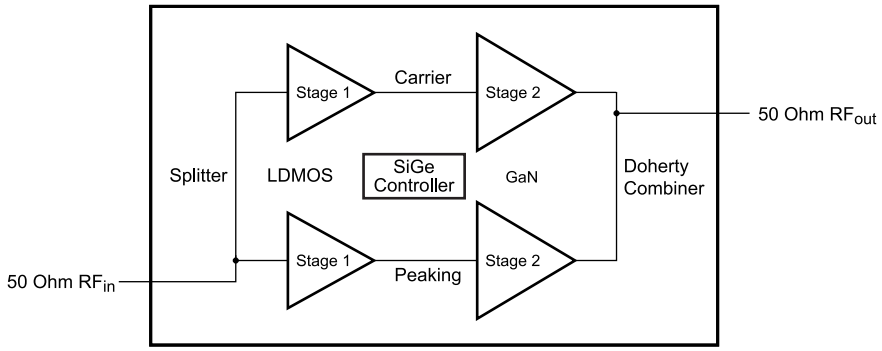



**Figure 1. Functional block diagram**

# 5 Pinning information

## 5.1 Pinning

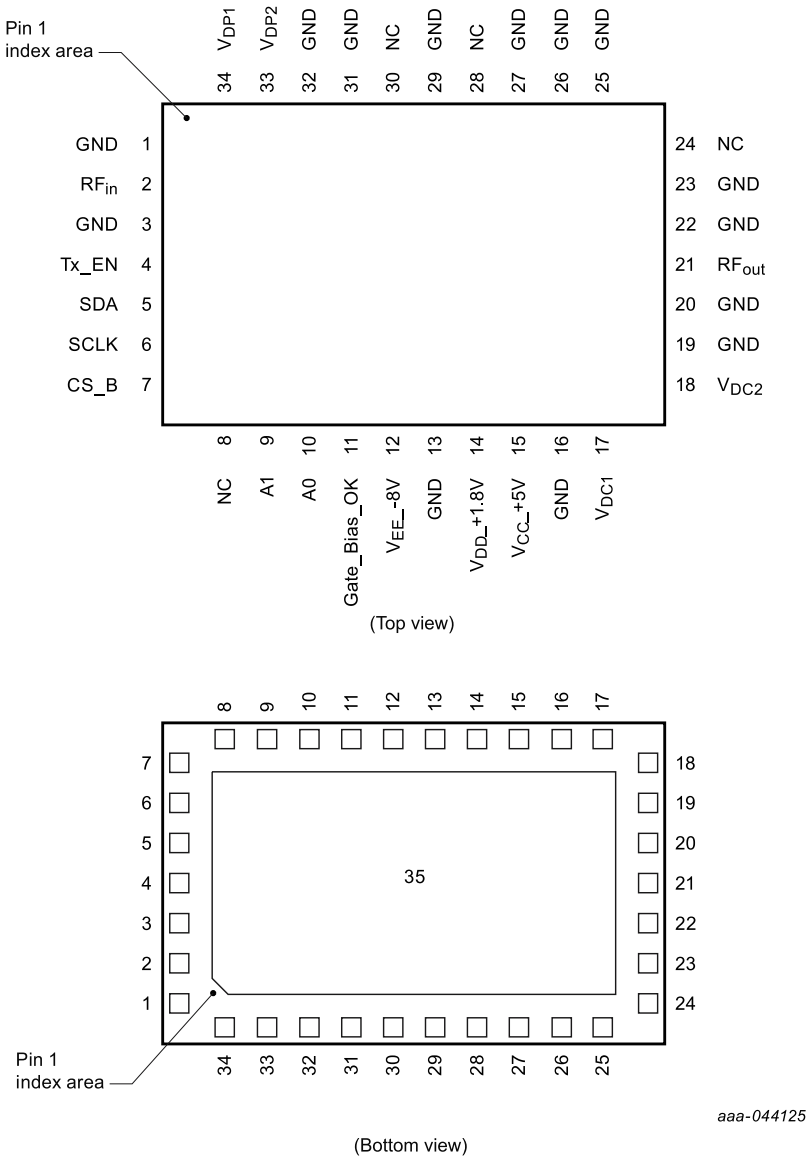



**Figure 2. Pin configuration**

## 5.2 Pin description

**Table 2. Pin description**

| Pin Number | Pin Function | Pin Description |
|---|---|---|
| 1, 3, 13, 16, 19, 20, 22, 23, 25, 26, 27, 29, 31, 32, 35 | GND | Ground |
| 2 | $RF_{in}$ | RF Input Signal @ 50 Ohms |
| 4 | Tx_EN | PA Enable Signal (1.8 V JEDEC compatible) |
| 5 | SDA | SPI/$I^2C$ Serial Data Signal (1.8 V JEDEC compatible) |
| 6 | SCLK | SPI/$I^2C$ Serial Clock Signal (1.8 V JEDEC compatible) |
| 7 | CS_B | Chip Selection Bar. Can be tied to GND when strictly following $I^2C$ protocol. |
| 8, 24, 28, 30 | NC | No Connection |
| 9 | A1 | $I^2C$ Address A1 (tri-state, tie to 1.8 V, tie to ground or leave floating) |
| 10 | A0 | $I^2C$ Address A0 (tri-state, tie to 1.8 V, tie to ground or leave floating) |
| 11 | Gate_Bias_OK | Gate Bias OK (1.8 V JEDEC compatible)<br>(Indicates gate voltage is present and drain voltage can now be applied.) |
| 12 | $V_{EE}$_–8V | Maximum –8 V Power Source for Autobias Controller |
| 14 | $V_{DD}$_+1.8V | 1.8 V Power Source for Autobias Controller<br>(No connection needed externally. The module generates 1.8 V internally for autobias controller.) |
| 15 | $V_{CC}$_+5V | 5 V $V_{CC}$ Power Source for Autobias Controller |
| 17 | $V_{DC1}$ | Carrier LDMOS Driver Drain Supply, Stage 1 |
| 18 | $V_{DC2}$ | Carrier GaN Drain Supply, Stage 2 |
| 21 | $RF_{out}$ | RF Output Signal @ 50 Ohms |
| 33 | $V_{DP2}$ | Peaking GaN Drain Supply, Stage 2 |
| 34 | $V_{DP1}$ | Peaking LDMOS Driver Drain Supply, Stage 1 |

# 6 Electrical characteristics

## 6.1 Ratings

### 6.1.1 Limiting values

**Table 3. Limiting values**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Gate-Bias Voltage Range | $V_{CC\_}$ +5V<br>$V_{EE\_}$ –8V | 4.75 to 5.25<br>–8.4, –7.6 | Vdc |
| 5 $V_{CC}$ Slew Rate, $T_C$ = 25°C | $V_{CC\_}$+5V_SLEW | < 9.5 | ms |
| Operating Voltage Range | $V_{DC1}$, $V_{DP1}$<br>$V_{DC2}$, $V_{DP2}$ | 4.75 to 5.25<br>+38 to +55 | Vdc |
| Operating Voltage Range | CS_B, SDA, SCLK, Tx_EN, A1, A0 | 1.65 to 1.95 | Vdc |
| Storage Temperature Range | $T_{stg}$ | –65 to +150 | °C |
| Case Operating Temperature | $T_C$ | 125 | °C |
| Peak Input Power<br>(3600 MHz, Pulsed CW, 10 µsec(on), 10% Duty Cycle) | $P_{in}$ | 28 | dBm |

### 6.1.2 Lifetime

**Table 4. Lifetime**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Mean Time to Failure<br>(Case Temperature 125°C, Internal Sense Temperature 101°C, 8 W Avg., $V_{DC1}$ = $V_{DP1}$ = 5 Vdc, $V_{DC2}$ = $V_{DP2}$ = 48 Vdc)[1] | MTTF | 10 | Years |

[1] All data measured with device soldered to NXP reference circuit.

### 6.1.3 Thermal characteristics

**Table 5. Thermal characteristics**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance by Infrared Measurement, Active Die Surface-to-Case<br>(Case Temperature 125°C, $P_D$ = 12.6 W) | $R_{\theta JC}$ (IR) | 4.2[1] | °C/W |
| Thermal Resistance by Finite Element Analysis, Channel-to-Case<br>(Case Temperature 125°C, $P_D$ = 10.1 W) | $R_{\theta CHC}$ (FEA) | 9.9[2] | °C/W |

[1] Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to http://www.nxp.com/RF and search for AN1955.

[2] $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression MTTF (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, A = –12.5 and B = 9729.

### 6.1.4 ESD protection characteristics

**Table 6. Lifetime ESD protection characteristics**

| Test Methodology | Class |
|---|---|
| Human Body Model (per JS-001-2017) | 2 |
| Charge Device Model (per JS-002-2014) | C3 |

### 6.1.5 Moisture sensitivity level

**Table 7. Moisture sensitivity level**

| Test Methodology | Rating | Package Peak Temperature | Unit |
|---|---|---|---|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

## 6.2 Operating characteristics

### 6.2.1 Typical $I_{DQ}$ currents

**Table 8. Typical $I_{DQ}$ currents** ($T_A$ = 25°C unless otherwise noted)[1]

| Characteristic | Symbol | Typ | Unit |
|---|---|---|---|
| LDMOS_VGC1_DAC Gate Quiescent ($V_{DC1}$ = 5 Vdc, LDMOS_SENSE_DAC = 32) | $I_{DQC1}$ | 63 | mA |
| LDMOS_VGP1_DAC Gate Quiescent ($V_{DP1}$ = 5 Vdc, LDMOS_SENSE_DAC = 32) | $I_{DQP1}$ | 43 | mA |
| GaN_VGC2_DAC Gate Quiescent ($V_{DC2}$ = 48 Vdc, GaN_SENSE_DAC = 18) | $I_{DQC2}$ | 60 | mA |
| GaN_VGP2_DAC Gate Quiescent[2] ($V_{DP2}$ = 48 Vdc, GaN_SENSE_DAC = 18) | $I_{DQP2}$ | 0 | mA |

[1] One-time programmable registers are set at final test to meet typical $I_{DQ}$ values for each stage on power up. DACs are programmable in Engineering Mode. Each stage of device is measured separately.

[2] Set GaN_VGP2_DAC until $I_{DQP2}$ = 40 mA current is attained, and then subtract 23 DAC steps.

### 6.2.2 Functional tests

**Table 9. Functional tests**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Functional Tests** — 3400 MHz (In NXP Doherty Production ATE[1] Test Fixture, $T_A$ = 25°C unless otherwise noted, 50 ohm system)[2] $V_{DC1}$ = $V_{DP1}$ = 5 Vdc, $V_{DC2}$ = $V_{DP2}$ = 48 Vdc, Nominal DAC Settings[3], Tx_EN = High, $P_{out}$ = 8 W Avg., 1-tone CW, f = 3400 MHz | | | | | |
| Gain | G | 29.0 | 31.5 | — | dB |
| Drain Efficiency | $\eta_D$ | 39.0 | 44.6 | — | % |
| Saturated Power[4] (Pulsed CW, 5% Duty Cycle) | $P_{sat}$ | 46.6 | 48.0 | — | dBm |
| **Functional Tests** — 3800 MHz (In NXP Doherty Production ATE[1] Test Fixture, $T_A$ = 25°C unless otherwise noted, 50 ohm system)[2] $V_{DC1}$ = $V_{DP1}$ = 5 Vdc, $V_{DC2}$ = $V_{DP2}$ = 48 Vdc, Nominal DAC Settings[3], Tx_EN = High, $P_{out}$ = 8 W Avg., 1-tone CW, f = 3800 MHz | | | | | |
| Gain | G | 29.5 | 31.7 | — | dB |
| Drain Efficiency | $\eta_D$ | 40.0 | 47.6 | — | % |
| Saturated Power[4] (Pulsed CW, 5% Duty Cycle) | $P_{sat}$ | 46.7 | 48.2 | — | dBm |

[1] ATE is a socketed test environment.
[2] Part input and output matched to 50 ohms.
[3] Nominal DAC setting is burnt during the OTP process to match the $I_{DQ}$ values in Table 8, Typical $I_{DQ}$ currents.
[4] $P_{sat}$ is defined at P3dB compression point.

### 6.2.3 Wideband ruggedness

**Table 10. Wideband ruggedness**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Wideband Ruggedness** (In NXP Doherty Power Amplifier Module Reference Circuit, $T_A$ = 25°C unless otherwise noted, 50 ohm system)[1] Nominal DAC Settings, Tx_EN = High, f = 3600 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR | | | | | |
| ISBW of 400 MHz at 55 Vdc, 3 dB Input Overdrive from 8 W Avg. Modulated Output Power | No Device Degradation | | | | |

[1] All data measured with device soldered to NXP reference circuit.

### 6.2.4 Typical performance

**Table 11. Typical performance**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Typical Performance** (In NXP Doherty Power Amplifier Module Reference Circuit, $T_A$ = 25°C unless otherwise noted, 50 ohm system)[1] $V_{DC1}$ = $V_{DP1}$ = 5 Vdc, $V_{DC2}$ = $V_{DP2}$ = 48 Vdc, Nominal DAC Settings, Tx_EN = High, f = 3600 MHz | | | | | |
| VBW Resonance Point, 2-tone, 1 MHz Tone Spacing (IMD Third Order Intermodulation Inflection Point) | $VBW_{res}$ | — | > 500 | — | MHz |
| **1-carrier 20 MHz LTE, 8 dB Input Signal PAR** | | | | | |
| Gain | G | — | 31.7 | — | dB |
| Power Added Efficiency | PAE | — | 46.3 | — | % |
| Adjacent Channel Power Ratio | ACPR | — | –26.2 | — | dBc |
| Adjacent Channel Power Ratio | ALT1 | — | –45.2 | — | dBc |
| Adjacent Channel Power Ratio | ALT2 | — | –49.3 | — | dBc |
| Gain Flatness[2] | $G_F$ | — | 0.8 | — | dB |
| **Pulsed CW, 10% Duty Cycle** | | | | | |
| Saturated Power[3] | $P_{sat}$ | — | 48.1 | — | dBm |
| AM/PM @ Saturated Power[3] | Φ | — | –38 | — | ° |
| Gain Variation @ Avg. Power over Temperature (–40°C to +105°C) | ΔG | — | 0.037 | — | dB/°C |
| Output Power Variation @ Saturated Power over Temperature[3] (–40°C to +105°C) | $\Delta P_{sat}$ | — | 0.002 | — | dB/°C |

[1] All data measured with device soldered to NXP reference circuit.
[2] Gain flatness = Max(G($f_{Low}$ to $f_{High}$)) – Min(G($f_{Low}$ to $f_{High}$))
[3] $P_{sat}$ is defined at P3dB compression point.

# 7 Register map and OTP memory

## 7.1 One-time programmable memory

The A5M36SG239 contains a one-time programmable (OTP) memory array that is used to store and recall register values for the integrated autobias controller at power up or reset. The data sheet $I_{DQ}$ target values from Table 8 are programmed into the OTP memory during NXP's production testing. These values can be overwritten using the Engineering Mode (EM) sequence; however, the overwritten values do not persist after a power cycle or a reset.

The OTP memory can be programmed only by NXP during the manufacturing process and cannot be changed by the user. The values in OTP memory have been selected to allow the device to operate in a wide variety of applications.

## 7.2 Register map

There are nine 8-bit user accessible registers available in the A5M36SG239. The register mapping is listed in Table 12. Address 0 RW register is designed to control soft reset, refresh OTP and read the chip version. Address 1−6 registers are RW and/or OTP controlled and provide settings for the two RF transistor group DACs. Address 15 is read only for temperature sense functionality. Address 17 is a virtual write only register for enabling Engineering Mode.

**Table 12. Register map**

| Address (in Decimal) | Register Attribute | Register Name | Register Definition | | | | | | | | Default Value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |
| 0 | RW | System_Reg | N/A | Soft Reset | Refresh OTP | N/A | Chip Version [3:0] (Read only) | | | | 8'b0000_0001 |
| 1 | OTP COPY (RW) | LDMOS_Sense_DAC | Reserved | | LDMOS Sense DAC | | | | | | OTP value |
| 2 | OTP COPY (RW) | LDMOS_VGC1_DAC | LDMOS $V_{GC1}$ DAC | | | | | | | | OTP value |
| 3 | OTP COPY (RW) | LDMOS_VGP1_DAC | LDMOS $V_{GP1}$ DAC | | | | | | | | OTP value |
| 4 | OTP COPY (RW) | GaN_Sense_DAC | Reserved | | GaN Sense DAC | | | | | | OTP value |
| 5 | OTP COPY (RW) | GaN_VGC2_DAC | GaN $V_{GC2}$ DAC | | | | | | | | OTP value |
| 6 | OTP COPY (RW) | GaN_VGP2_DAC | GaN $V_{GP2}$ DAC | | | | | | | | OTP value |
| 7 | RO | Device_ID | Final GaN stage nominal drain voltage = 48 V [7:2] | | | | | | Device version [1:0] | | 8'b11000000 |
| 8–14 | — | — | Reserved | | | | | | | | — |
| 15 | RO | Temp_ADC | Temperature Sensor [7:0] | | | | | | | | — |
| 16 | — | — | Reserved | | | | | | | | — |
| 17 | Virtual W only | EM_Passcode | Engineering Mode (EM) passcode 8'hE3 | | | | | | | | — |

Read Only register (RO)
Read Write register (RW)
Read Write register with OTP overwrite at Startup (RW)
Reserved non-accessible register
Write Only register

**Table 13. Register overview and bit description**

| Address | Register Name | Bit | Bit Descriptions | Power On/Reset Value[1] | Overwritten by OTP | Attribute | EM Mode |
|---|---|---|---|---|---|---|---|
| 0 | System_Reg | 7 | Not available | N/A | N/A | N/A | N/A |
| | | 6 | Soft Reset. A 1 written to this register will perform a reset of all registers to their default values. A 0 should be written after the reset operation is completed. | 0 | No | RW | |
| | | 5 | Refresh OTP. A 1 written to this register will overwrite current DAC values with those stored in OTP into registers identified in the "Overwritten by OTP" column. A 0 should be written after the reset operation is completed. | 0 | No | | |
| | | 4 | Not available | N/A | N/A | N/A | |
| | | 0–3 | Chip version bits. Inserted by NXP to provide revision information. Cannot be changed. | N/A | No | R | |
| 1 | LDMOS_Sense_DAC | 6–7 | Not available | N/A | N/A | N/A | |
| | | 0–5 | LDMOS_Sense_DAC 6-bit logic value for LDMOS driver stage amplifiers. LDMOS_Sense_DAC sets the reference voltage to compare to the $V_{DS}$ across the reference device. Optimal value set by NXP. Adjustment by end user to the optimal setting is not recommended. | 8'h20 | Yes | RW[2] | Yes |
| 2 | LDMOS_VGC1_DAC | 0–7 | Sets 8-bit DAC logic value for carrier amplifier driver stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value. | 8'h80 | | | |
| 3 | LDMOS_VGP1_DAC | 0–7 | Sets 8-bit DAC logic value for peaking amplifier driver stage. 8'h00 sets gate to equal ceiling voltage. 8'hFF reduces gate voltage by a max value. | 8'h80 | | | |

(continued)

**Table 13. Register overview and bit description** (continued)

| Address | Register Name | Bit | Bit Descriptions | Power On/Reset Value[1] | Overwritten by OTP | Attribute | EM Mode |
|---|---|---|---|---|---|---|---|
| 4 | GaN_Sense_DAC | 6–7 | Not available | N/A | N/A | N/A | No |
| | | 0–5 | GaN_Sense_DAC 6-bit logic value for GaN final stage amplifiers. GaN_Sense_DAC sets the reference voltage to compare to the $V_{DS}$ across the reference device. Optimal value set by NXP. Adjustment by end user to the optimal setting is not recommended. | 8'h20 | Yes | RW[2] | Yes |
| 5 | GaN_VGC2_DAC | 0–7 | Sets 8-bit DAC logic value for carrier final stage. 8'hFF sets gate to equal ceiling voltage. 8'h00 reduces gate voltage by a max value. | 8'h80 | | | |
| 6 | GaN_VGP2_DAC | 0–7 | Sets 8-bit DAC logic value for peaking final stage. 8'hFF sets gate to equal ceiling voltage. 8'h00 reduces gate voltage by a max value. | 8'h80 | | | |
| 7 | Device ID | 7–2 | Final stage GaN nominal drain voltage for both carrier and peaking sides = 48 V. | | N/A | R | No |
| | | 0–1 | Device version ID | | N/A | R | No |
| 8–14 | Reserved | N/A | Not available | N/A | N/A | N/A | No |
| 15 | Temp_ADC | 0–7 | Temperature sensor 8-bit DAC value. 8'h00 is lowest temperature, 8'hFF is highest temperature. | 8'h00 | No | R | No |
| 16 | Reserved | N/A | Not available | N/A | N/A | N/A | No |
| 17 | EM_Passcode | 0–7 | Engineering Mode (EM). By writing 8'hE3 to this register the user can enter engineering mode. EM can be cleared by writing any other code to this register. In EM registers identified in EM mode column can be changed. | N/A | No | W | Yes |

[1] At power on or reset, OTP values set by NXP are automatically loaded into registers indicated with a “Yes” in the “Overwritten by OTP” column. For these registers, values shown in the “Power On/Reset Value” column will be loaded only if OTP has not been programmed to prevent damage to the device.

[2] Register can be read at any time. Can write to register only when in Engineering Mode (EM).

# 8 Power supply sequence

Power Up Sequence

1. $V_{EE}$_–8V: –8 V power up
2. $V_{CC}$_+5V: 5 V, $V_{DP1}$, $V_{DC1}$: 5 V power up. Note: $V_{CC}$_+5V needs to reach steady state within 9.5 ms.
3. Gate_Bias_OK should return 1.8 V as this indicates SPI/$I^2C$ interface is active.
4. $V_{DP2}$, $V_{DC2}$: 48 V power up
5. Tx_EN: 1.8 V power up
6. DUT is now biased and ready for RF measurements.

Power Down Sequence

1. Tx_EN: 1.8 V power down
2. $V_{DP2}$, $V_{DC2}$: 48 V power down
3. $V_{DP1}$, $V_{DC1}$: 5 V, $V_{CC}$_+5V: 5 V power down
4. SPI/$I^2C$ interface deactivated
5. $V_{EE}$_–8V: –8 V power down

Note: All digital interfaces (SDA, SCLK, CS_B, Tx_EN, A0, A1) are 1.8 V logic.

# 9 Autobias functionality

## 9.1 General overview

After power up, the integrated bias controller develops and applies a quiescent bias voltage to the gate of each of the RF transistors contained within the power amplifier module (PAM) based on the preset OTP values. The standard SPI or $I^2C$ interface can be used to read the temperature sensor and overwrite preset DAC values. The device can be used without the programming interface at initial power up; however, additional compensation for the GaN FETs over temperature is recommended to achieve optimal performance. The thermal compensation circuit is analog and not programmable; however, the preset DAC values for the four $V_{GS}$ DACs can be overwritten to provide an additional thermal compensation scheme via the SPI or $I^2C$ interface. This section describes the operation and programming of the bias controller.

## 9.2 Operational overview

### 9.2.1 LDMOS driver stage autobias operation

Figure 3 shows a detailed view of the driver stage autobias controller. The driver stage on both the carrier side and peaking side is an RF LDMOS field-effect transistor (FET). Each die for the carrier and peaking driver stage also contains a small periphery reference FET that is designed to match the properties of the larger RF transistors with regard to part-to-part process and temperature-dependent variations. The bias controller interfaces with each of the RF FETs and provides flexibility to control the biasing of the driver stage transistor groups independently.

The bias controller operates by establishing a known current through each reference FET. This in turn establishes a gate-source operating voltage by sensing the voltage drop across an integrated, high tolerance resistor placed between $V_{CC}$ (5 V) and the reference device drain terminal. The bias controller $V_{CC}$_+5V pin should be operated from a 5 V supply with a tolerance of ±5%. The reference voltage across the precision resistor R1 is compared to a voltage programmed in the bias controller (LDMOS_Sense_DAC), thereby providing fine incremental adjustment to the default bias current of the reference FET. Because the reference FET and RF FET are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies.

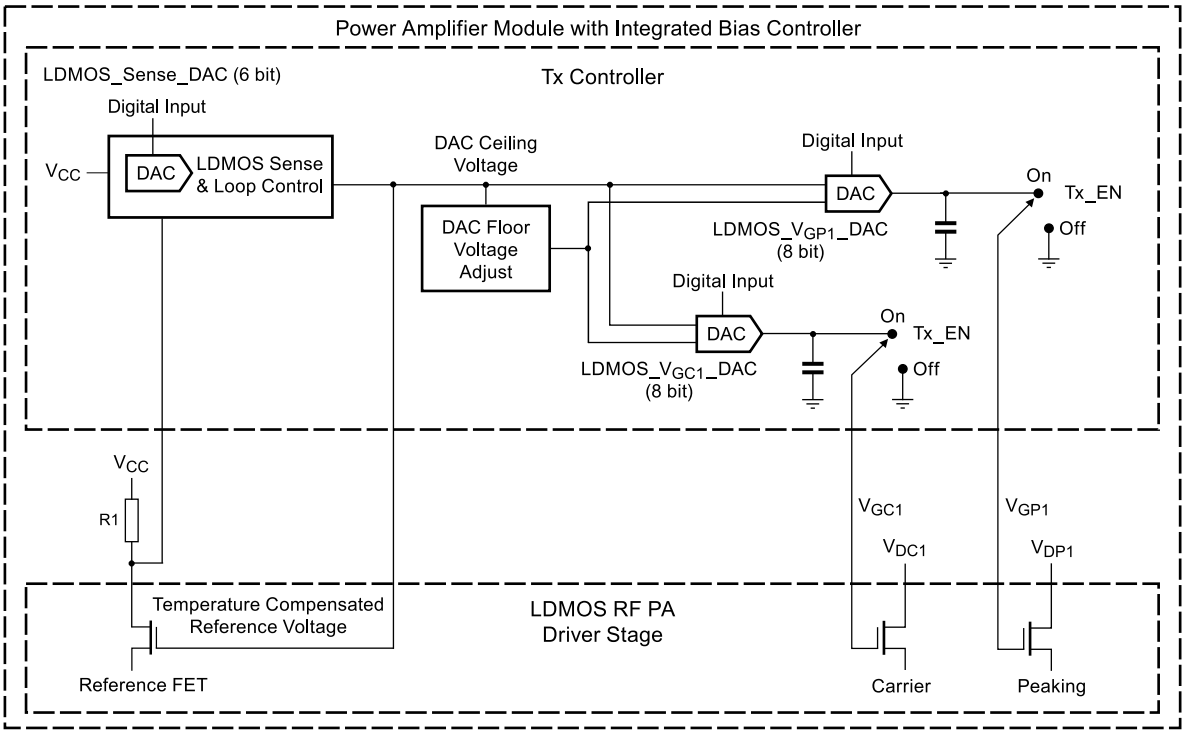



**Figure 3. Block diagram of LDMOS driver autobias functionality**

The initial bias condition is set via the LDMOS_Sense_DAC register. The bias condition is then sensed and adjusted as temperature changes via the closed-loop feedback. The feedback mechanism adjusts the DAC ceiling voltage to maintain a constant $I_{DS}$ current through the reference FET. The temperature compensated DAC ceiling voltage can either be passed to the carrier PA driver and peaking PA driver directly, or reduced by values set in the LDMOS_VGC1_DAC and LDMOS_VGP1_DAC to the DAC floor voltage.

### 9.2.2 GaN final stage autobias operation

Figure 4 shows a detailed view of the final stage autobias controller. The final stage on both the carrier side and the peaking side are RF GaN FETs. Each die for the carrier and peaking final stage also contains a small periphery reference FET that is designed to match the properties of the larger RF transistors with regard to part-to-part process and temperature-dependent variations. The bias controller interfaces with each of the RF FETs and provides flexibility to control the biasing of the final stage transistors independently.

The bias controller operates by establishing a known current through the reference FET. This in turn establishes a gate-source operating voltage by sensing the voltage drop across an integrated, high tolerance resistor on the reference device drain terminal. The bias controller $V_{CC}$_+5V pin should be operated from a 5 V supply with tolerance of ±5%. The bias controller $V_{EE}$_–8V pin should be operated from a –8 V supply with tolerance of ±5%. The reference voltage across the precision resistor R1 is compared to a voltage programmed in the bias controller (GaN_Sense_DAC), thereby providing fine incremental adjustment to the default bias current of the reference FET. Because the reference FET and RF FET are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies. Additional compensation is recommended for the GaN FETs over temperature to achieve optimal performance.

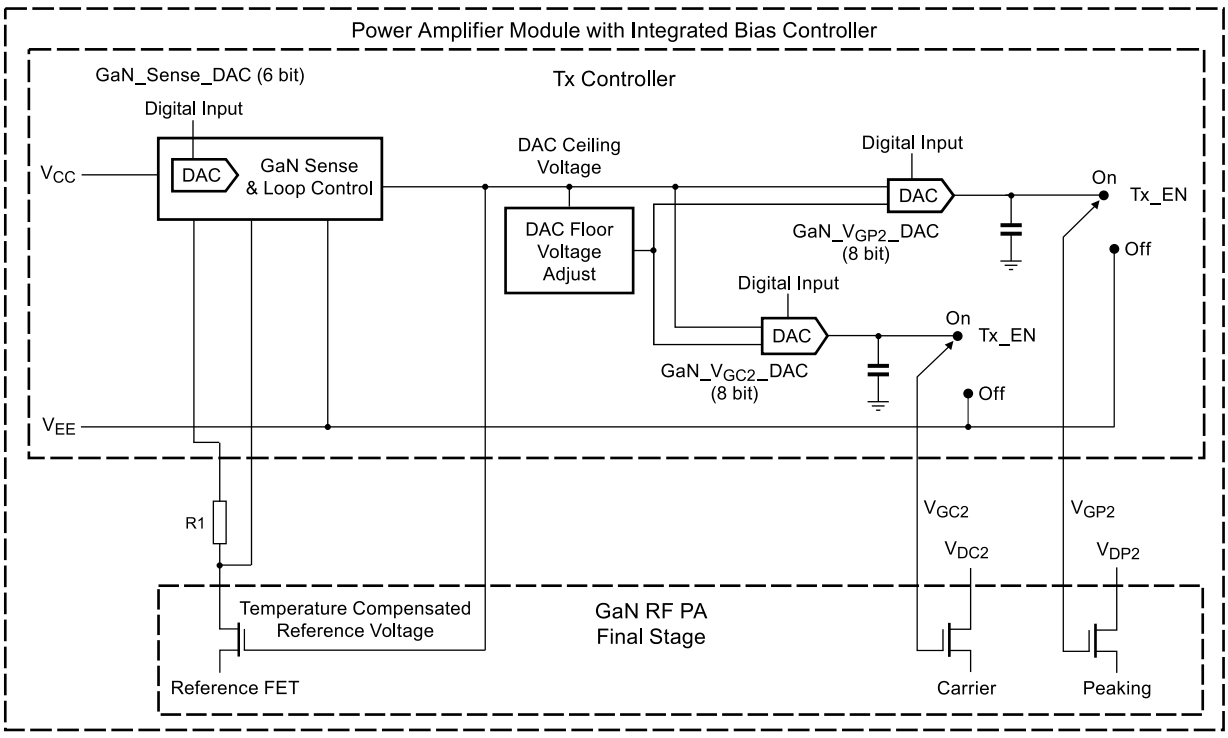



**Figure 4. Block diagram of GaN final stage autobias functionality**

## 9.3 Tx enable control

A 1.8 V JEDEC compliant enable signal (Tx_EN) is included for bias control to support TDD operation. The controller provides capability to quickly switch the RF FETs between ON and OFF modes in less than 100 ns. With Tx_EN in an ON state, the RF FET gate terminals are internally decoupled with sufficient capacitance providing a low impedance for wide baseband signals. The large capacitance also serves as a charge holding cap for reducing switching transient time in TDD operation. In Tx OFF mode, LDMOS RF FET device gates are grounded and GaN RF FETs are tied to –8 V, effectively shutting them OFF.

**Table 14. TX_EN off-state typical currents**

| Characteristic | Typical Value | Unit |
|---|---|---|
| $V_{CC}$_+5V Supply Current | 35–38 | mA |
| $V_{EE}$_–8V Supply Current (with $V_{CC}$_+5V Supply ON) | 9–11 | mA |

## 9.4 Sense_DAC

The current in the reference FET is controlled and programmed with 6 bits (two MSBs of the 8-bit register are not used) via the sense DAC (LDMOS_Sense_DAC and GaN_Sense_DAC). By programming the sense DAC, the RF stage DAC ceiling voltage reference operating point can be optimally set. The DAC ceiling voltage reference point impacts both RF PA stages simultaneously for each group. After OTP has been programmed, the Sense_DAC is loaded with the programmed values and should not be adjusted in Engineering Mode.

The factory programmed values for LDMOS_Sense_DAC and GaN_Sense_DAC are decimal 32 and 18 respectively. These values have been optimized for best power, linearity and efficiency tradeoffs.

## 9.5 VGS_DAC

The VGS_DAC voltage is determined via the Sense_DAC setting, creating the top end or ceiling of the VGS_DAC voltage range and a fixed offset voltage creating the bottom end or floor of the VGS_DAC voltage range. With a decimal VGS_DAC setting of 0, the gate voltage developed on the reference FET is buffered with minimum offset to the gates of the RF transistors in the carrier amplifier. As the LDMOS VGS_DAC value increases, the voltage applied to the gates of the driver stage RF transistors decreases, which reduces $I_{DQ}$. As the GaN VGS_DAC value increases, the voltage applied to the gates of the final stage RF transistors increases, which increases $I_{DQ}$. This allows the operating point of the four RF devices to be set to any desired value, from Class AB to Class C.

The reference FETs and RF FETs exhibit approximately the same current density (that is, $I_{DQ}$/mm gate width). It is important to note that, because the reference device and RF transistors are manufactured on the same die in close proximity, they exhibit similar process and temperature dependencies. Both the driver amplifiers and the final amplifiers operate in the same way with regard to the reference device and the RF transistors.

## 9.6 Engineering Mode (EM)

Flexibility exists to overwrite the OTP memory values. A special Engineering Mode (EM) is available to allow the user to overwrite data that has been placed into the OTP memory space. To enter EM, issue the write address d'17 command with the predefined EM passcode (see Table 12). After entering EM, all DAC OTP registers (address 1–6) can be overwritten with the normal $I^2C$/SPI write instruction. This interface programmed value will be valid so long as the $V_{CC}$ supply power is maintained. The $V_{CC}$ power cycle will load OTP programmed DAC settings again. If the user writes the address d'17 register with any value other than the passcode, EM will automatically exit.

# 10 Ordering information

**Table 15. Ordering information**

| Device | Tape and Reel Information | Package |
|---|---|---|
| A5M36SG239T2 | T2 Suffix = 2000 Units, 24 mm Tape Width, 13-inch Reel | 12 mm × 8 mm Module |

# 11 Product marking

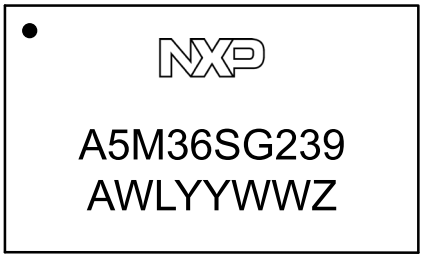


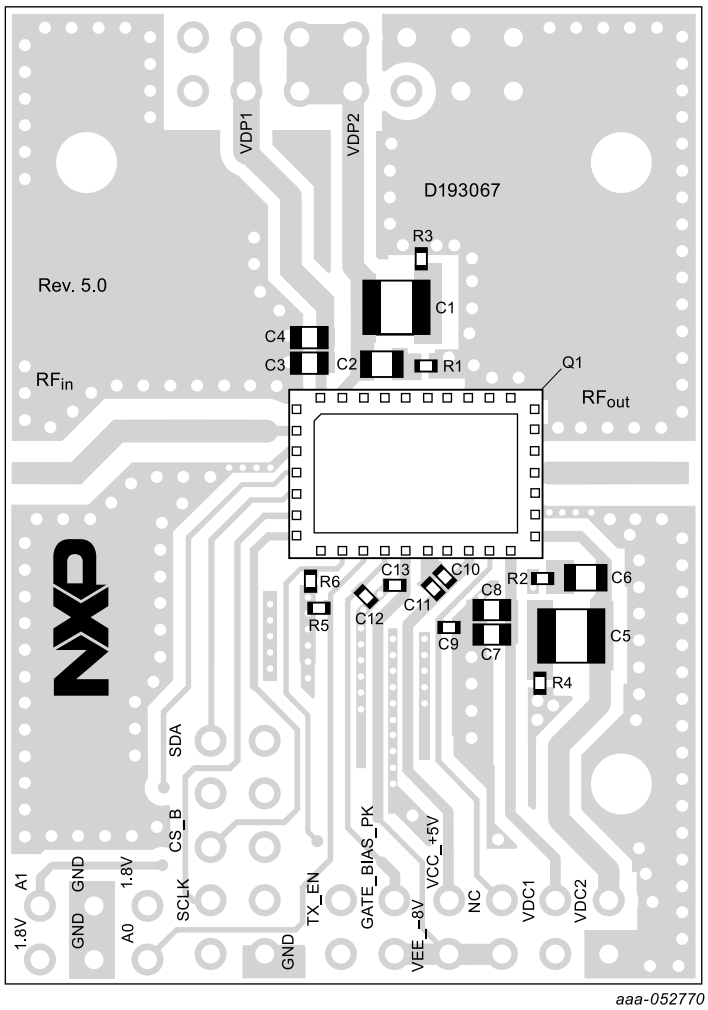

**Figure 5. Product marking**

**Table 16. Product marking trace code**

| Identifier | Description |
|---|---|
| A | Assembly location |
| WL | Wafer lot indicator |
| YYWW | Date code |
| Z | Assembly lot |

# 12 Component layout and parts list

## 12.1 Component layout




aaa-052770

**Figure 6. A5M36SG239 reference circuit component layout**

## 12.2 Component designations and values

**Table 17. A5M36SG239 reference circuit component designations and values**

| Part | Description | Part Number | Manufacturer |
|---|---|---|---|
| C1, C5 | 10 μF Chip Capacitor | GRM32EC72A106KE05L | Murata |
| C2, C6 | 1 μF Chip Capacitor | GRM21BC72A105KE01 | Murata |
| C3, C7, C9, C12 | Do not place | — | — |
| C4, C8 | 10 μF Chip Capacitor | GRM188D71A106MA73 | Murata |
| C10 | 0.01 μF Chip Capacitor | CGA2B3X7R1H103K050BB | TDK |
| C11, C13 | 1 μF Chip Capacitor | GRM155R61H105KE5D | Murata |
| Q1 | Power Amplifier Module | A5M36SG239 | NXP |
| R1, R2, R3, R4, R5, R6 | 0 Ω, 1/10 W Chip Resistor | ERJ2GE0R00X | Panasonic |
| PCB | Rogers RO4350B, 0.020″, $\varepsilon_r$ = 3.66 | D193067 | MTL |

# 13 Temperature sensor

The temperature value is converted from the 8-bit temperature sense ADC value (stored in the Temp_ADC register) via the following preliminary equation. Further measurement and validation of this equation may result in future changes.

$T_J$ in °C = (0.67481 × Temp_ADC) – 45.14529

A plot of this equation is shown in Figure 7.

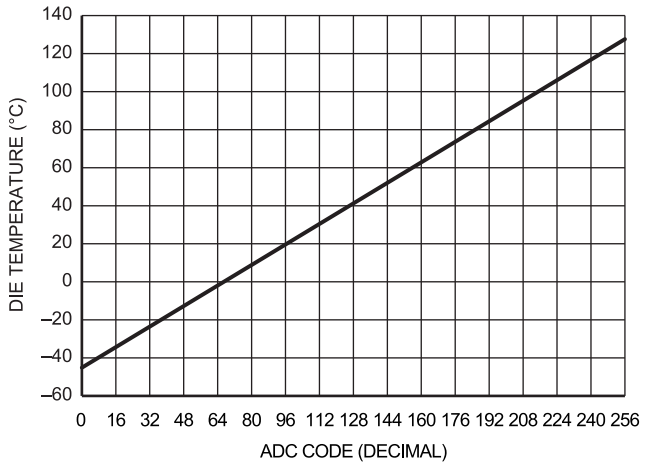



**Figure 7. Die temperature versus ADC code**

**Table 18. Temperature sensor accuracy**

| Characteristic | Value | Unit |
|---|---|---|
| Operating Die Temperature, $T_J$ = 25°C to 85°C | ±3 | °C |
| Operating Die Temperature, $T_J$ = –35°C to +125°C | ±5 | °C |

# 14 Communication interfaces

The A5M36SG239 device contains a digital interface that supports either a 3-pin SPI or 2-pin $I^2C$ interface. The digital interface is used to both read and write data to and from the device. The preferred interface type can be selected externally by adjusting the A0 and A1 pins.

## 14.1 SPI

The A5M36SG239 can be programmed and the Tx bias settings and temperature read through the 3-pin SPI interface. To enable SPI mode, pins A0 and A1 must be connected to ground (see Table 20).

### 14.1.1 SPI timing diagram

The SPI interface timing of A5M36SG239 complies with SPI mode3 as shown in Figure 8.

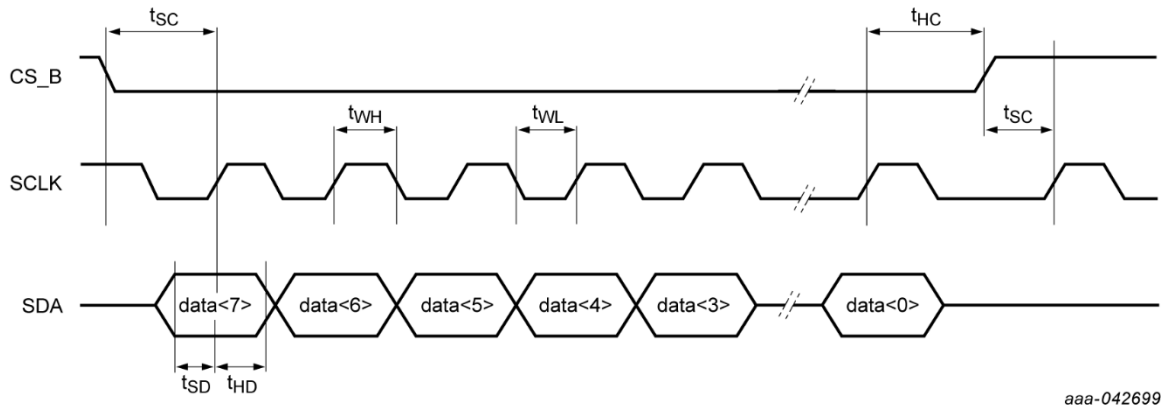



**Figure 8. Serial interface timing diagram**

**Table 19. Serial interface timing specification**

| Symbol | Parameter | Min (ns) |
|---|---|---|
| $t_{SC}$ | Setup timing requirement of CS_B (both rising and falling) in relation to the rising edge of SCLK | 50 |
| $t_{WH}$ | clk high duration | 160 |
| $t_{WL}$ | clk low duration | 160 |
| $t_{SD}$ | Date to clock rising edge setup | 20 |
| $t_{HD}$ | clk rising edge to data hold time | 20 |
| $t_{HC}$ | clk to CS_B hold time | 50 |
| $t_{WH} + t_{WL}$ | Minimum clock period | 400 |

### 14.1.2 SPI instruction set definition

The SPI instruction set is determined by the first byte after releasing the CS_B signal. The order of SPI instruction is MSB sent first, LSB sent last. Bit 7 of the SPI instruction set is defined as read (1) or write (0) command. Bits 6−5 define the burst width in the range of 1−4 bytes: 00 is for 1 byte data, 01 for 2 bytes data, 10 for 3 bytes data and 11 is for 4 bytes data. Bits 4−0 are defined as the register address that is to be accessed.

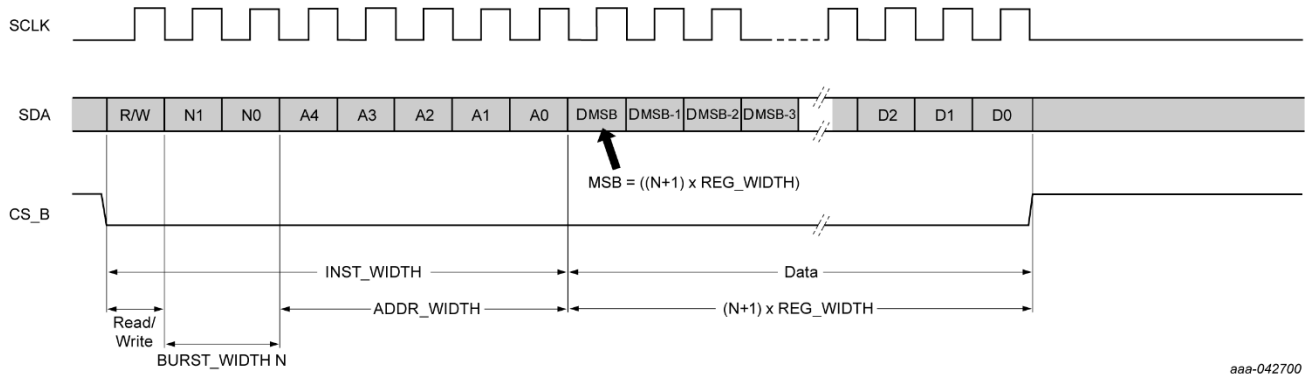



**Figure 9. SPI instruction sets diagram**

SPI instruction set information:

- R/W read = 1, write = 0
- N1, N0
  - 2'b00 1 byte
  - 2'b01 2 bytes
  - 2'b10 3 bytes
  - 2'b11 4 bytes
- A4, A3, A2, A1, A0 decode for address 0–15
- MSB sent first, LSB last

## 14.2 I²C

The A5M36SG239 follows the I²C protocol standard. It supports I²C fast mode with a bit rate up to 400 Kbit/s. It also supports I²C standard mode with bit rate up to 100 Kbit/s.

### 14.2.1 I²C addressing

The two external tri-state address pins A0 and A1 use 1.8 V logic levels and are decoded into 7-bit I²C addresses as shown in Table 20. The three LSBs of the 7-bit address are set via the A0 and A1 pins. The four MSBs are the base address, which is fixed at 1000.

**Table 20. I²C 7-bit address assignment**

| A1 | A0 | I²C 7-Bit Address |
|---|---|---|
| 0 | 0 | Disable I²C (SPI Mode) |
| 0 | Z | 1000 000 |
| 0 | 1 | 1000 001 |
| Z | 0 | 1000 010 |
| Z | Z | 1000 011 |
| Z | 1 | 1000 100 |
| 1 | 0 | 1000 101 |
| 1 | Z | 1000 110 |
| 1 | 1 | 1000 111 |

### 14.2.2 I²C instruction set

#### 14.2.2.1 I²C Write instruction

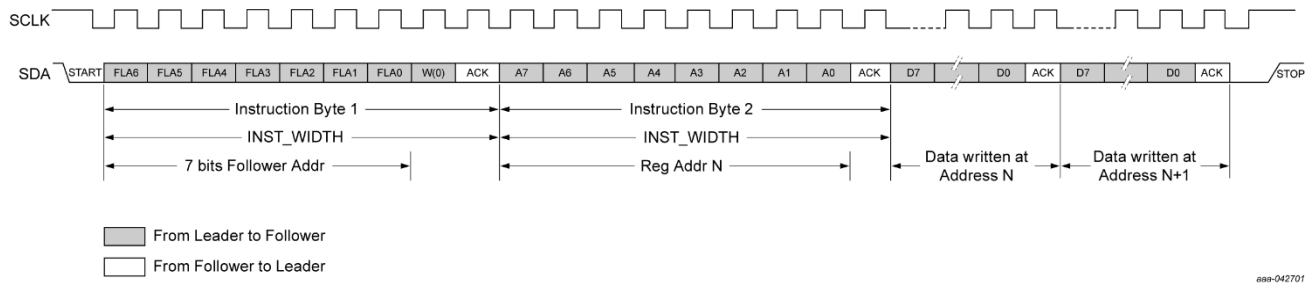



**Figure 10. I²C Write instruction**

#### 14.2.2.2 I²C Read instruction

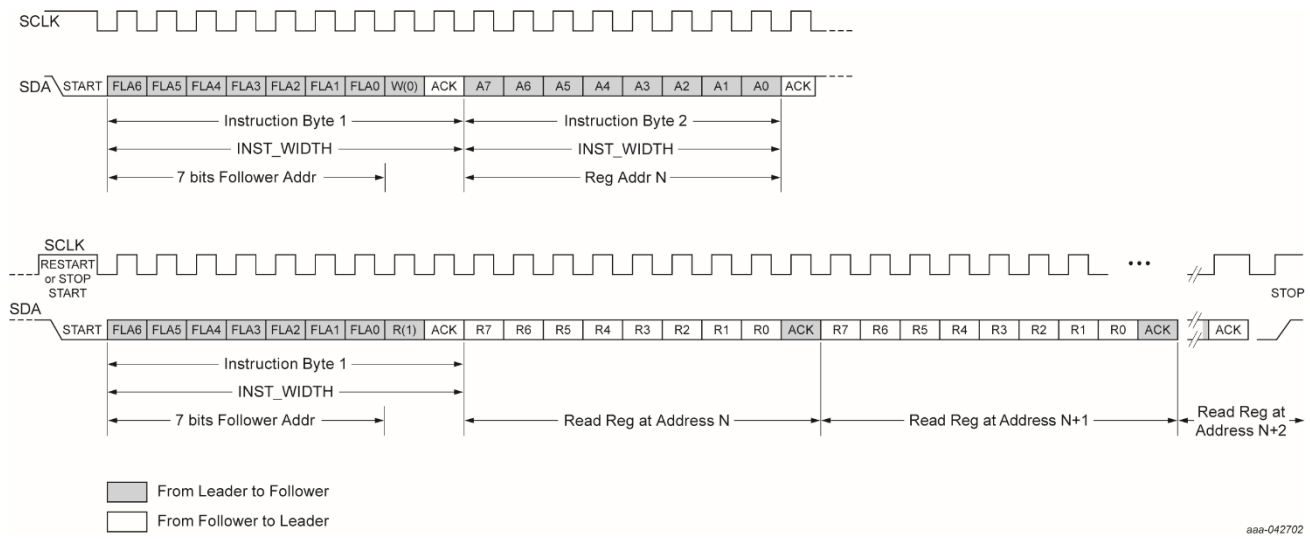



**Figure 11. I²C Read instruction**

### 14.2.2.3 I²C Write and Read combination sequence

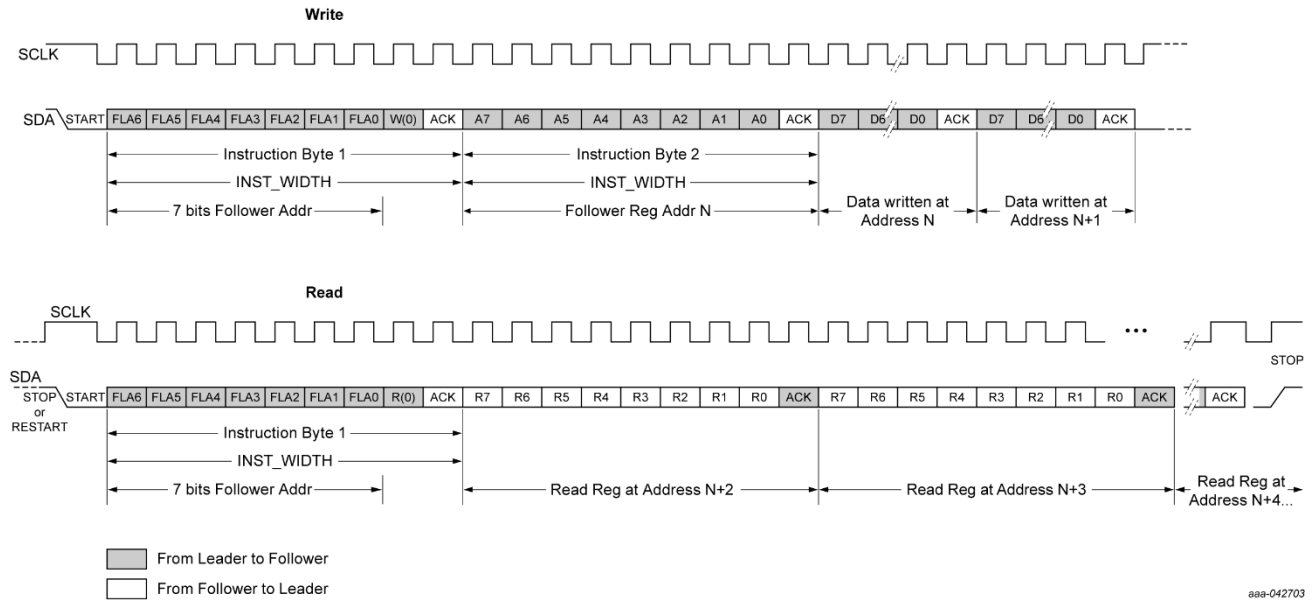



**Figure 12. I²C Write and Read combination sequence**

## 14.2.3 I²C Device ID Read instruction

The Device ID is read only, hardwired in the device and can be accessed as follows:

1. START condition
2. The leader sends the Reserved Device ID I²C bus address followed by the R/W bit set to '0' (write): '1111 1000'.
3. The leader sends the I²C bus follower address of the follower device it must identify. The LSB is a "don't care" value. Only one device must acknowledge this byte (the device that has the I²C bus follower address).
4. The leader sends a RESTART condition.

**Remark:** A STOP condition followed by a START condition resets the follower state machine and the Device ID read cannot be performed. Also, a STOP condition or a RESTART condition followed by an access to another follower device resets the follower state machine and the Device ID read cannot be performed.

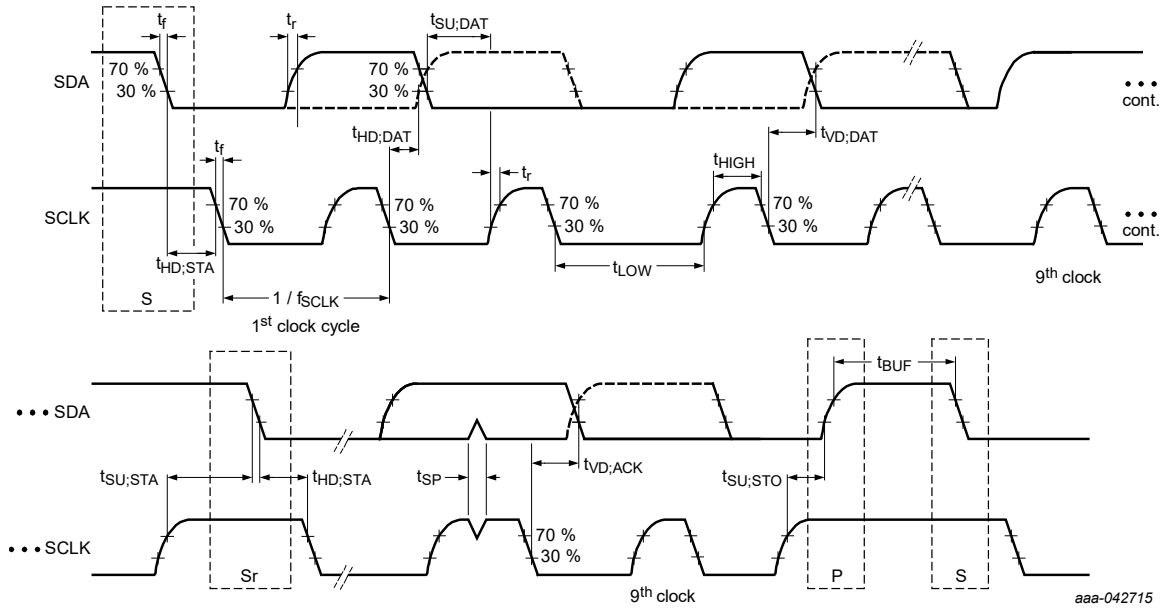
1. The leader sends the Reserved Device ID I²C bus address followed by the R/W bit set to '1' (read): '1111 1001'.
2. The Device ID read can be completed, starting with the 12 manufacturer bits (first byte + four MSBs of the second byte), followed by the nine part identification bits (four LSBs of the second byte + five MSBs of the third byte), and then the three die revision bits (three LSBs of the third byte).
3. The leader ends the reading sequence by NACKing the last byte, thus resetting the follower device state machine and allowing the leader to send the STOP condition.

**Remark:** The reading of the Device ID can be stopped anytime by sending a NACK.

**Table 21. I²C Device Read instructions**

| Leader to Follower | Leader to Follower | Leader to Follower | Leader to Follower | Leader to Follower | Follower to Leader | Leader to Follower | Leader to Follower |
|---|---|---|---|---|---|---|---|
| START | 1111 1000 | XXXXXXX+'0/1' | RESTART | 1111 1001 | 3 bytes ID | NACK | STOP |

## 14.3 I²C electrical specification and timing for I/O stages and bus lines




Note: $V_{IL}$ = 0.3 $V_{DD}$, $V_{IH}$ = 0.7 $V_{DD}$

**Figure 13. I²C electrical specification and timing for I/O stages and bus lines**

### 14.3.1 I²C SCLK and SDA characteristics

**Table 22. I²C SCLK and SDA**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK clock frequency | — | 0 | 400 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition | After this period, the first clock pulse is generated. | 0.6 | — | µs |
| $t_{LOW}$ | Low period of the SCLK clock[1] | — | 1.3 | — | µs |
| $t_{HIGH}$ | High Period of the SCLK clock | — | 0.6 | — | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | — | 0.6 | — | µs |
| $t_{HD;STA}$ | Data hold time[2] | BBUS-compatible masters | — | — | µs |
| | | I²C bus devices | 0 | — | µs |
| $t_{SU;STA}$ | Data setup time | — | 100[3] | — | µs |
| $t_r$ | Rise time of both SDA and SCLK signals | — | 20 | 300 | ns |
| $t_f$ | Fall time of both SDA and SCLK signals[4], [5], [6] | — | 6.5 | 300 | ns |
| $t_{SU;STA}$ | Setup time for STOP condition | — | 0.6 | — | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | — | 1.3 | — | µs |
| $t_{VD;DAT}$ | Data valid time[7] | — | — | 0.9 | µs |
| $t_{VD;ACK}$ | Data valid acknowledge time[6] | — | — | 0.9 | µs |

[1] Note: All values referred to $V_{IH(min)}$ (0.3 $V_{DD}$) and $V_{IL(max)}$(0.7 $V_{DD}$) level.

[2] $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCLK and applies to data in transmission and the Acknowledge.

[3] A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement $t_{SU:DAT}$ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCLK signal. If such a device does not stretch the LOW period of the SCLK signal, it must output the next data bit to the SDA line $t_{r(max)}$ + $t_{SU;DATA}$ = 1000 + 250 = 1250 ns (according to the Standard Mode I²C Bus Specification) before the SCLK line is released. Also the Acknowledge timing must meet this setup time.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

[5] The maximum $t_{HD:DAT}$ could be 3.45 µs and 0.9 µs for standard mode and fast mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period ($i_{LOW}$) of the SCLK signal. If the clock stretches the SCLK, the data must be valid by the setup mode before it releases the clock.

[6] $t_{VD;ACK}$ = time for Acknowledgement signal from SCLK LOW to SDA output (HIGH or LOW, depending on which one is longer).

[7] $t_{VD:DAT}$ = time for data signal from SCLK LOW to SDA output (HIGH or LOW, depending on which one is longer).

### 14.3.2 I²C bus electrical characteristics

**Table 23. I²C SCLK and SDA**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | LOW-level input voltage | — | — | 0.3*$V_{DD}$[1] | V |
| $V_{IH}$ | HIGH-level input voltage | — | 0.7*$V_{DD}$[1] | — | V |
| $V_{hys}$ | Hysteresis of Schmitt trigger inputs | — | 0.05*$V_{DD}$[1] | — | V |
| $V_{OL}$ | LOW-level output voltage | (Open-drain/open-collector) at 2 mA sink current $V_{DD}$[1] = < 2 V | 0 | 0.2*$V_{DD}$[1] | V |
| $V_{OH}$ | HIGH-level output voltage | (Open-drain/open-collector) | 0.7*$V_{DD}$[1] | $V_{DD}$[1] | V |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V | 3 | — | mA |
| | | $V_{OL}$ = 0.6 V | 6 | — | mA |
| $I_{iL}$ | Input leakage current at the pin | $V_{DD}$ = 1.8, Pin voltage = 1.8 V, 0.1 $V_{DD}$ < VI < 0.9 $V_{DD}$[1] | –10 | 10 | µA |
| $C_i$ | Capacitance for each I/O pin | — | — | 10 | pF |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by the input filter | — | 0 | 50 | ns |
| $t_{of}$ | Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ | Pullup res = 250 ohm and max allowed load capacitance $C_b$ | — | 250 | ns |
| $C_b$ | Capacitive load for each bus line[2] | — | — | 400 | pF |

[1] $V_{DD}$ in this table refers to 1.8 V provided by the Leader.

[2] The maximum $t_f$ for the SDA and SCLK bus lines is specified at 300 ns. This allows series protection resistors to be connected in between the SDA and the SCLK pins and the SCLK bus lines without exceeding the maximum specified $t_f$.

# 15 Design considerations

## 15.1 Power on sequence

The initial power on sequence will take approximately 200 µs to complete the OTP memory fetching process. Therefore, it is suggested to wait at least 200 µs before issuing the SPI or I²C read and write processes. The normal SPI or I²C read and write processes should follow the sequence illustrated in Figure 14, “Power on sequence timing diagram.”

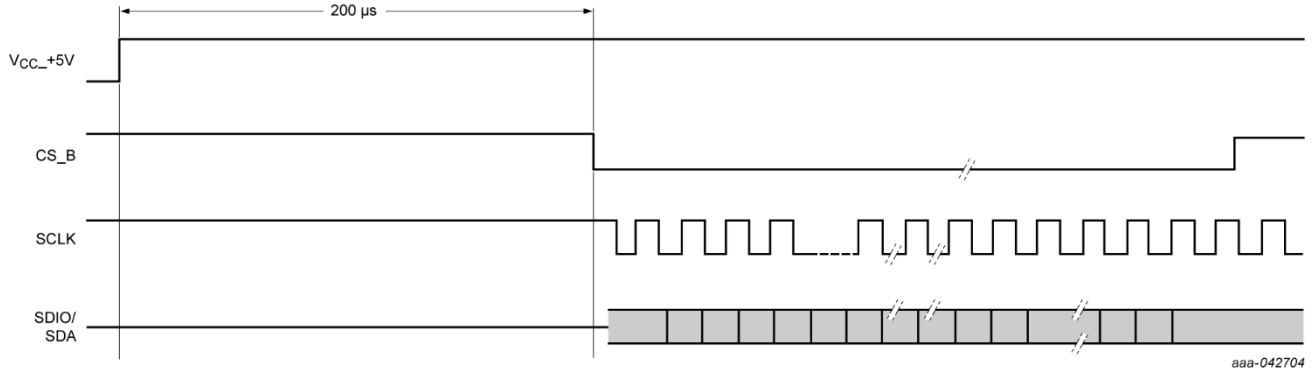



**Figure 14. Power on sequence timing diagram**

## 15.2 Programming guidelines to avoid hardware failure or damage

Users must be aware of the following guidelines to avoid potential hardware failure or damage.

- Do not program the Refresh OTP and Soft Reset bits to a 1 state at the same time.
- Soft Reset bit will reset Engineering Mode (EM).
- The Soft Reset bit is easily accessible; therefore, be cautious of the accidental reset.
- Tx_EN must not be active during an OTP refresh or during Engineering Mode.

## 15.3 Group programming

A common way of grouping A5M36SG239 modules is with parallel data inputs and unique chip CS_B connectivity. In this case, each module can be independently controlled and programmed by its individual CS_B, which has more flexibility to program each module separately as Figure 15 illustrates.

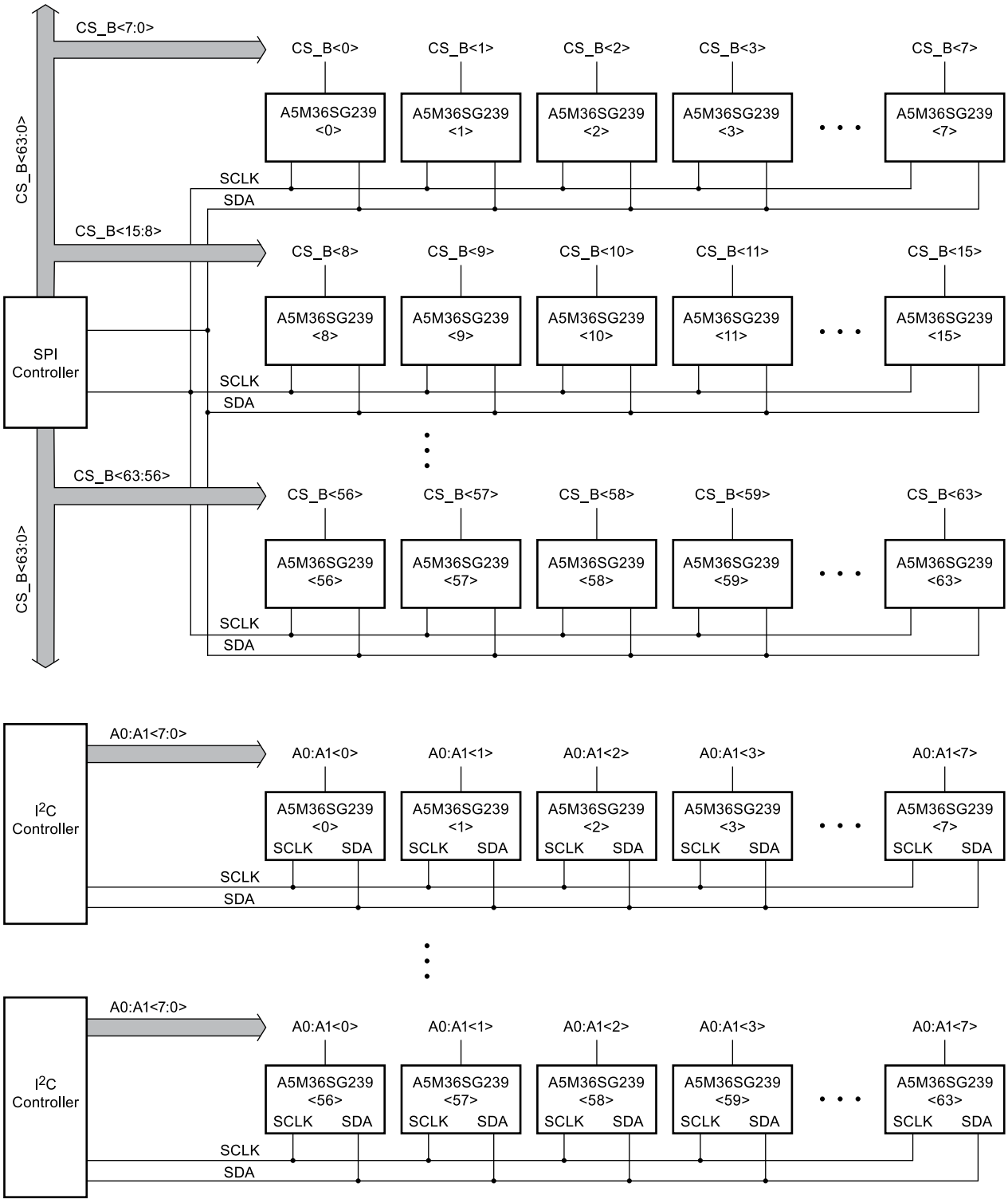



**Figure 15. Parallel connectivity of grouping**

# 16 Package information

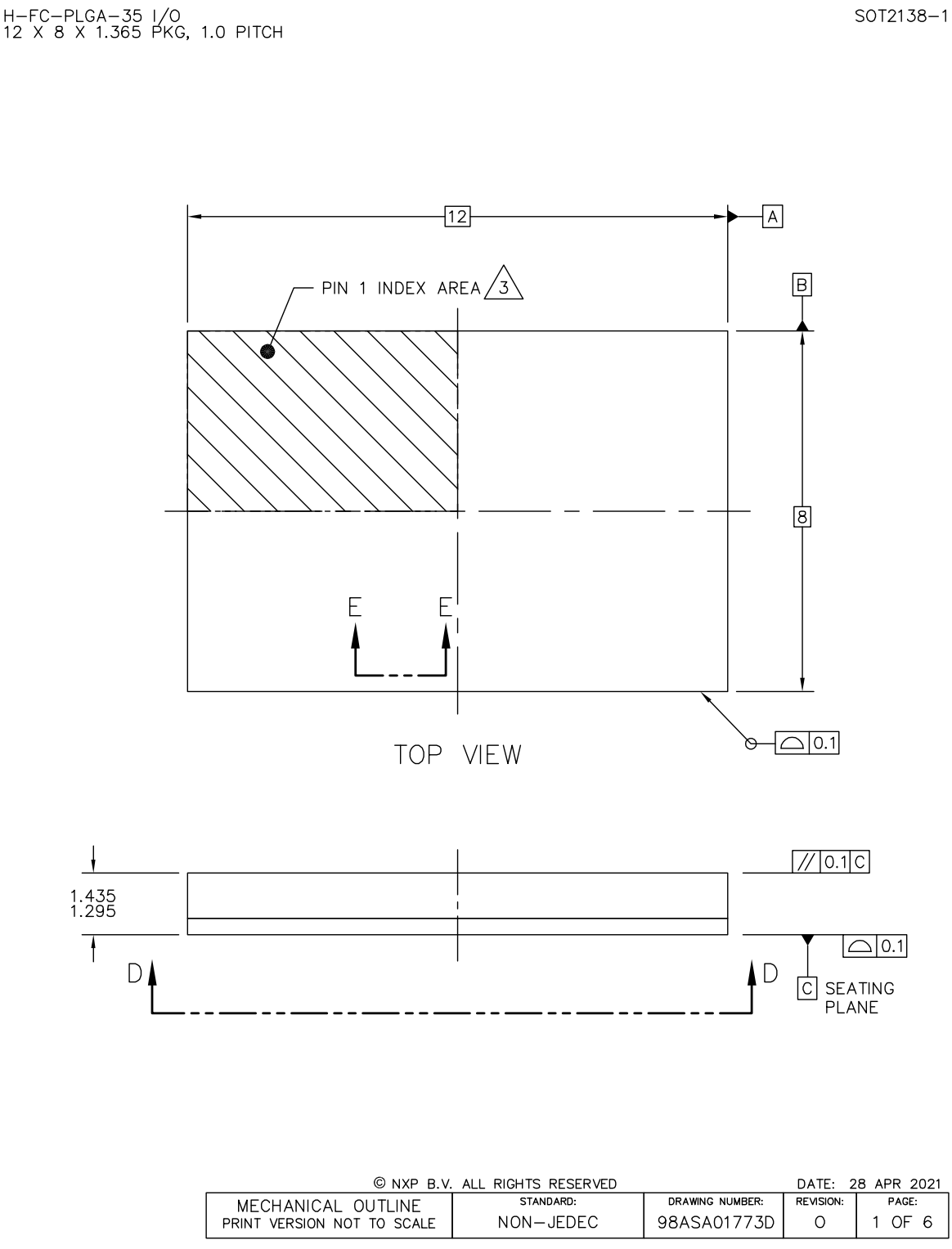



**Figure 16. Package outline (12 mm × 8 mm Module) — top view**

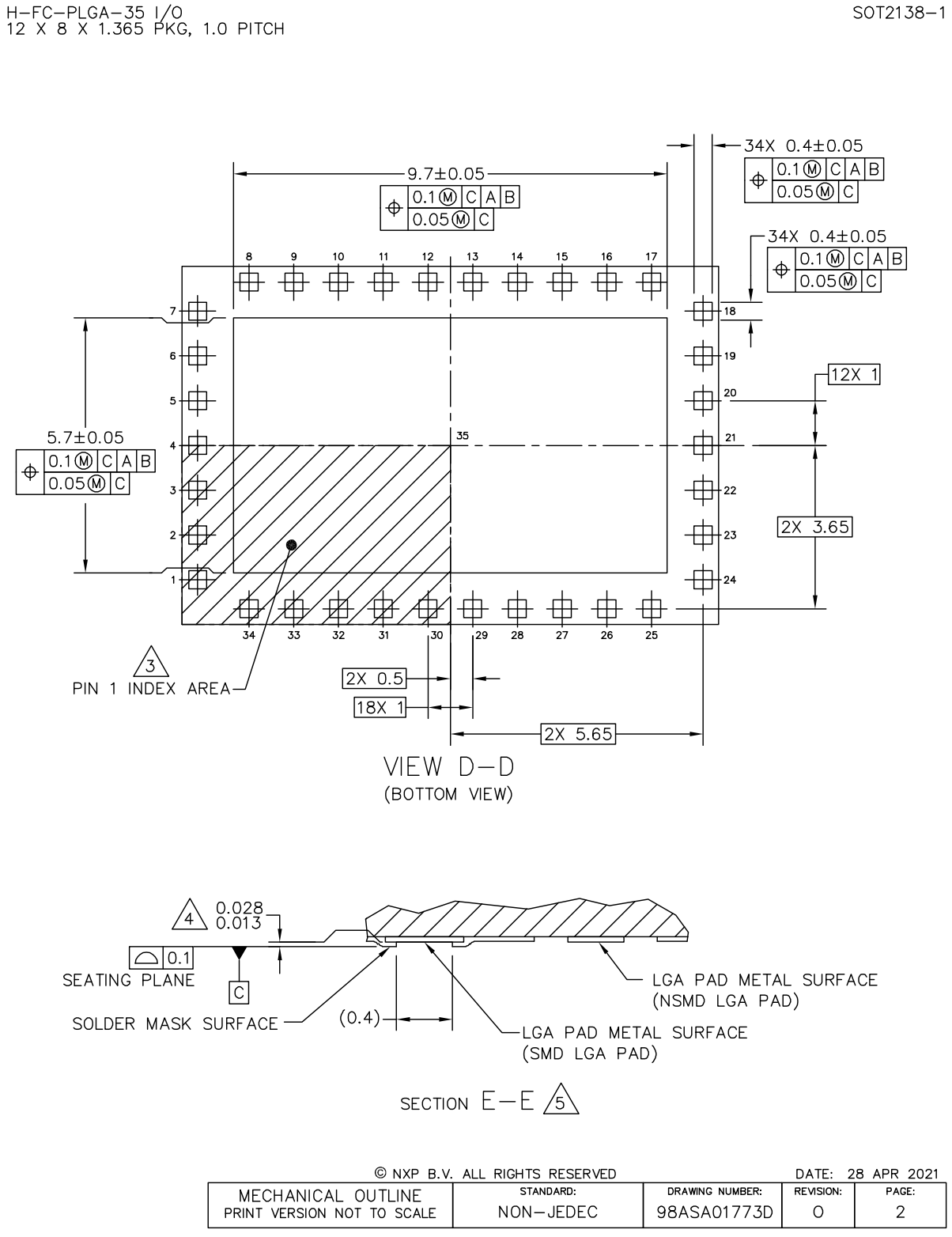
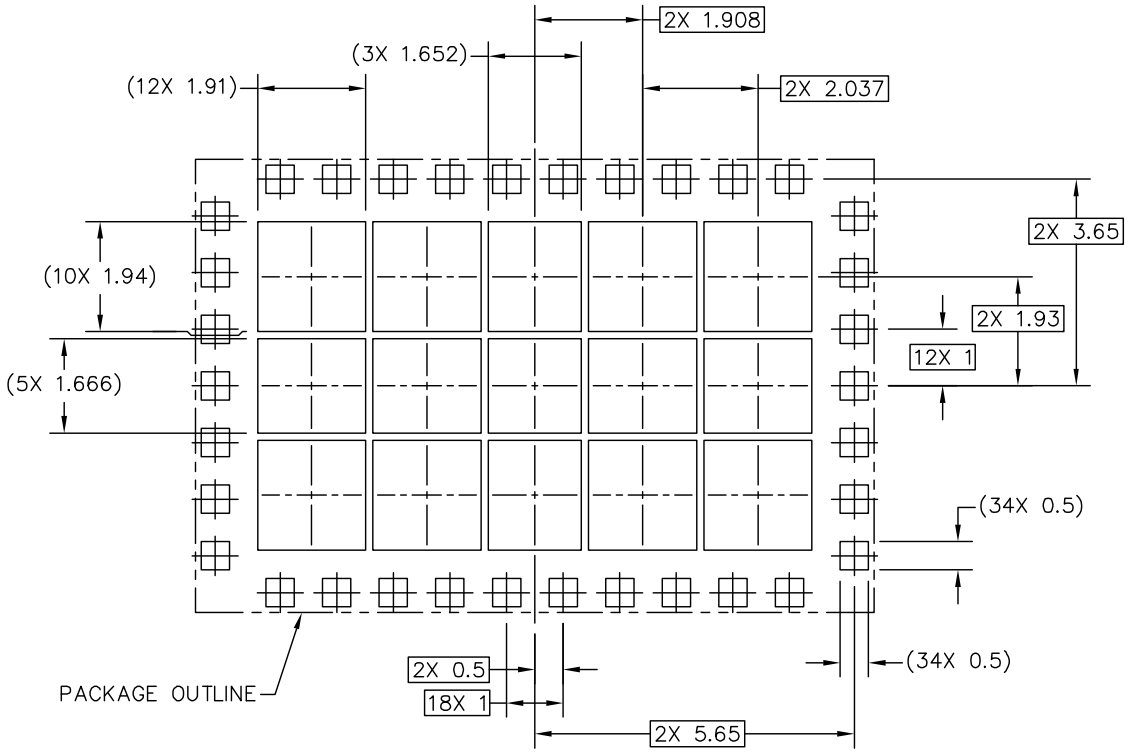



**Figure 17. Package outline (12 mm × 8 mm Module) — bottom view**

H–FC–PLGA–35 I/O
12 X 8 X 1.365 PKG, 1.0 PITCH

SOT2138–1




PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



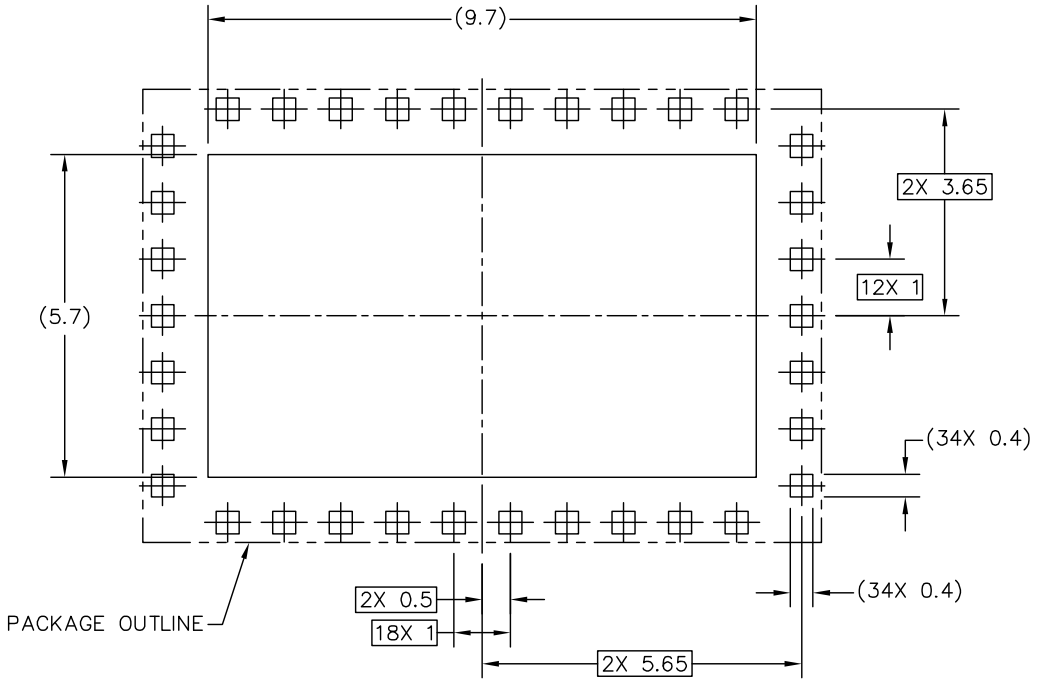
DATE: 28 APR 2021

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON–JEDEC | DRAWING NUMBER:<br>98ASA01773D | REVISION:<br>O | PAGE:<br>3 |
|---|---|---|---|---|

**Figure 18. Package outline (12 mm × 8 mm Module) — PCB design guidelines: solder mask opening pattern**

H–FC–PLGA–35 I/O
12 X 8 X 1.365 PKG, 1.0 PITCH

SOT2138–1




PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREAS

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



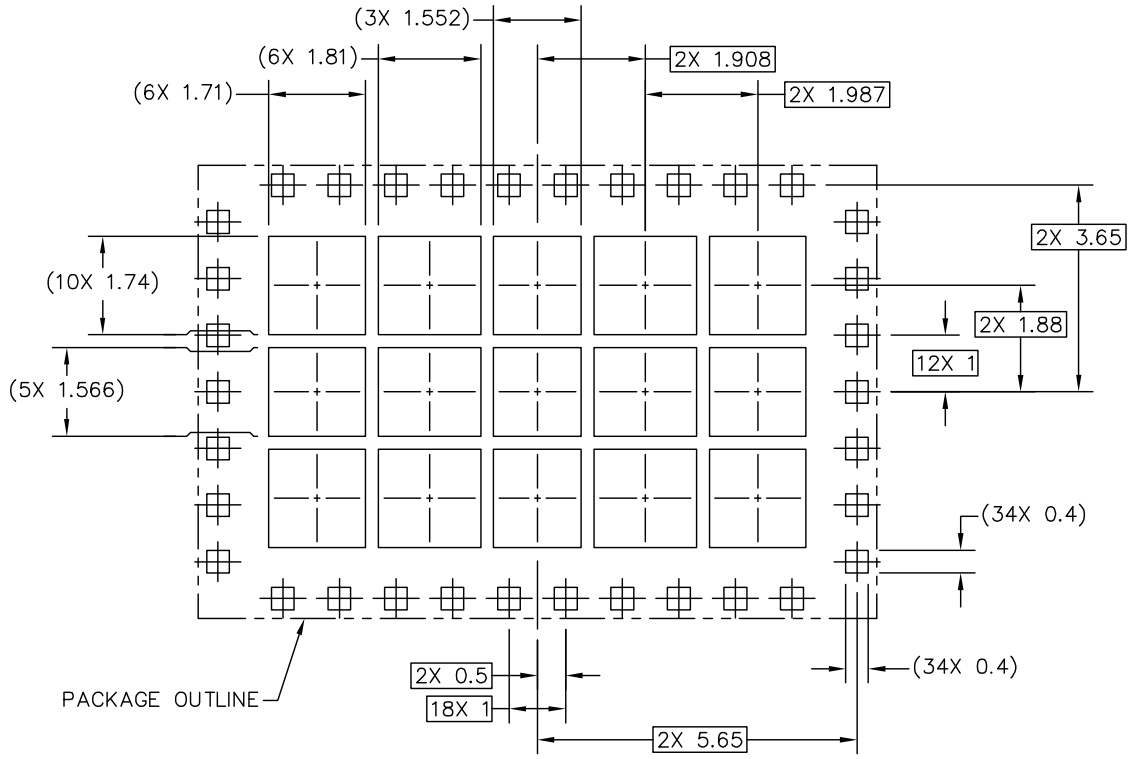
DATE: 28 APR 2021

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON–JEDEC | DRAWING NUMBER:<br>98ASA01773D | REVISION:<br>O | PAGE:<br>4 |
|---|---|---|---|---|

**Figure 19. Package outline (12 mm × 8 mm Module) — PCB design guidelines: I/O pads and solderable areas**

H–FC–PLGA–35 I/O
12 X 8 X 1.365 PKG, 1.0 PITCH

SOT2138–1




RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.



DATE: 28 APR 2021

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON–JEDEC | DRAWING NUMBER:<br>98ASA01773D | REVISION:<br>O | PAGE:<br>5 |
|---|---|---|---|---|

**Figure 20. Package outline (12 mm × 8 mm Module) — PCB design guidelines: solder paste stencil**

H–FC–PLGA–35 I/O
12 X 8 X 1.365 PKG, 1.0 PITCH

SOT2138–1

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. DIMENSION APPLIES TO ALL LEADS AND FLAG.
5. THE BOTTOM VIEW SHOWS THE SOLDERABLE AREA OF THE PADS. THE CENTER PAD (PIN 35) IS SOLDER MASK DEFINED. SOME PERIPHERAL PADS ARE SOLDER MASK DEFINED (SMD) AND OTHERS ARE NON–SOLDERMASK DEFINED (NSMD).



DATE: 28 APR 2021

| MECHANICAL OUTLINE<br>PRINT VERSION NOT TO SCALE | STANDARD:<br>NON–JEDEC | DRAWING NUMBER:<br>98ASA01773D | REVISION:<br>O | PAGE:<br>6 |
|---|---|---|---|---|

**Figure 21. Package outline (12 mm × 8 mm Module) — notes**

# 17 Product software and tools

Refer to the following resources to aid your design process.

**Development Software**

- Test, Debug and Analyzer Software

**Development Tools**

- Printed Circuit Boards

# 18 Failure analysis

At this time, because of the physical characteristics of the part, failure analysis is limited to electrical signature analysis. In cases where NXP is contractually obligated to perform failure analysis (FA) services, full FA may be performed by third party vendors with moderate success. For updates contact your local NXP Sales Office.

# 19 Revision history

The following table summarizes revisions to this document.

**Table 24. Revision history**

| Revision | Date | Description |
|---|---|---|
| 0 | 10 October 2023 | • Initial release of data sheet |

# 20 Legal information

## 20.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 20.2 Definitions

**Draft** — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 20.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Suitability for use in non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

**Security** — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

**NXP B.V.** — NXP B.V. is not an operating company and it does not distribute or sell products.

## 20.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

**NXP** — wordmark and logo are trademarks of NXP B.V.

**Airfast** — is a trademark of NXP B.V.

# Contents





For more information, please visit: http://www.nxp.com

**Date of release: 10 October 2023**
**Document identifier: A5M36SG239**