P-Channel Power MOSFET

FEATURES

- Advance trench process technology
- High density cell design for ultra-low on-resistance
- RoHS compliant
- Halogen-free

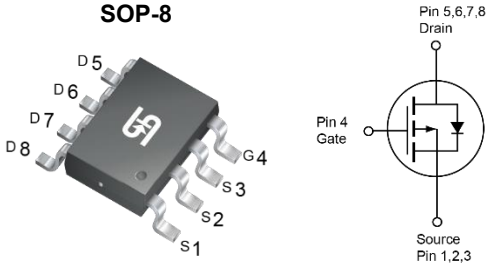
APPLICATIONS

- Battery protection
- Load switch

KEY PERFORMANCE PARAMETERS			
PARAMETER		**VALUE**	**UNIT**
V_{DS}		-60	V
$R_{DS(on)}$ (max)	V_{GS} = -10V	155	mΩ
	V_{GS} = -4.5V	200	
Q_g		18	nC

Pb-Free RoHS COMPLIANT HALOGEN FREE

SOP-8



Note: MSL 3 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	-60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25°C	I_D	-3	A
Pulsed Drain Current (Note 1)		I_{DM}	-12	A
Total Power Dissipation	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

THERMAL PERFORMANCE			
PARAMETER	**SYMBOL**	**LIMIT**	**UNIT**
Junction to Ambient Thermal Resistance (Note 2)	$R_{\Theta JA}$	50	°C/W

Notes:

1. Pulse Width ≤ 100μs.
2. Device on a PCB FR4 with 1 in^2 (single layer, 2 oz thickness) copper area for drain connection.

ELECTRICAL SPECIFICATIONS (T_A = 25°C unless otherwise noted)						
PARAMETER	**CONDITIONS**	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**
Static (Note 3)						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	BV_{DSS}	-60	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	$V_{GS(TH)}$	-1	-1.9	-2.5	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -60V, V_{GS} = 0V	I_{DSS}	--	--	-1	μA
Drain-Source On-State Resistance	V_{GS} = -10V, I_D = -3A	$R_{DS(on)}$	--	36	155	mΩ
	V_{GS} = -4.5V, I_D = -2.7A		--	47	200	
Forward Transconductance	V_{DS} = -10V, I_D = -0.8A	g_{fs}	--	5.9	--	S
Dynamic (Note 4)						
Total Gate Charge	V_{DS} = -30V, I_D = -3A, V_{GS} = -10V	Q_g	--	18	--	nC
Gate-Source Charge		Q_{gs}	--	3.3	--	
Gate-Drain Charge		Q_{gd}	--	2.9	--	
Input Capacitance	V_{DS} = -30V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	1101	--	pF
Output Capacitance		C_{oss}	--	359	--	
Reverse Transfer Capacitance		C_{rss}	--	29	--	
Switching (Note 5)						
Turn-On Delay Time	V_{DD} = -30V, R_G = 6Ω, I_D = -3A, V_{GS} = -10V	$t_{d(on)}$	--	6.4	--	ns
Turn-On Rise Time		t_r	--	2.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	58	--	
Turn-Off Fall Time		t_f	--	32	--	
Source-Drain Diode						
Forward Voltage (Note 3)	I_S = -3A, V_{GS} = 0V	V_{SD}	--	-0.8	-1.5	V

Notes:

3. Pulse test: Pulse Width ≤ 300μs, duty cycle ≤ 2%.
4. Defined by design. Not subject to production test.
5. Switching time is essentially independent of operating temperature.

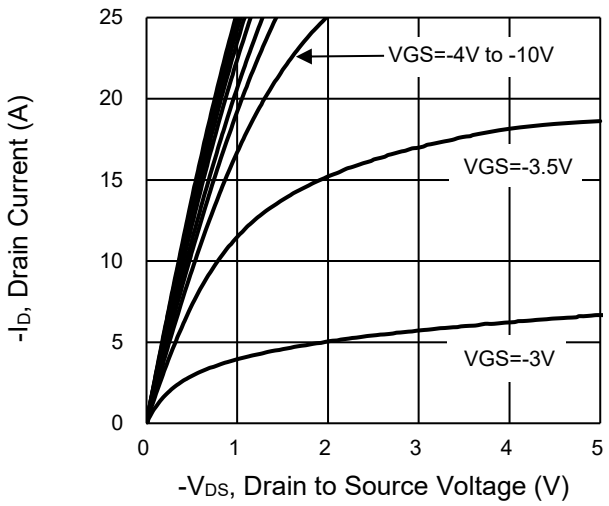
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM9409CS RLG	SOP-8	2.5kpcs / 13” Reel

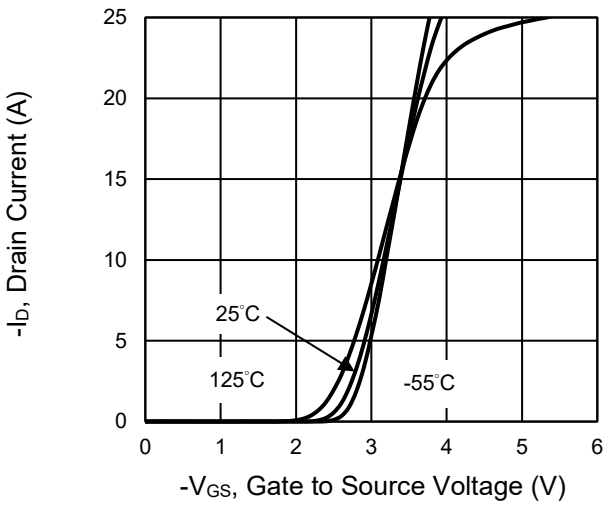
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

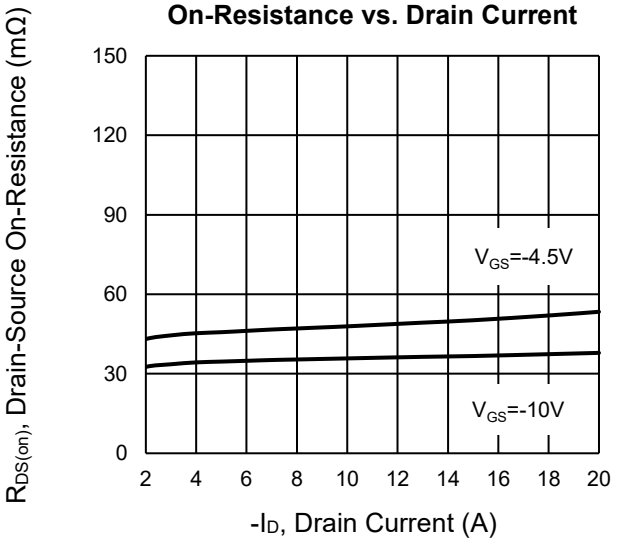
Output Characteristics



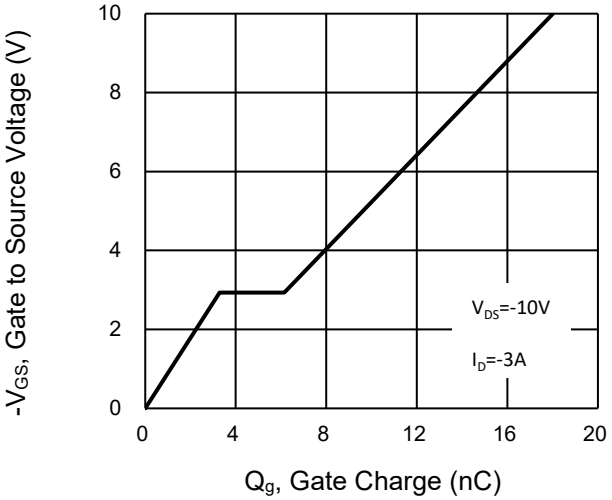
Transfer Characteristics



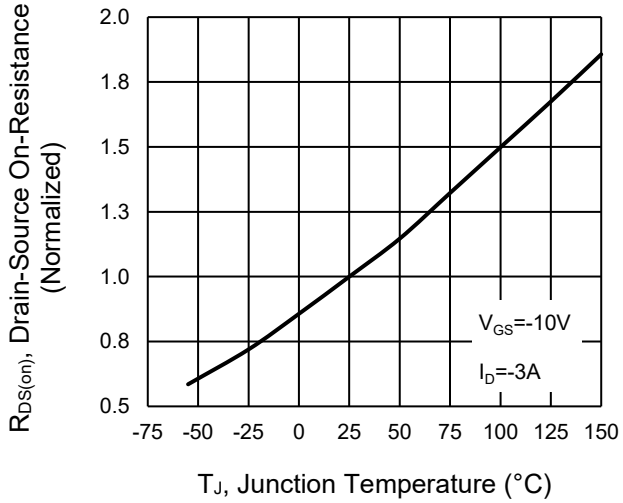
On-Resistance vs. Drain Current



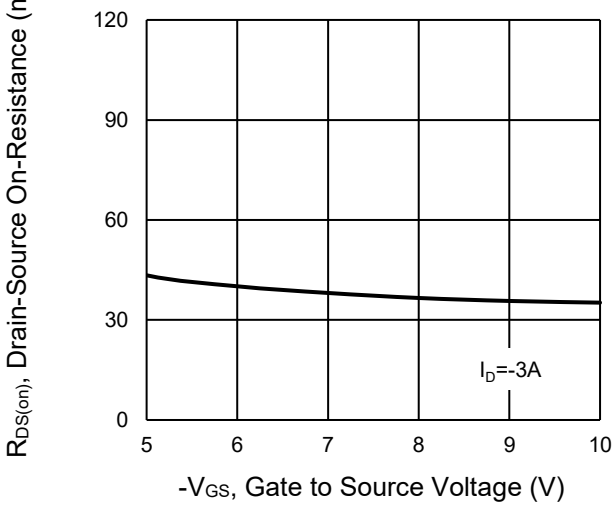
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



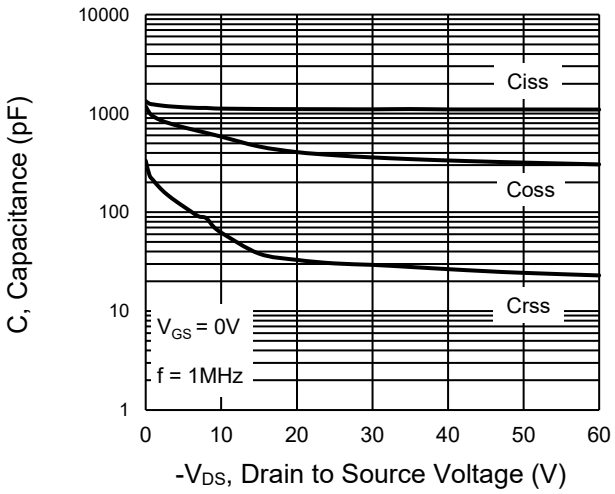
On-Resistance vs. Gate-Source Voltage



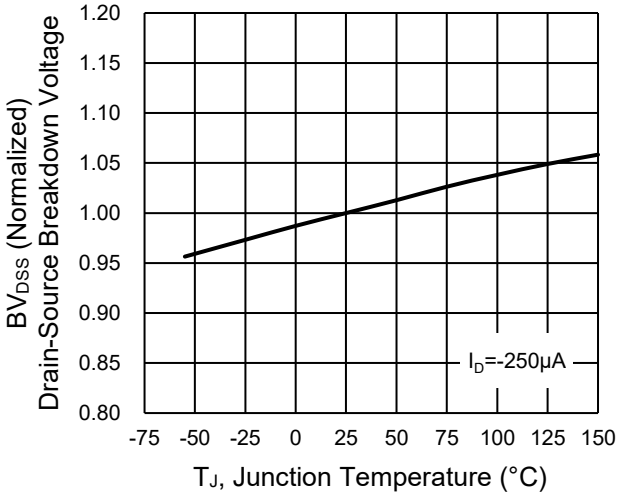
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

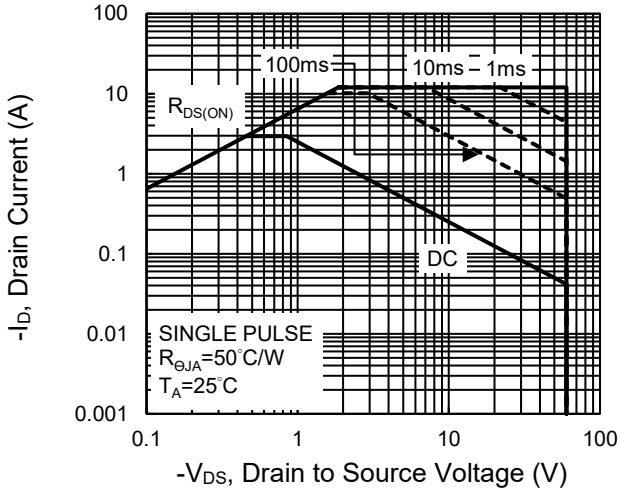
Capacitance vs. Drain-Source Voltage



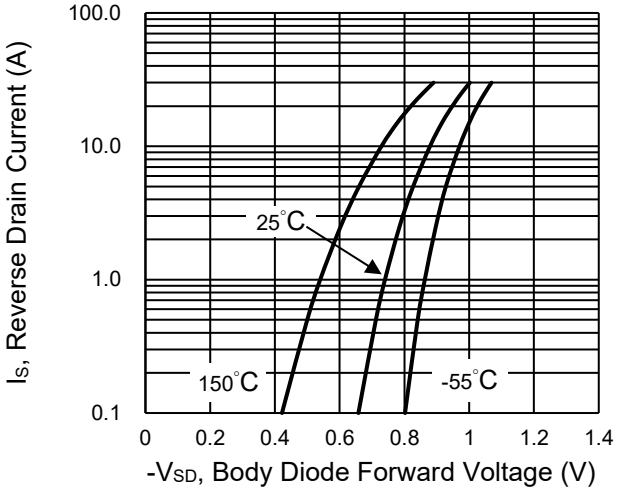
BV_{DSS} vs. Junction Temperature



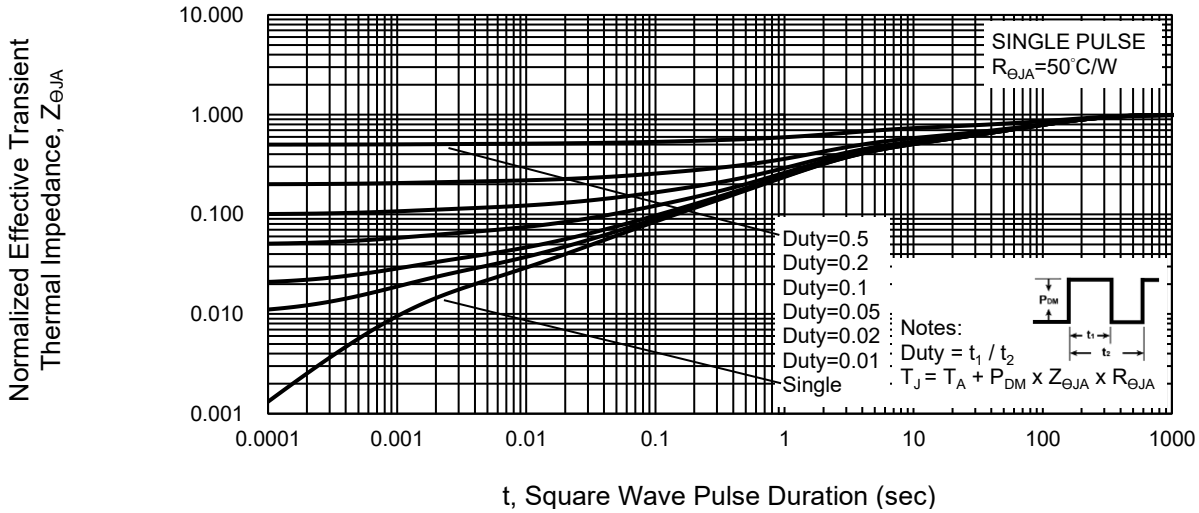
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage



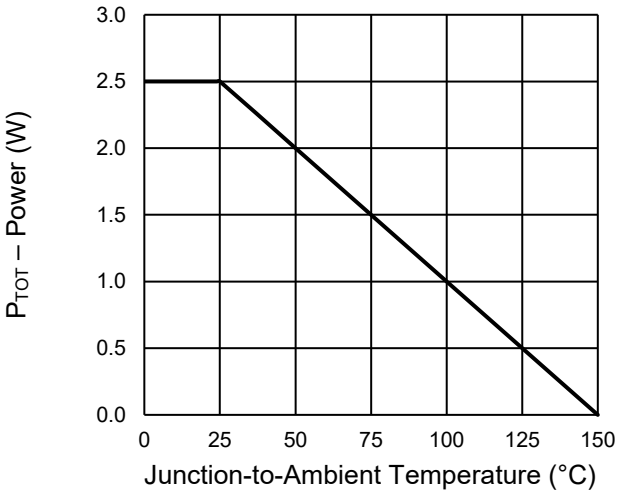
Normalized Thermal Transient Impedance, Junction-to-Ambient



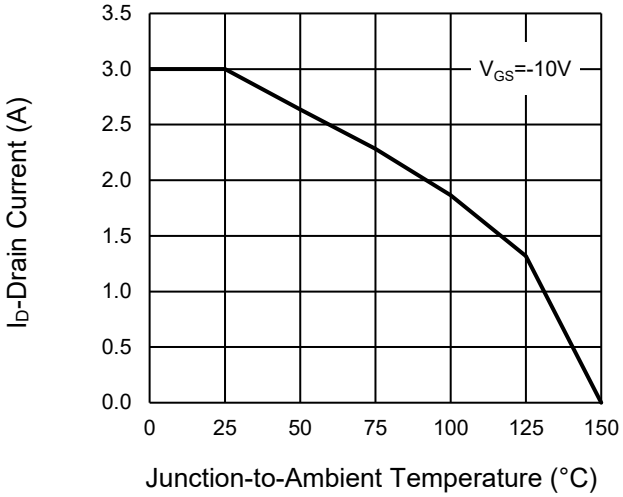
CHARACTERISTICS CURVES

(T_A = 25°C unless otherwise noted)

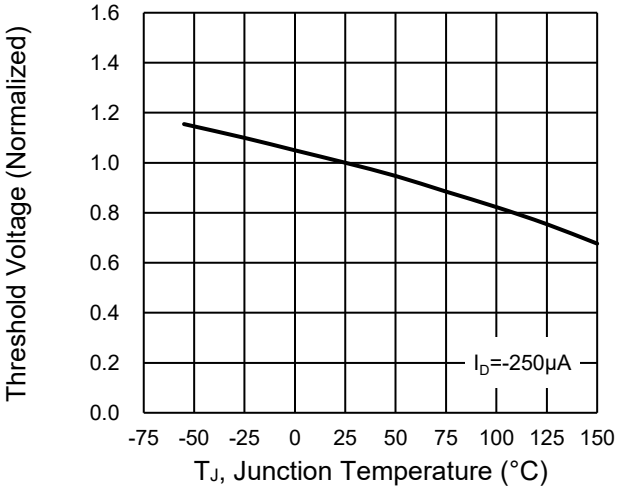
Power Dissipation



Drain Current

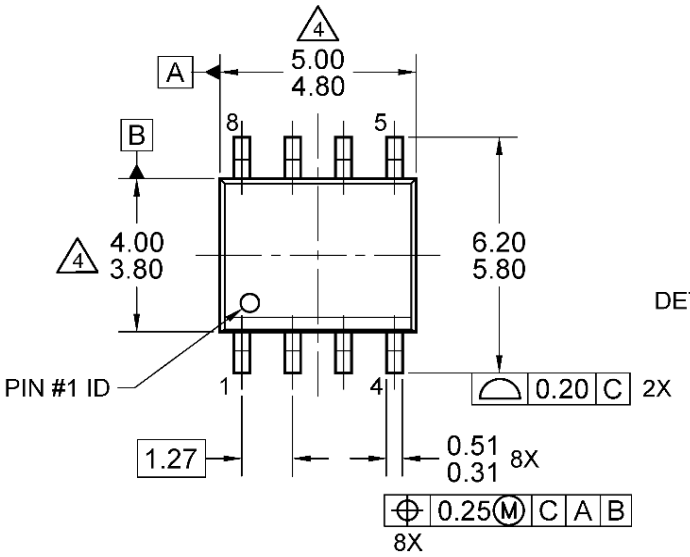


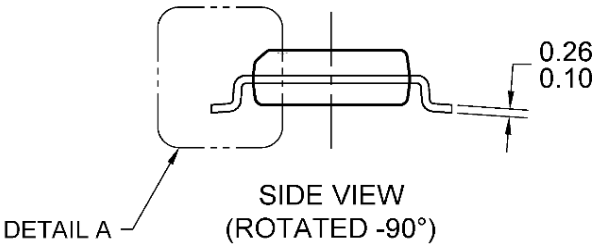
Normalized gate threshold voltage vs Temperature

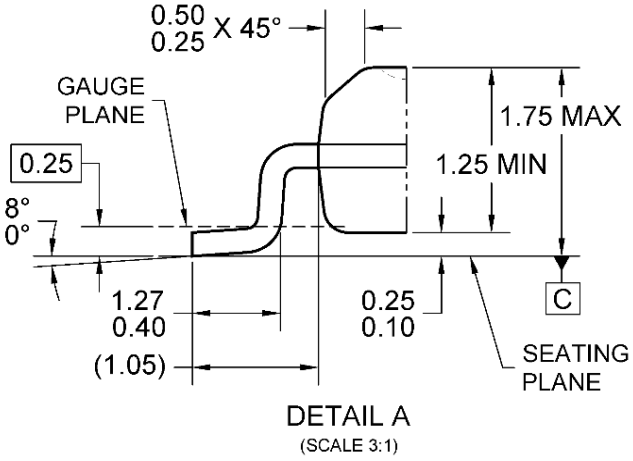


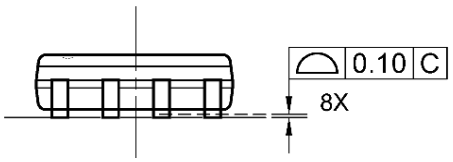
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

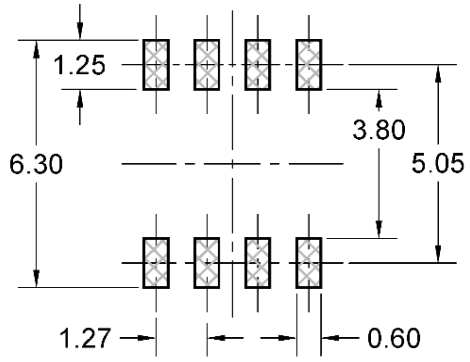
SOP-8

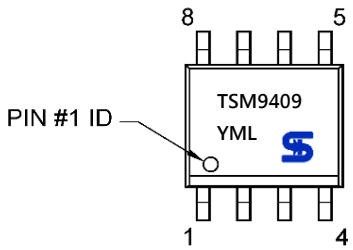












MARKING DIAGRAM

Y = YEAR CODE

M = MONTH CODE FOR HALOGEN FREE PRODUCT

O =JAN	P =FEB	Q=MAR	R = APR
S =MAY	T =JUN	U=JUL	V = AUG
W =SEP	X =OCT	Y=NOV	Z = DEC

L = LOT CODE

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PACKAGE OUTLINE REFERENCE: JEDEC MS-012, ISSUE G, VARIATION AA.
4. MOLDED PLASTIC BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
5. DWG NO REF: HQ2SD07-SOP8STD-028 REV A.

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