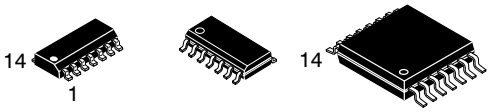
LVDS 1-Bit, High-Speed Differential Reciever

MM74HC164



SOIC−14 NB
CASE 751A−03

SOIC−14,
CASE 751EF

TSSOP−14 NB
CASE 948G

Description

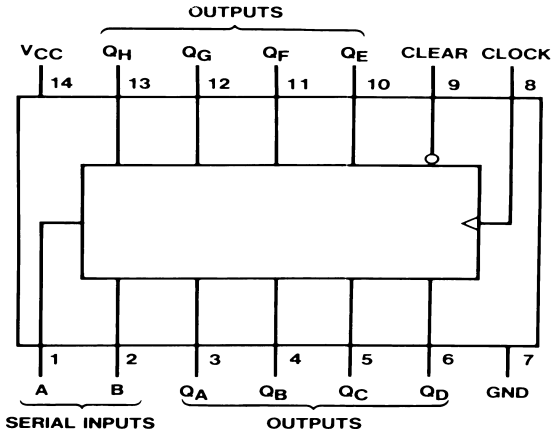
The MM74HC164 utilizes advanced silicon−gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8−bit shift register has gated serial inputs and CLEAR. Each register bit is a D−type master/slave flip− flop. Inputs A & B permit complete control over the incoming data. A LOW at either or both inputs inhibits entry of new data and resets the first flip−flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip−flop. Data at the serial inputs may be changed while the clock is HIGH or LOW, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8−bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 74HC logic family is functionally as well as pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

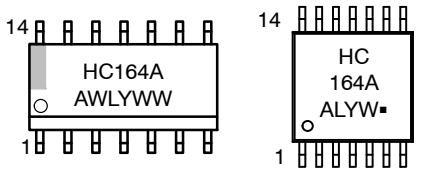
- Typical Operating Frequency: 50 MHz
- Typical Propagation Delay: 19 ns (clock to Q)
- Wide Operating Supply Voltage Range: 2 V to 6 V
- Low Input Current: 1 μA maximum
- Low Quiescent Supply Current: 160 μA maximum (74HC Series)
- Fanout of 10 LS−TTL Loads



Top View

Figure 1. Connection Diagram

MARKING DIAGRAMS



(SOIC−14, SOIC−14NB)

(TSSOP−14NB)

HC164A = Specific Device Code
A = Assembly Location
L/WL = Wafer Lot
Y/YY = Year
W/WW = Work Week
G = Pb−Free Package

TRUTH TABLE

Inputs				Outputs	
Clear	Clock	A	B	Q_A	Q_B … Q_H
L	X	X	X	L	L … L
H	L	X	X	Q_{AO}	Q_{BO}… Q_{HO}
H	↑	H	H	H	Q_{An} … Q_{Gn}
H	↑	L	X	L	Q_A … Q_{Gn}
H	↑	X	L	L	Q_{An} … Q_{Gn}

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOW−to−HIGH level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent = transition of the clock; indicated a one−bit shift.

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

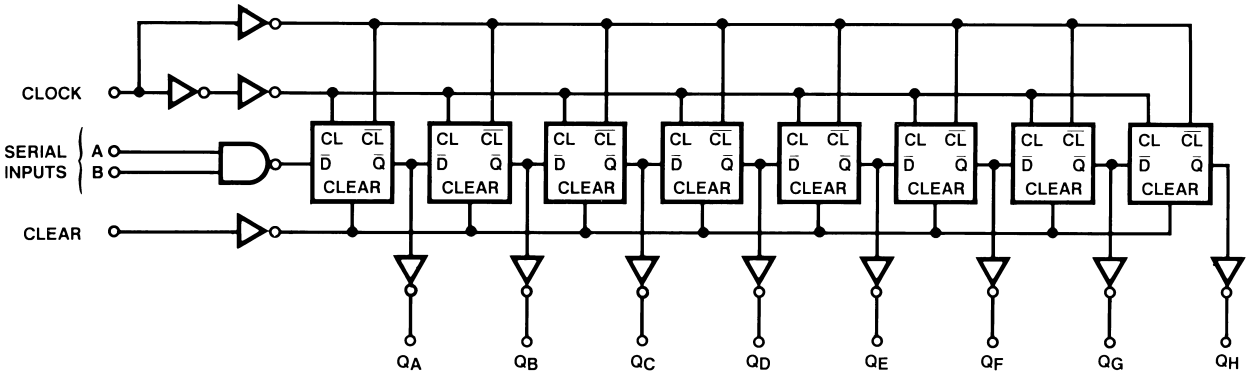


Figure 2. Logic Diagram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	−0.5 to +7.0	V
V_{IN}	DC Input Voltage	−0.5 to V_{CC}+0.5	V
V_{OUT}	DC Output Voltage	−0.5 to V_{CC}+0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per pin	±25	mA
I_{CC}	Maximum Junction Temperature	±50	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
P_D	Power Dissipation S.O. Package only	500	mW
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2	6	V
V_{IN},V_{OUT}	Input Voltage	0	V_{CC}	V
T_A	Magnitude of Differential Voltage	−55	+125	°C
t_r, t_f	Input Rise or Fall Times V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	 – – –	 1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 2)

Symbol	Parameter	V_{CC} (V)	Test Conditions	$T_A = 25°C$	$T_A = -40°C$ to $85°C$	$T_A = -55°C$ to $125°C$	Unit
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	2.0	–	–	1.5	1.5	1.5	V
		4.5		–	3.15	3.15	3.15	
		6.0		–	4.2	4.2	4.2	
V_{IL}	Maximum LOW Level Input Voltage	2.0	–	–	0.5	0.5	0.5	V
		4.5		–	1.35	1.35	1.35	
		6.0		–	1.8	1.8	1.8	
V_{OH}	Minimum HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20$ μA	2.0	1.9	1.9	1.9	V
		4.5		4.5	4.4	4.4	4.4	
		6.0		6.0	5.9	5.9	5.9	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0$ mA	4.2	3.98	3.84	3.7	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 5.2$ mA	5.7	5.48	5.34	5.2	
V_{OL}	Maximum LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 20$ μA	0	0.1	0.1	0.1	V
		4.5		0	0.1	0.1	0.1	
		6.0		0	0.1	0.1	0.1	
		4.5	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 4.0$ mA	0.2	0.26	0.33	0.4	
		6.0	$V_{IN} = V_{IH}$ or V_{IL}, $\|I_{OUT}\| \le 5.2$ mA	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND	–	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ μA	–	8.0	80	160	μA

2. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns)

Symbol	Parameter	Typ.	Guaranteed Limit	Unit
f_{MAX}	Maximum Operating Frequency	–	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output	19	30	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output	23	35	ns
t_{REM}	Minimum Removal Time, Clear to Clock	–2	0	ns
t_S	Minimum Setup Time, Data to Clock	12	20	ns
t_H	Minimum Hold Time, Clock to Data	1	5	ns
tW	Minimum Pulse Width, Clear or Clock	10	16	ns

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	Test Conditions	T_A = 25°C	T_A = –40°C to 85°C	T_A = –55°C to 125°C		Unit
				Typ.	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	2.0		–	5	4	3	MHz
		4.5		–	27	21	18	
		6.0		–	31	24	20	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output	2.0	–	115	175	218	254	ns
		4.5		13	35	44	51	
		6.0		20	30	38	44	
t_{PHL}	Maximum Propagation Delay, Clear to Output	2.0	–	140	205	256	297	ns
		4.5		28	41	51	59	
		6.0		24	35	44	51	
t_{REM}	Minimum Removal Time, Clear to Clock	2.0	–	–7	0	0	0	ns
		4.5	–	–3	0	0	0	
		6.0	–	–2	0	0	0	
t_S	Minimum Setup Time, Data to Clock	2.0	–	25	100	125	150	ns
		4.5		14	20	25	30	
		6.0		12	17	21	25	
t_H	Minimum Hold Time, Clock to Data	2.0	–	–2	5	5	5	ns
		4.5		0	5	5	5	
		6.0		1	5	5	5	
t_W	Minimum Pulse Width Clear or Clock	2.0	–	22	80	100	120	ns
		4.5		11	16	20	24	
		6.0		10	14	18	20	
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	2.0	–	–	75	95	110	ns
		4.5		–	15	19	22	
		6.0		–	13	16	19	
t_r, t_f	Maximum Input Rise and Fall Time	2.0	–	–	1000	1000	1000	ns
		4.5		–	500	500	500	
		6.0		–	400	400	400	
C_{PD}	Power Dissipation Capacitance (Note 4)	5.0	(per package)	150	–	–	–	pF
C_{IN}	Maximum Input Capacitance	–		5	10	10	10	pF

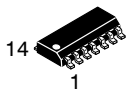
3. C_{PD} determines the no load dynamic power consumption, $PD = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

Product Number	Package	Shipping†
MM74HC164M	SOIC–14 NB (Pb–Free)	55 Units / Tube
MM74HC164MTCX	TSSOP–14 WB (Pb–Free)	2500 / Tape and Reel
MM74HC164MX	SOIC–14 (Pb–Free)	2500 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

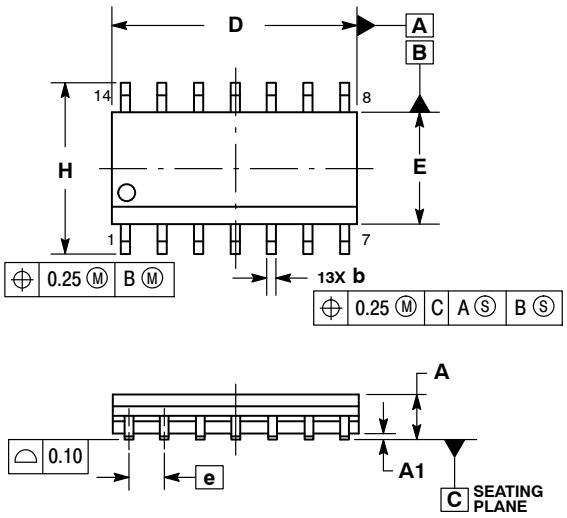
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

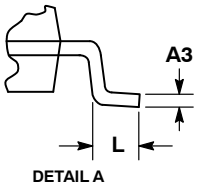


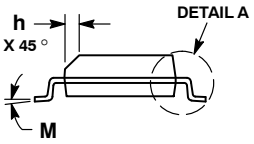
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



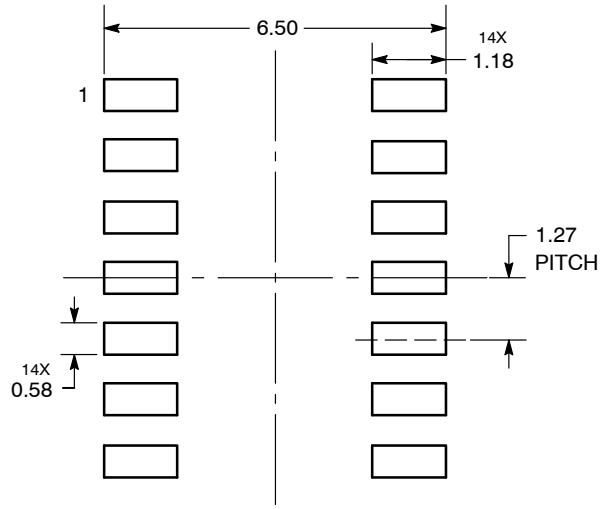




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

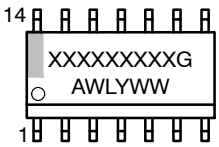
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42565B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOIC−14 NB**	**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

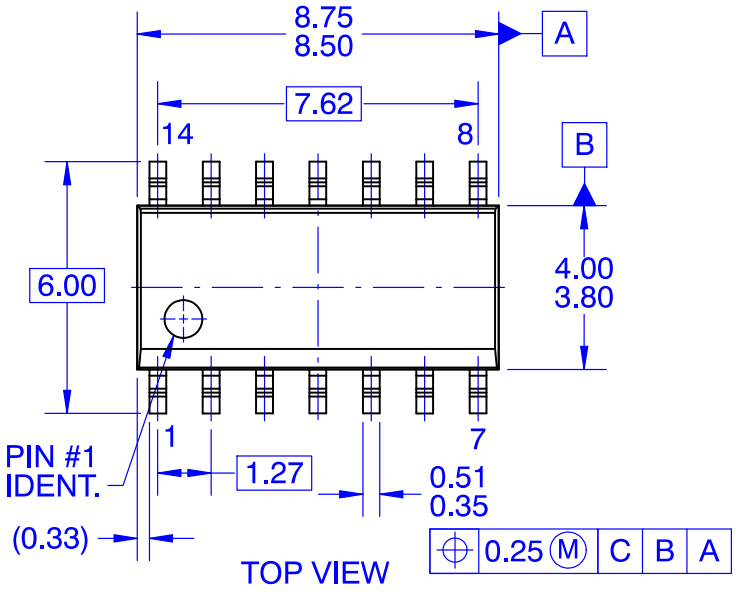
STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

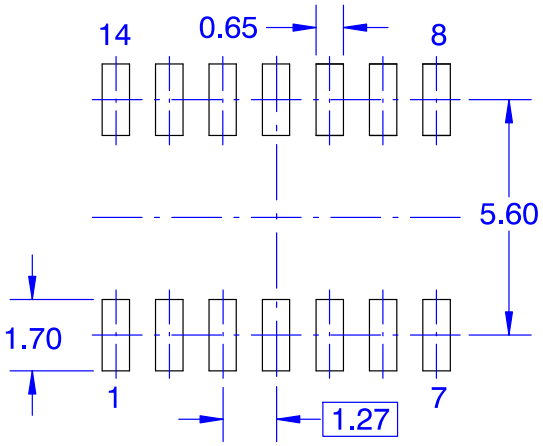
STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

SOIC14
CASE 751EF
ISSUE O

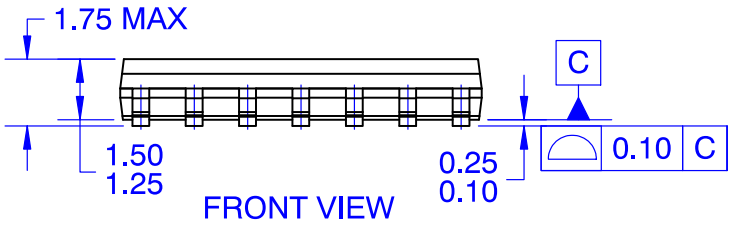
DATE 30 SEP 2016



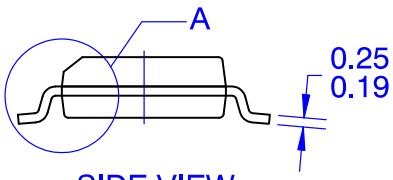
TOP VIEW



LAND PATTERN RECOMMENDATION

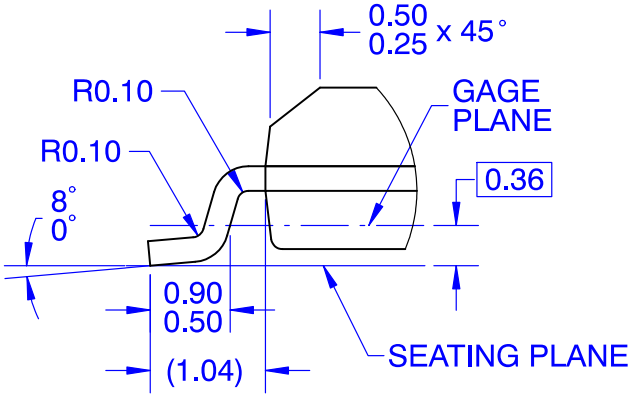


FRONT VIEW



SIDE VIEW

NOTES:
A. CONFORMS TO JEDEC MS–012, VARIATION AB, ISSUE C
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
D. LAND PATTERN STANDARD: SOIC127P600X145–14M
E. CONFORMS TO ASME Y14.5M, 2009



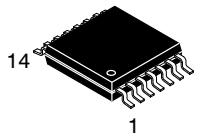
DETAIL A
SCALE 16 : 1

DOCUMENT NUMBER:	**98AON13739G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC14**	**PAGE 1 OF 1**

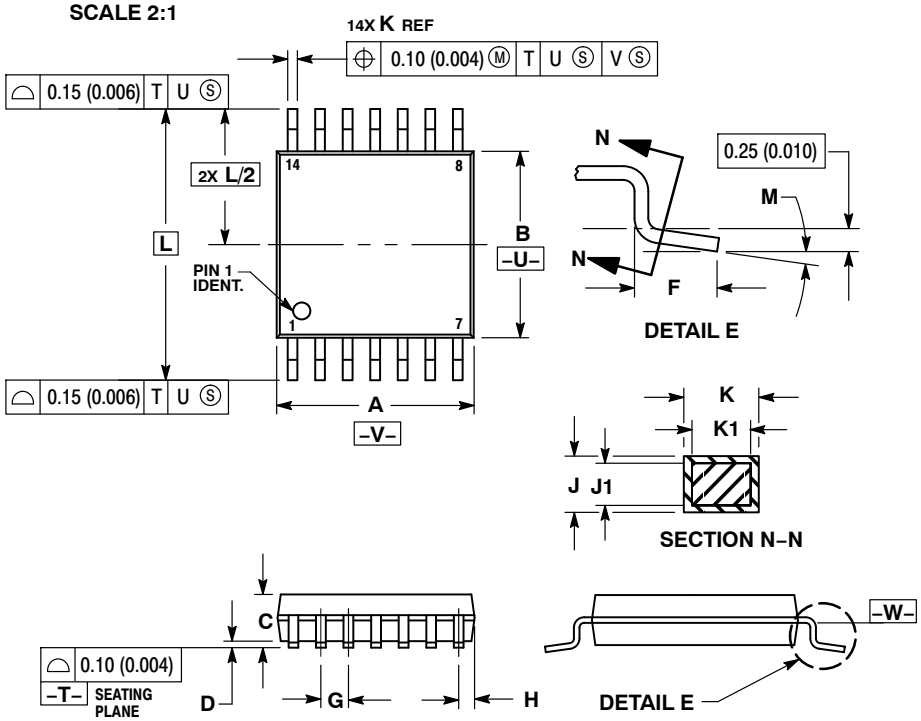
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



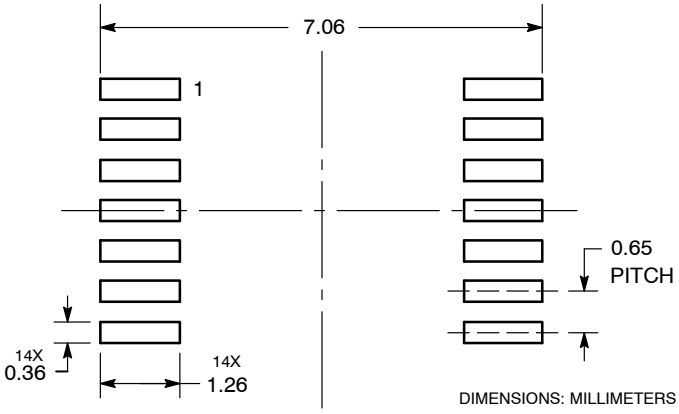
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

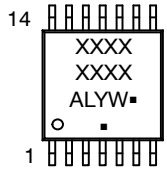
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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