Automotive Two-Channel Linear LED Controller with Internal PWM Dimming

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: September 30, 2024

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to the A6270 and A6270-1.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Allegro MicroSystems reserves the right to make, from time to time, revisions to the anticipated product life cycle plan for a product to accommodate changes in production capabilities, alternative product availabilities, or market demand. The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringements of patents or other rights of third parties which may result from its use.

Downloaded from Arrow.com.

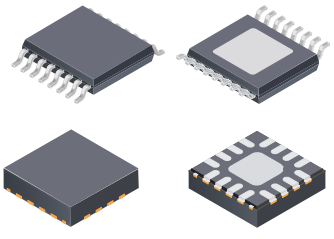
A6272

Automotive Two-Channel Linear LED Controller with Internal PWM Dimming

FEATURES AND BENEFITS

- AEC-Q100 qualified
- 5.3 to 40 V supply; operates down to 5.1 V, when enabled
- LED current programmed independently with two external MOSFETs
- Flexible LED dimming options
  - Integrated PWM dimming set by resistors
  - External PWM dimming set by microcontroller
  - Analog voltage control for PWM dimming
  - Current slew rate limit during PWM dimming
- Adjustable LED current derating for elevated V_{IN}
- LED current derating for elevated junction temperature
- Low regulation voltage for low power dissipation
- Extensive fault detection and protection
  - Drain short-to-ground detection
  - Drain short-to-V_{IN}, LED open, and thermal protection

PACKAGES:



16-pin TSSOP with exposed thermal pad (suffix LP)

16-pin TQFN with wettable flank and exposed thermal pad (suffix ES)

Not to scale

DESCRIPTION

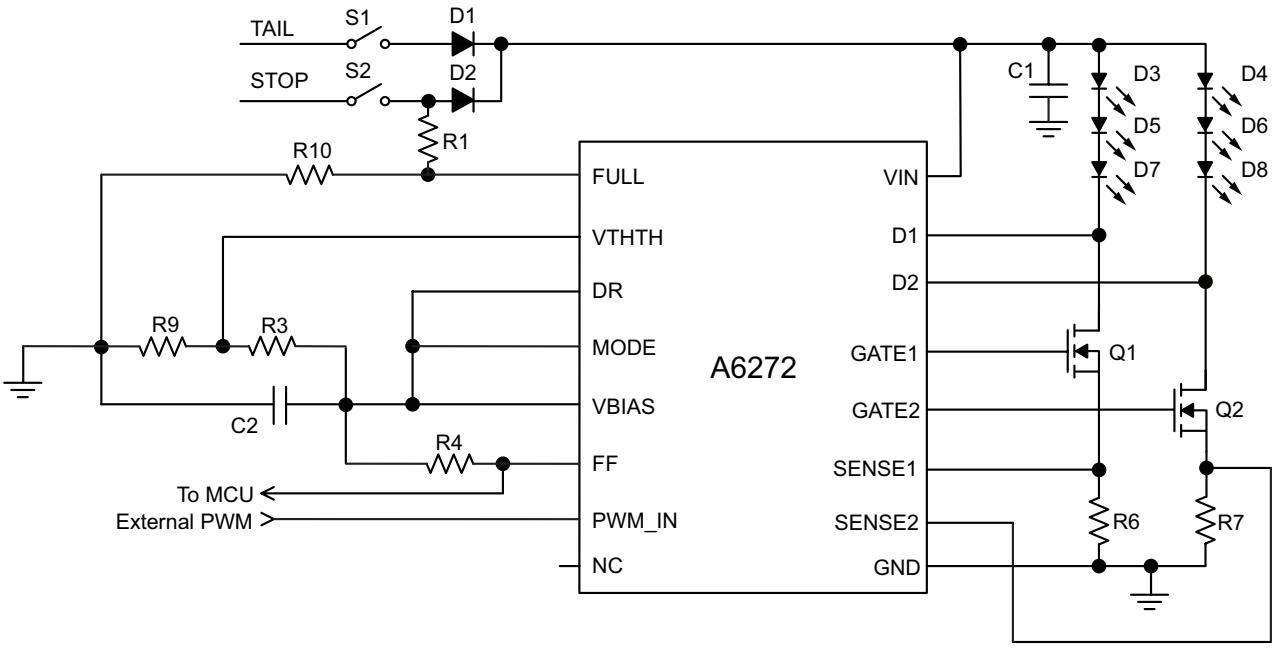
The A6272 is a linear programmable current controller capable of accurately regulating LED current in two strings with external MOSFETs. The LED current can be switched between high current and low current for stop/tail or DRL/position applications. The two LED current levels from each output are set by two sense resistors. Current reference accuracy for each string current is better than ±4%.

Driving LEDs with constant current ensures safe operation with maximum possible light output. ICs can be connected in parallel for larger lighting applications.

Drain short-to-ground detection is provided for both external MOSFETs. A6272 also offers MOSFET drain short-to-V_{IN} and open-LED fault protection. The MODE pin controls the action of the IC in the case of a fault.

A temperature monitor is included to reduce the LED drive current if the chip temperature exceeds a thermal threshold. An input voltage monitor is included to reduce LED current if V_{IN} rises enough to exceed the set level.

The device is available in a 16-pin TSSOP (LP) and a 16-pin wettable flank TQFN (ES), both with exposed pad for enhanced thermal dissipation. Both packages are lead (Pb) free, with 100% matte-tin leadframe plating.



Typical Application Diagram

Downloaded from Arrow.com.

SELECTION GUIDE

Part Number	Packing[1]
A6272KLPTR-T	4000 pieces per reel
A6272KESTR-J[2]	1500 pieces per reel

[1] Contact Allegro™ for additional packing options.
[2] Contact factory.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
VIN, D1, D2 Pins	–		–0.3 to 42	V
FULL Pin	–	Through 10 kΩ resistor	–1 to 42	V
GATE1, GATE2 Pins	–		–0.3 to 10	V
DR Pin	–		–0.3 to V_{VBIAS} + 0.7	V
All Other Pins	–		–0.3 to 7	V
Maximum Continuous Junction Temperature	T_J(max)		150	ºC
Transient Junction Temperature	T_{TJ}		175	ºC
Storage Temperature Range	T_{stg}		–55 to 150	ºC

*With respect to GND.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

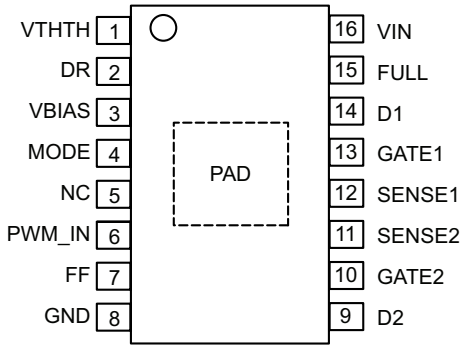
Characteristic	Symbol	Package	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	LP	On 4-layer PCB based on JEDEC standard	34	ºC/W
			On 2-layer PCB with 3.8 in.^{2} copper area each side	43	ºC/W
		ES	On 4-layer PCB based on JEDEC standard	47	ºC/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$			2	ºC/W

*Additional thermal information available on the Allegro website.

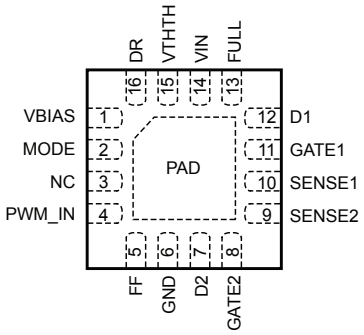
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package LP, 16-Pin TSSOP with Exposed Thermal Pad Pinout Diagram



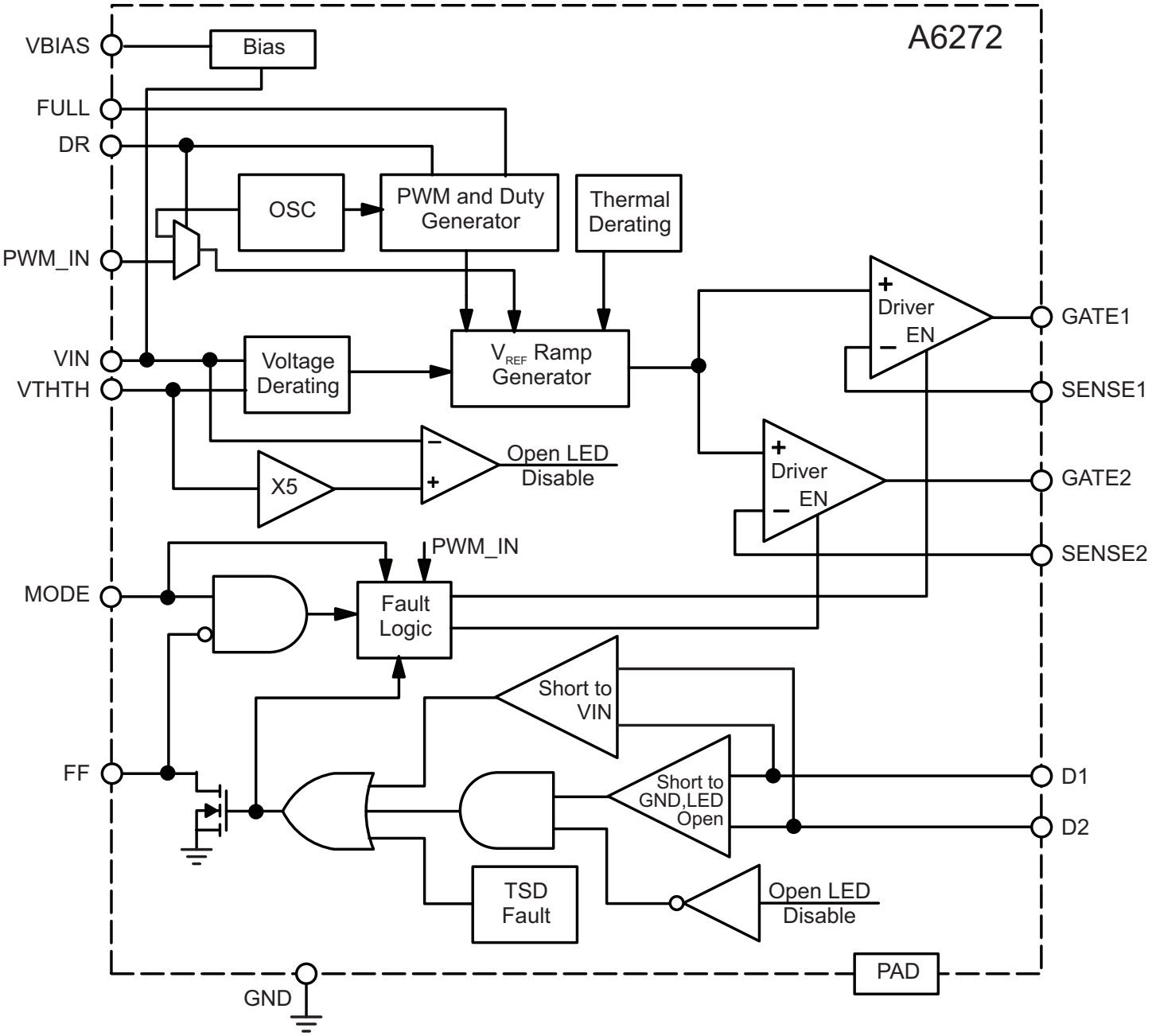
Package ES, 16-Pin TQFN with Exposed Thermal Pad Pinout Diagram

Terminal List Table

Name	Pin Number		Function
	LP Package	ES Package	
D1	14	12	Drain sensing for channel 1 faults: drain short-to-V_{IN}, and LED open- or drain short-to-GND. If this channel is not used, connect the D1 pin to GND through 10 kΩ resistor.
D2	9	7	Drain sensing for channel 2 faults: drain short-to-V_{IN}, and LED open- or drain short-to-GND. If this channel is not used, connect D2 pin to GND through 10 kΩ resistor.
DR	2	16	Connect to external DC voltage to adjust operating duty cycle in internal PWM mode only. In external PWM mode, connect DR pin to VBIAS. When DR connected to VBIAS, PWM duty cycle is controlled by PWM_IN.
FF	7	5	Fault flag output. Also used as fault input when MODE is connected to VBIAS.
FULL	15	13	Full (Stop) mode current-select 100% duty cycle operation. While FULL pin is high, the DR pin, PWM_IN pin, and external PWM information is overridden.
GATE1	13	11	Gate driver for external N-channel MOSFET1.
GATE2	10	8	Gate driver for external N-channel MOSFET2.
GND	8	6	Ground. Connect separate signal and power GND planes to this pin.
MODE	4	2	MODE pin decides the fault mode. Refer to Table 1 for details.
PAD	–	–	Exposed thermal pad. Connect to external ground pad for better thermal performance.
PWM_IN	6	4	In internal PWM mode (DR pin voltage < 3.7 V), PWM frequency is set by a resistor to GND. If DR pin connected to VBIAS, PWM frequency and duty cycle are determined by external signal.
NC	5	3	No connect pin. Connect it to GND or leave it open.
SENSE1	12	10	Current sense for channel 1. Connect sense resistor to set peak current level for channel 1.
SENSE2	11	9	Current sense for channel 2. Connect sense resistor to set peak current level for channel 2.
VBIAS	3	1	Internal bias supply. Connect to GND through a 0.1 μF capacitor.
VIN	16	14	Input supply.
VTHTH	1	15	Voltage at this pin sets the V_{IN} derating threshold and the V_{IN} threshold for open-LED detect fault.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.



Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS: Valid at V_{IN} = 7 to 19 V, • indicates specifications across the full operating temperature range with $T_A = T_J$ = –40ºC to 125ºC; other specifications are at $T_A = T_J$ = 25ºC, unless noted otherwise. Refer to Figure A1 in Application Information section for typical application circuit.

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Supply							
Operating Input Voltage Range	V_{IN}		•	5.3	–	40	V
V_{IN} Operational Current	I_{INQ}	FULL = V_{IHF}	•	–	–	10	mA
Startup Time	t_{ON}	V_{IN} > 7 V, C_{VBIAS} = 0.1 µF, V_{REF} = 20 mV		–	100	–	µs
Current Regulation							
Reference Voltage on SENSE1 and SENSE2	V_{REF}	$V_{VTHTH} = V_{VBIAS}$ (no V_{IN} derating)	•	192	200	208	mV
		$V_{VTHTH} = V_{VBIAS}$ (no V_{IN} derating, T_J = 125°C)		194	200	206	mV
Maximum V_{IN} Derating for Reference Voltage	V_{REF1}	V_{VTHTH} = 2 V, V_{IN} ≥ 26 V		–	50	–	%
Matching Between SENSE1 and SENSE2 Reference[1]	$ErrV_{REF}$	No V_{IN} derating		–	–	2	%
VBIAS Pin Voltage	V_{VBIAS}	I_{VBIAS} = 0 to 3 mA	•	5.15	5.3	5.45	V
VBIAS Undervoltage Release	$V_{VBIASUV}$	V_{IN} rising		–	4.5	–	V
VBIAS Undervoltage Lockout Hysteresis	$V_{VBIASHYS}$	IC disabled		–	0.2	–	V
Gate Driver							
GATE1 and GATE2 High-Level Output	V_{GATEH}	V_{IN} = 12 V, PWM_IN = high, V_{REF} = 150 mV, DR = VBIAS		6	–	9	V
GATE1 and GATE2 Low-Level Output	V_{GATEL}	PWM_IN = low		–	–	0.7	V
GATE Driver Dropout	V_{GATE_drop}	V_{IN} = 7 V, V_{REF} = 150 mV, measured as ($V_{IN} – V_{GATE}$)		–	–	1	V
Gate Pull-Up Current	I_{GPU}	V_{SENSE} = 180 mV, V_{GATE} = 0 V, V_{IN} = 7 V		–	–360	–	µA
Gate Pull-Down Current	I_{GPD}	V_{SENSE} = 220 mV, V_{GATE} = 7 V, V_{IN} = 7 V		–	360	–	µA
External FET Gate Capacitance Range	C_{GISS}	For stable operation		250	–	2000	pF
PWM Dimming Frequency	f_{PWM}	External R_{FPWM} = 30.9 kΩ, across PWM_IN to GND	•	180	200	220	Hz
PWM Duty Cycle[5]	D_{PWML}	V_{DR} driven by resistor divider from VBIAS, V_{VBIAS}/ V_{DR} = 18.7 V/V, f_{PWM} = 200 Hz		7	7.7	8.4	%
	D_{PWMH}	V_{DR} driven by resistor divider from VBIAS, V_{VBIAS}/ V_{DR} = 1.62 V/V, f_{PWM} = 200 Hz		88	90	92	%
Current Slew Time	t_{SR}	Rising or falling between 20% and 90% levels, for internal reference ramp		43	70	97	µs
Rise Time to Fall Time Matching[2]	t_{SRM}	Rising or falling between 20% and 90% levels, for internal reference ramp		–	20	–	µs
Rise Time and Fall Time Mismatch Between Two Strings[3, 4]	t_{SRMS}	Rise and fall time mismatch between 20% and 90% levels in two strings		–	–	2	%

Continued on the next page…

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

ELECTRICAL CHARACTERISTICS (continued): Valid at V_{IN} = 7 to 19 V, • indicates specifications across the full operating temperature range with $T_A = T_J$ = –40ºC to 125ºC; other specifications are at $T_A = T_J$ = 25ºC, unless noted otherwise. Refer to Figure A1 in Application Information section for typical application circuit.

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Logic Pins							
MODE, PWM_IN Pins Input Low Voltage	V_{IL}	Below V_{IL} level, input voltage considered as logic LOW	•	–	–	0.8	V
MODE, PWM_IN Pins Input High Voltage	V_{IH}	Above V_{IH} level, input voltage considered as logic HIGH	•	2	–	–	V
FF Pins Output Low Voltage	V_{OL}	I_{OL} = 1 mA	•	–	–	0.4	V
FULL Pin Input Low Voltage	V_{ILF}	Below V_{ILF} level, input voltage on FULL pin will disable FULL mode	•	0.85	–	1.15	V
FULL Pin Input High Voltage	V_{IHF}	Above V_{IHF} level, input voltage on FULL pin will enable FULL mode	•	1.06	–	1.44	V
MODE Pin Pull-Down Current	I_{Ikg}	MODE connected to VBIAS		–	10	–	μA
Protection							
Input Voltage Required to Derate V_{REF} by 10%	$V_{INth(L)}$	V_{VTHTH} = 2 V		19.7	20.7	21.7	V
VIN Derating Range ($V_{INth(H)}$ to $V_{INth(L)}$)	V_{INthd}	V_{REF} drops from 180 to 120 mV		–	2.16	–	V
VIN-to-Drain Short Detect Voltage	V_{SCV}	Measured as $V_{IN} – V_{Dx}$, GATEx = high	•	0.5	0.8	1.1	V
Open-LED Fault Detect Voltage	V_{OLED}	Measured at Dx, GATEx = low, $V_{IN} > V_{OLED_dis}$	•	0.19	0.24	0.29	V
Open-LED Disable Voltage	V_{OLED_dis}	V_{VTHTH} = 2 V		–	10	–	V
Thermal Monitor Activation Temperature[4]	T_{JM}	T_J with I_{SENSEx}, V_{REF} = 180 mV		–	T_{JF} – 21	–	°C
Thermal Monitor Low-Current Temperature[4]	T_{JL}	T_J with I_{SENSEx}, V_{REF} = 70 mV		–	T_{JF} – 7	–	°C
Overtemperature Shutdown[4]	T_{JF}	Temperature increasing		–	170	–	°C
Overtemperature Hysteresis[4]	T_{Jhys}	Recovery = $T_{JF} – T_{Jhys}$		–	30	–	°C

[1] Reference matching is defined as: $(V_{SENSE1} – V_{SENSE2}) / V_{SENSE(AVG)}$, where $V_{SENSE(AVG)}$ is the average of V_{SENSE1} and V_{SENSE2}.
[2] Rise Time to Fall Time Matching is defined as the maximum difference between the rise time and the fall time of the same string.
[3] Rise Time to Fall Time Mismatch Between Two Strings is defined as the maximum ratio of the difference between either the rise time or the fall time to the average of the rise time or fall times between two strings.
[4] Ensured by design and characterization.
[5] Measured at 50% level of LED current.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

FUNCTIONAL DESCRIPTION

Protection Functions

Various short-circuit faults handled by the A6272 are shown in Figure 1.

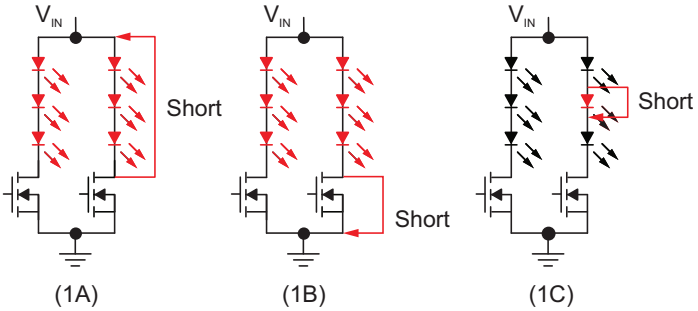


Figure 1: Short-Circuit Protection

For the fault description below, it is assumed (for a simpler explanation) that the fault is applied on the D2 string and the D1 string is assumed to be a healthy string. The IC will respond similarly in the case of a fault on D1.

DRAIN SHORT-TO-V_{IN} (FIGURE 1A, FIGURE 2A, AND FIGURE 2B)

This fault is detected when $V_{IN} - V_{D2} < 0.8$ V and both GATEs are asserted high and after completion of reference ramp. When detected, the FF flag remains low, independent of GATE status. Once the fault detected, GATE2 is pulled high to detect the removal of the fault and restore operation. As the GATE2 remains continuously high, Q2 will dissipate significant power. Current through Q2 is regulated to set level.

When MODE = VBIAS, GATE2 remains high with 100% duty cycle, regardless of FULL or TAIL mode. GATE1 and FF are pulled low once the fault is detected but they are not latched. The IC returns to normal operation (FF = HIGH and GATE1 active) when the fault is removed. As the drain is shorted to V_{IN}, current through LED2 string is zero and GATE1 is pulled low to keep LED1 current low. ICs connected in parallel turn off as FF is pulled low.

When MODE = LOW, both gates switch at 100% duty cycle (FULL mode) or desired PWM duty cycle (TAIL mode). Only

Figure 2A: Drain Short-to-V_{IN} Fault on D2 with MODE = HIGH and PWM Dimming
C4: 5 V/div; C2-C3: 200 mV/div; M1, M3 & M4: 5 V/div; Time: 5 ms/div.

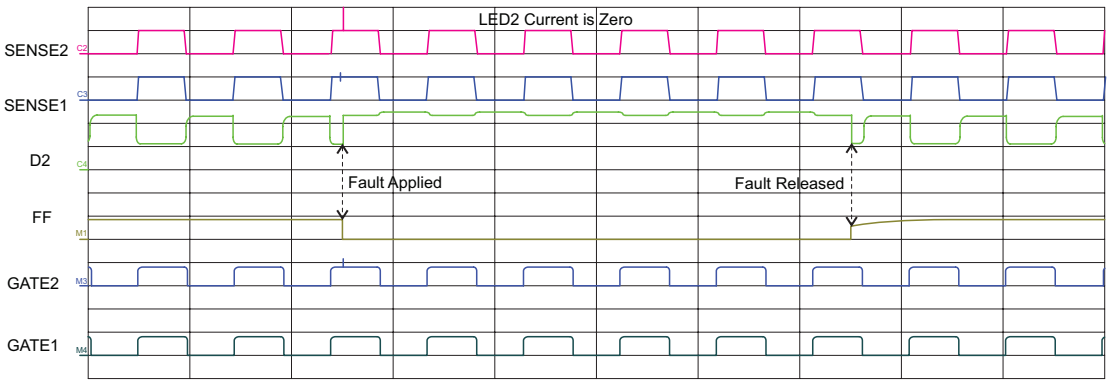


Figure 2B: Drain Short-to-V_{IN} Fault on D2 with MODE = LOW and PWM Dimming
C4: 5 V/div; C2-C3: 200 mV/div; M1, M3 & M4: 5 V/div; Time: 5 ms/div.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

the FF pin is pulled low continuously. The IC returns to normal operation (FF = HIGH) when the fault is removed and GATE2 is asserted high. In this mode, the IC will operate normally except the FF pin is pulled low. The current in the LED1 string and the current in parallel-connected ICs will be normal. The current in the LED2 string is zero as D2 is shorted to V_{IN}. The FF pin does not affect the operation of parallel-connected ICs.

The symmetrical action applies if the fault is in string 1 (i.e., $V_{IN} - V_{D1} < 0.8$ V).

OPEN LED (FIGURE 3, FIGURE 4A, AND FIGURE 4B)

This fault is detected when $V_{IN} > V_{OLED_dis}$ and $V_{D2} < 0.24$ V.

When MODE = VBIAS, GATE2 remains on with 100% duty cycle, regardless of FULL or TAIL mode. GATE1 and FF are pulled low once the fault is detected, but they are not latched. The IC returns to normal operation (FF = HIGH and GATEs active) when the fault is removed.

As the LED2 string is open, current through the LED2 string is zero and GATE1 is pulled low to keep LED1 current off. Parallel-connected ICs turn off the LED string current as FF is pulled low.

When MODE = LOW, both gates run at 100% duty cycle (FULL mode) or desired PWM duty cycle (TAIL mode). Only the FF pin is pulled low as long as $V_{D2} < 0.24$ V. The IC returns to normal

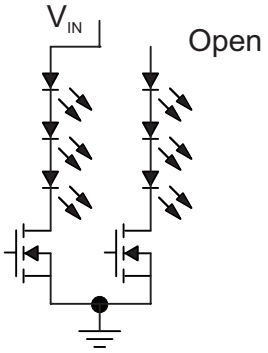


Figure 3: Open-LED Protection

Figure 4A: Open-LED Fault on D2 with MODE = HIGH and PWM Dimming
C4: 5 V/div; C2-C3: 200 mV/div; M1, M3 & M4: 5 V/div; Time: 5 ms/div.

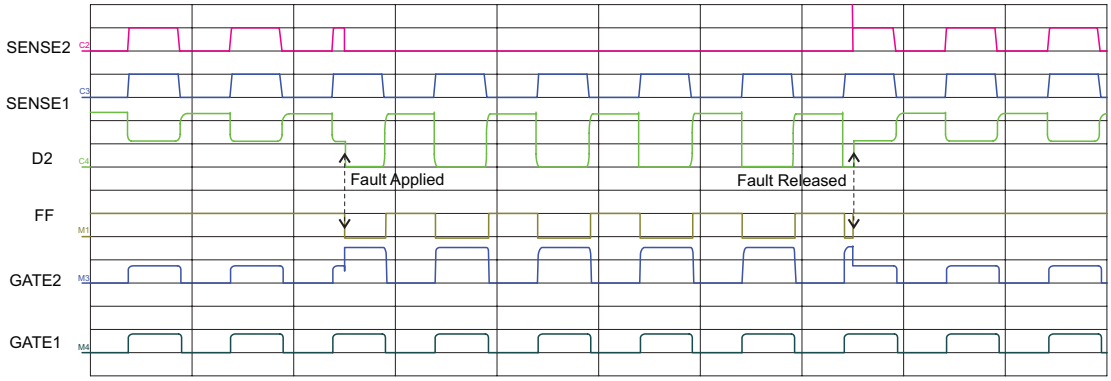


Figure 4B: Open-LED Fault on D2 with MODE = LOW and PWM Dimming
C4: 5 V/div; C2-C3: 200 mV/div; M1, M3 & M4: 5 V/div; Time: 5 ms/div.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

operation (FF = HIGH) when the fault is removed. In this mode, the IC will operate normally except the FF pin is pulled low. LED1 and current in parallel-connected ICs will be normal. Current in the LED2 string is zero as the LED2 string is open. The FF pin does not affect the operation of parallel-connected ICs.

The symmetrical action applies if the fault is in string 1 (i.e., $V_{IN} > V_{OLED_dis}$ and $V_{D1} < 0.24$ V).

DRAIN SHORT-TO-GND (FIGURE 1B, FIGURE 5, AND FIGURE 6)

This fault is detected when $V_{IN} > V_{OLED_dis}$ and $V_{Dx} < 0.24$ V (same as open-LED fault).

When MODE = VBIAS, GATE2 remains on with 100% duty cycle, regardless of FULL or TAIL mode. GATE1 and FF are pulled low once the fault is detected, but they are not latched. The IC returns to normal operation (FF = HIGH and GATEs active) when the fault is removed.

As the LED2 string is shorted to GND, a large current will flow through the LED2 string. GATE1 will be pulled low to keep LED1 current off. Parallel-connected ICs turn the LED string current off as FF is pulled low.

When MODE = LOW, both gates run at 100% duty cycle (FULL mode) or desired PWM duty cycle (TAIL mode). Only the FF pin is pulled low as long as $V_{D2} < 0.24$ V. The IC returns to normal operation (FF = HIGH) when the fault is removed. In this mode, the IC will operate normally except the FF pin is pulled low. The current in LED1 and the current in parallel-connected ICs will be normal. As the LED2 string is shorted to GND, a large current will flow through the LED2 string. The FF pin does not affect the operation of parallel-connected ICs.

The symmetrical action applies if the fault is in string 1 (i.e., $V_{IN} > V_{OLED_dis}$ and $V_{D1} < 0.24$ V).

SINGLE LED SHORT (FIGURE 1C)

In the case where a few LEDs are shorted, the IC continues to work normally.

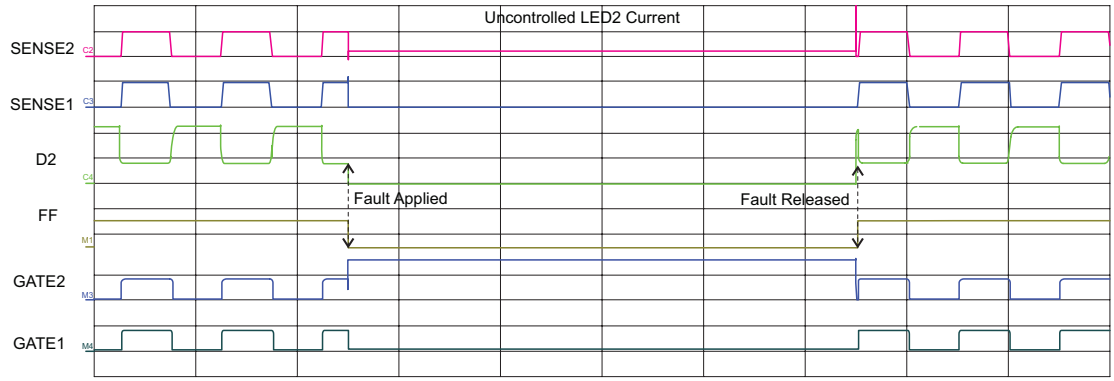


Figure 5: Drain Short-to-GND Fault on D2 with MODE = HIGH and PWM Dimming

C4: 5 V/div; C2-C3: 200 mV/div; M1, M3 & M4: 5 V/div; Time: 5 ms/div.

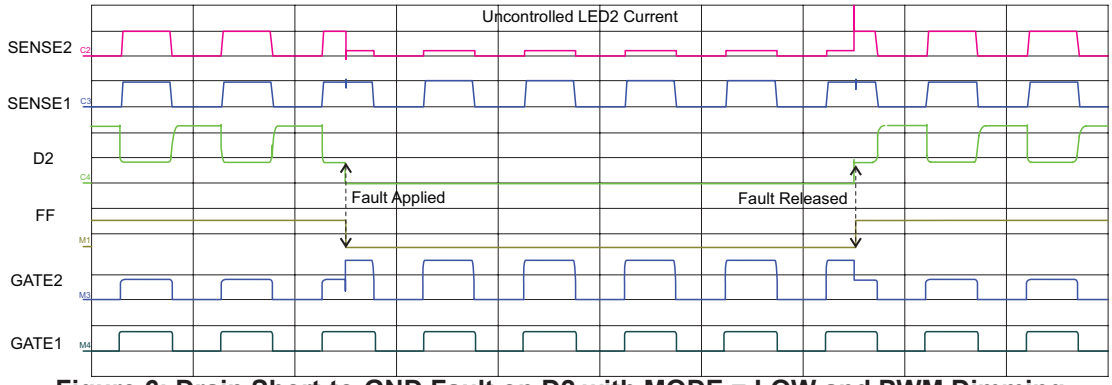


Figure 6: Drain Short-to-GND Fault on D2 with MODE = LOW and PWM Dimming

C4: 5 V/div; C2-C3: 200 mV/div; M1, M3 & M4: 5 V/div; Time: 5 ms/div.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

OPEN-LED DISABLE THRESHOLD

When input voltage, V_{IN}, is below V_{OLED_dis}, defined by voltage on the VTHTH pin, drain short-to-GND and open-LED faults are disabled. Select a V_{OLED_dis} level higher than the LED forward voltage. The IC will continue to operate normally in cases where these faults exist. V_{OLED_dis} value is given by:

$$V_{OLED_dis} = 5 \times V_{VTHTH} \qquad (1)$$

Voltage on VTHTH sets the input voltage derating threshold ($V_{INth(L)}$) as well as the open-LED disable level (V_{OLED_dis}). Select a VTHTH voltage suitable to avoid an open-LED fault due to insufficient input voltage. This also sets $V_{INth(L)}$.

INPUT OVERVOLTAGE DERATING

This feature takes effect at higher V_{IN} levels, limiting power dissipation in the external MOSFETs. At higher input voltages, output current drops, corresponding with increasing V_{IN}. Output current is controlled with peak current (see Figure 8). The V_{IN} threshold can be set with an external resistor divider from VBIAS connected to VTHTH. The reference voltage drops to 90% at the $V_{INth(L)}$ level and to 60% at $V_{INth(H)}$ level. Reference level drops to 50% and stays at this level for higher input voltages. Voltage on the VTHTH pin sets the $V_{INth(L)}$ level, and the $V_{INth(H)}$ level is typically higher than $V_{INth(L)}$ by V_{INthd} (2.16 V). The range for $V_{INth(L)}$ is from 16 to 36 V, determined by:

$$V_{INth(L)} = 10 \times V_{VTHTH} + 0.7\ V \qquad (2)$$

where $V_{INth(L)}$ is the supply voltage level where V_{REF} drops to the 90% level, and V_{VTHTH} is the voltage on VTHTH pin. Figure 7 shows the relationship between voltage on the VTHTH pin and $V_{INth(L)}$.

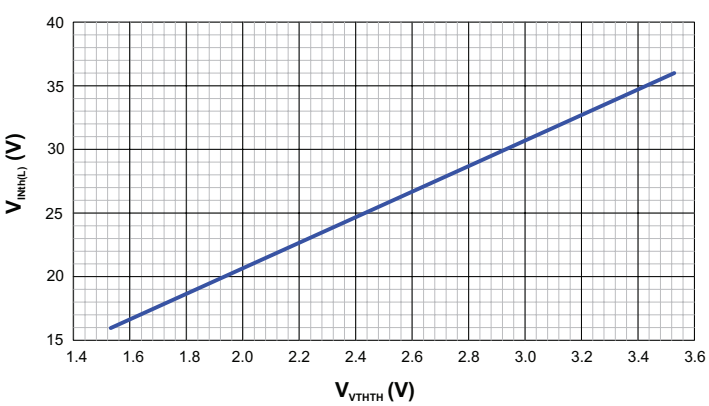


Figure 7: VTHTH Voltage versus V_{IN} Derating Threshold

THERMAL DERATING AND PROTECTION SHUTDOWN

This feature takes effect at higher temperatures, limiting power dissipation in the external MOSFETs. At higher temperatures, the reference voltage drops with increasing T_J as shown in Figure 9. Thermal shutdown (TSD) completely disables the outputs under extreme overtemperature (>170°C) conditions, and FF goes low. The IC restarts when the temperature drops by 30°C.

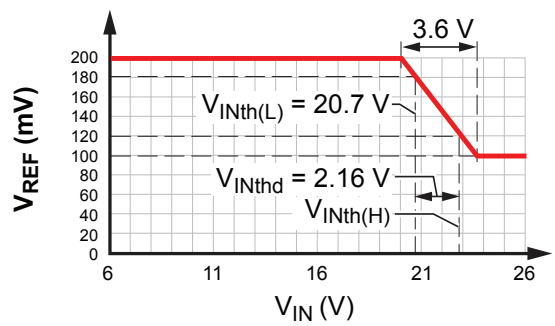


Figure 8: Output Current Foldback Based on V_{IN}

Output current changed by DC current control ($V_{INth(L)}$ determined by voltage on VTHTH pin). V_{REF} drops to the 90% level when V_{IN} exceeds $V_{INth(L)}$, which is 20.7 V when V_{VTHTH} = 2 V.

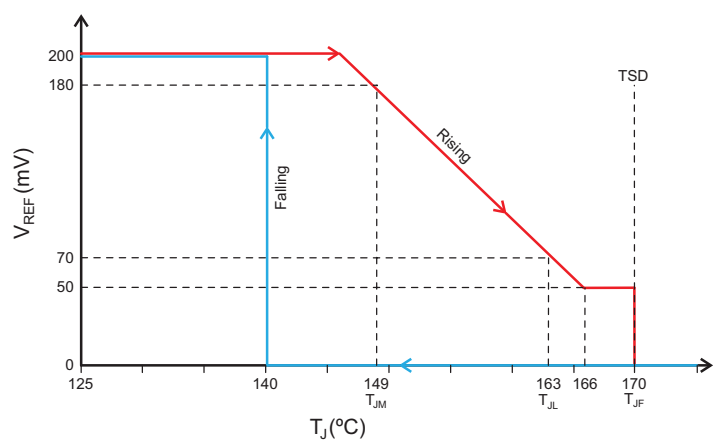


Figure 9: Output Current Foldback Based on Rising T_J

Output current changed by DC current control; when temperature exceeds 170°C (typ), the gates turn off due to TSD function, and turns on again at 140°C (30°C (typ) hysteresis).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

Internal Dimming Frequency and Duty Cycle

Dimming frequency can be set using the PWM_IN pin. This PWM frequency can be set in the range from 200 Hz to 1 kHz, either by using an external resistor, or by using an external clock signal, on the PWM_IN pin. The equation for frequency setting with the PWM_IN pin resistor is as follows:

$$f_{PWM} = 5400 / R_{FPWM} + 25 \qquad (3)$$

where f_{PWM} is in Hz and R_{FPWM} is in kΩ. For example, with a 30.9 kΩ resistor, f_{PWM} = 200 Hz.

When frequency is set through an external resistor (for internal PWM), the voltage on the DR pin determines the operating duty cycle. For better accuracy, derive this voltage from VBIAS using a voltage divider. The PWM duty cycle depends on ratio of the DR and VBIAS pin voltages. The IC works with 100% duty cycle in STOP mode (FULL = HIGH). In TAIL mode, the duty cycle can be programmed by controlling the analog voltage on the DR pin. The duty cycle can be changed from 5% to 90% (see Figure 10), as:

$$PWM\ (\%) = [146 \times (V_{DR} / V_{VBIAS})] - 0.1 \qquad (4)$$

where V_{DR} and V_{VBIAS} are in volts.

If the DR pin is connected to VBIAS, an external clock pulse on the PWM_IN pin controls dimming frequency and duty cycle.

LED CURRENT SETTING

LED peak current (100%) level can be set independently for each channel by selecting a proper resistor value from the SENSEx pin to GND, as follows:

$$LED\ Peak\ Current = 200 / R_{SENSE} \qquad (5)$$

where LED peak current is in mA and R_{SENSE} is in Ω.

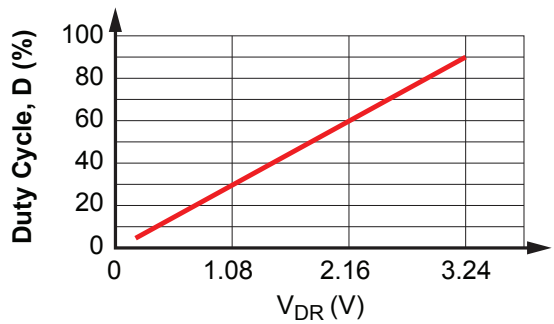


Figure 10: Relationship of External Voltage Input on DR Pin and Dimming Duty Cycle

V_{DR} can be varied from 0 to 3.6 V.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

Table 1: Fault Operation and Derating

	FF	Operation	
		MODE = VBIAS	MODE = LOW
Drain Shorted to V_{IN}	Low	Detected when $V_{IN} – V_{Dx} < 0.8$ V. The faulty string remains on with 100% duty cycle regardless of FULL or TAIL mode. Other string and FF pull low once fault is detected but is not latched. Faulty MOSFET drops full VIN voltage. IC recovers to normal operation when fault removed.	Detected when $V_{IN} – V_{Dx} < 0.8$ V. IC operates normally except FF pin pulled low. Faulty MOSFET drops full VIN voltage when enabled. FF pin goes high when fault is removed.
	Fault is detected when both GATEs are asserted high and after completion of reference ramp. When detected, the fault remains active independent of GATE status.		
Open LED	Low	Detected when $V_{IN} > V_{OLED_dis}$ and $V_{Dx} < 0.24$ V. The faulty string remains on with 100% duty cycle regardless of FULL or TAIL mode. Other GATEx is turned off. IC recovers to normal operation when fault is removed.	Detected when $V_{IN} > V_{OLED_dis}$ and $V_{Dx} < 0.24$ V. IC operates normally except FF pin is pulled low. FF pin goes high when fault is removed.
Drain Shorted to GND	Low	Detected when $V_{IN} > V_{OLED_dis}$ and $V_{Dx} < 0.24$ V. The faulty string remains on with 100% duty cycle regardless of FULL or TAIL mode. Other GATEx is turned off. IC recovers to normal operation when fault is removed. LEDs in faulty string may be damaged due to excessive LED current.	Detected when $V_{IN} > V_{OLED_dis}$ and $V_{Dx} < 0.24$ V. IC operates normally except FF pin pulled low. LEDs in faulty string may be damaged due to excessive LED current. FF pin goes high when fault is removed.
Thermal Derating	Normal	LED current derates based on junction temperature.	Same operation as MODE = VBIAS.
V_{IN} Derating	Normal	LED current derates based on supply voltage and VTHTH setting.	Same operation as MODE = VBIAS.
TSD	Low	LEDs turn off when T_J exceeds 170ºC. Auto-recover when T_J drops below 140ºC.	LEDs turn off when T_J exceeds 170ºC. Auto-recover when T_J drops below 140ºC.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

APPLICATION INFORMATION

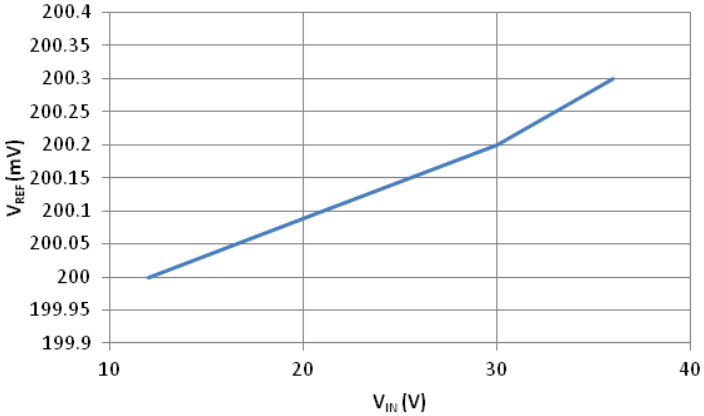


Figure 11: V_{IN} vs. V_{REF} (V_{VTHTH} = 3.6 V)

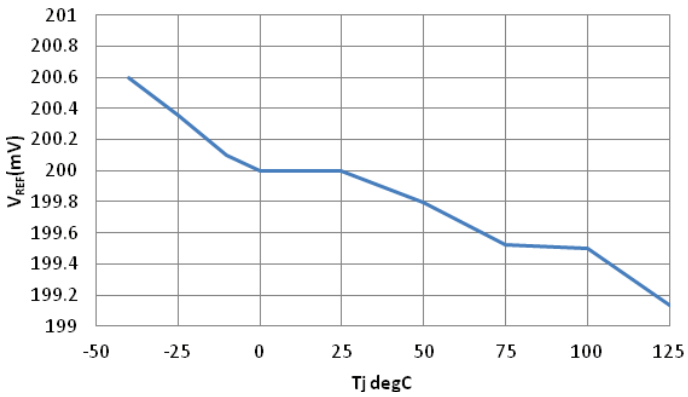


Figure 12: Temperature vs. V_{REF}

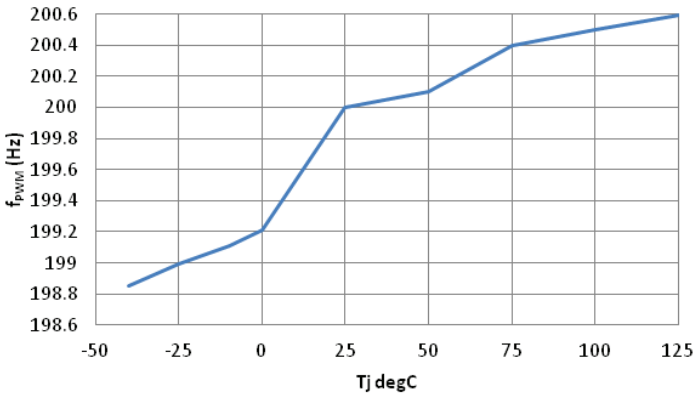


Figure 13: Temperature vs. f_{PWM} (R_{FPWM} = 30.9 kΩ)

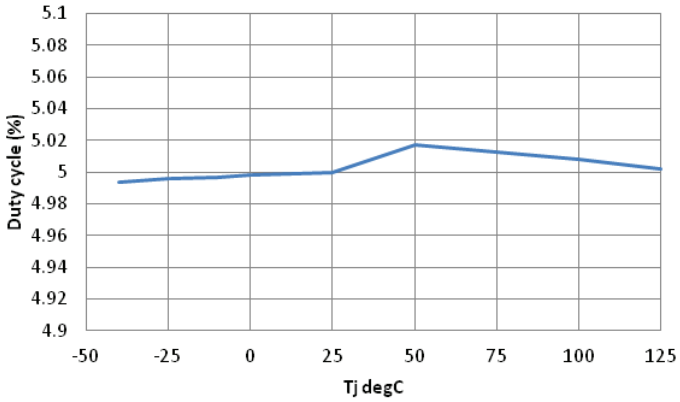


Figure 14: Temperature vs. Duty Cycle (V_{VBIAS}/V_{DR} = 28.6 V/V)

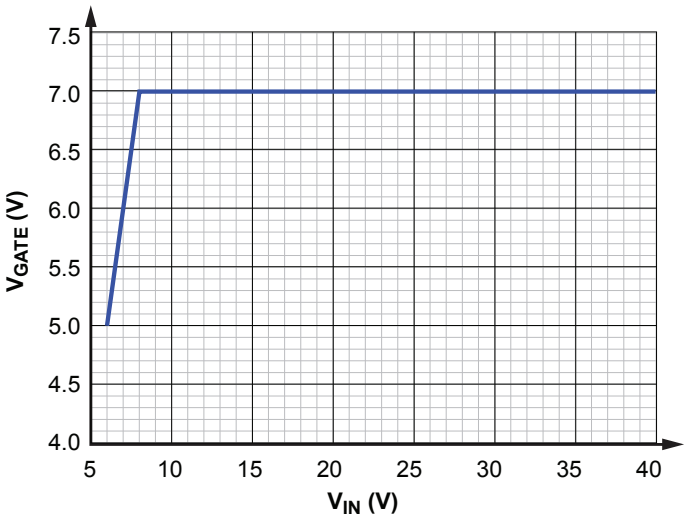


Figure 15: GATE Voltage vs. V_{IN}

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

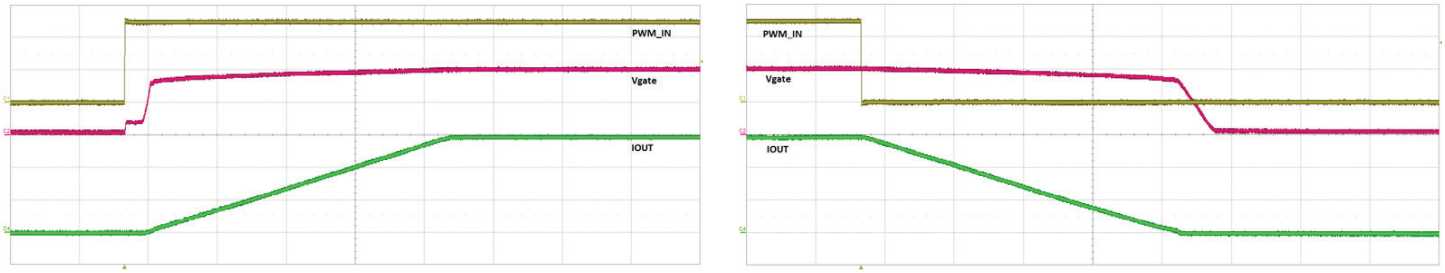


Figure 16: Rise Time and Fall Time During PWM Dimming.
I_{OUT} (Total LED Current) (200 mA/div), PWM_IN and V_{GATE} (2 V/div), Time (20 µs/div)

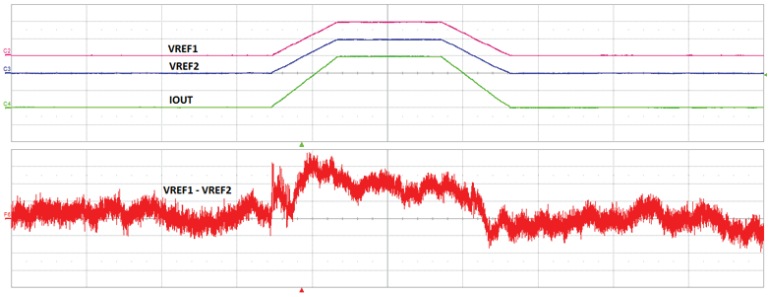


Figure 17: Reference Matching During PWM Dimming
V_{REF1}, V_{REF2} (100 mV/div), I_{OUT} (Total LED Current)(200 mA/div), V_{REF1}-V_{REF2} (2 mV/div), Time (100 µs/div).

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

Modes of Operation

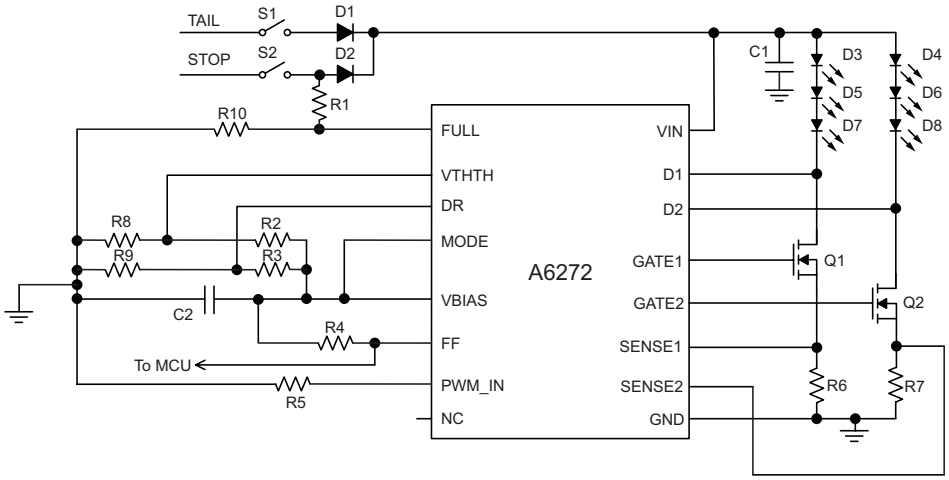
The IC can operate in one of the following modes:

A. Single IC, internal PWM mode
B. Single IC, external PWM mode
C. Multiple ICs, in parallel mode

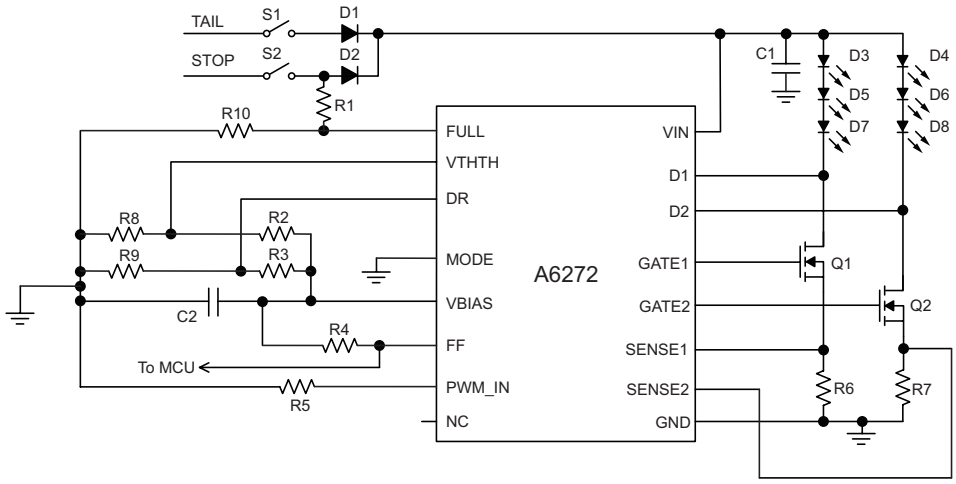
These are each described in the remainder of this section.

A. SINGLE IC, INTERNAL PWM MODE

In TAIL mode, the IC generates its PWM frequency based on a resistor connected from the PWM_IN pin to GND, and the duty cycle is controlled by voltage at the DR pin (which can be generated by a resistor divider, or driven by an external DC signal). In FULL (STOP) mode, the duty cycle is always 100%. Overtemperature or input overvoltage conditions derate LED current by controlling peak current in both STOP and TAIL modes. Voltage on the VTHTH pin controls the input voltage derating threshold.



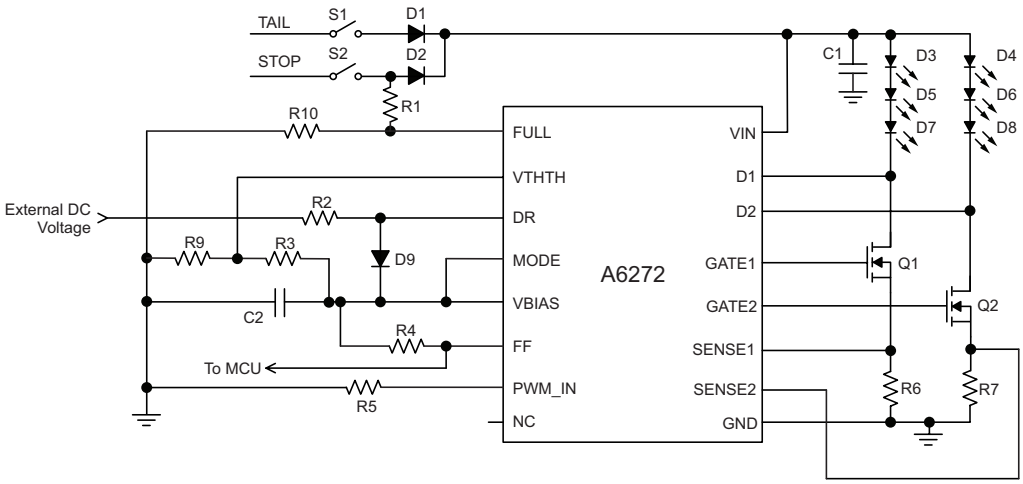
Typical Application Circuit A1: Single IC Operation with Internal Reference to DR and MODE Pulled High.



Typical Application Circuit A2: Single IC Operation with Internal Reference to DR and MODE Shorted to GND.

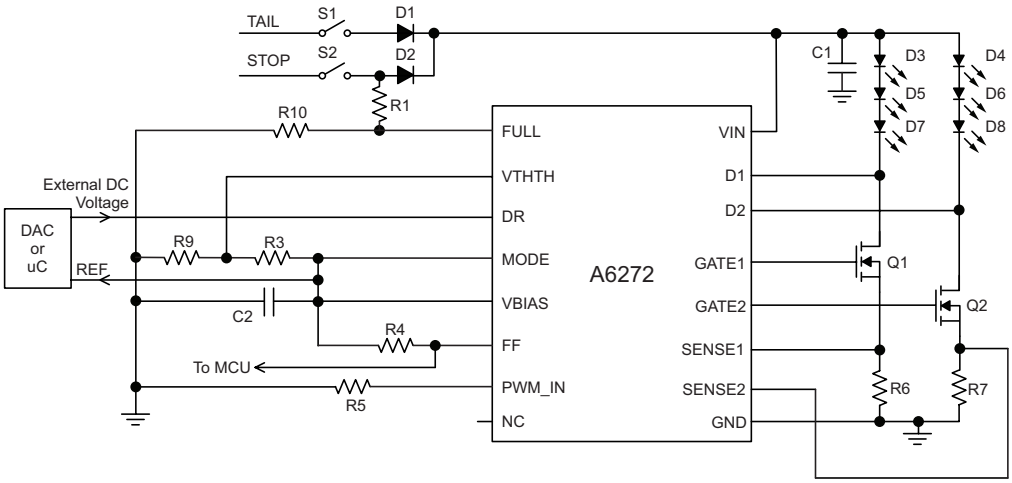
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.



Typical Application Circuit A3a: Single IC Operation with External Analog Reference to DR and MODE Pulled High

External DC voltage can be applied on DR pin to control PWM dimming. Voltage on DR pin should be $0 < V_{DR} < 3.6$ V for duty cycle control. Voltage on DR pin must be lower than V_{VBIAS} under all conditions. Optional R2-D9 clamp used to ensure DR pin voltage limited to V_{VBIAS}.



Typical Application Circuit A3b: Using DAC to Microcontroller to Control PWM Duty Cycle

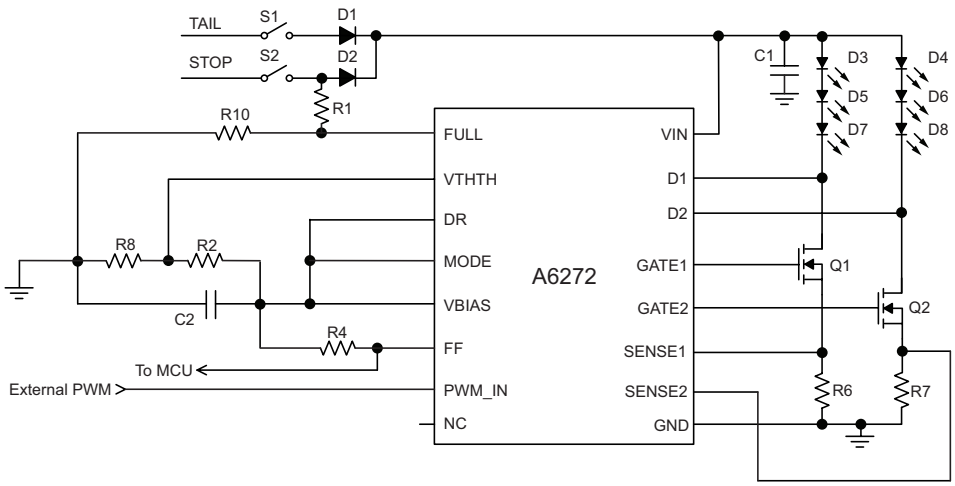
The PWM duty cycle is ratiometric to V_{VBIAS}. Using VBIAS as reference to DAC improves accuracy with external DC voltage. DR pin voltage should be lower than V_{VBIAS} under all conditions. Apply voltage on DR pin after VBIAS powers up.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

B. SINGLE IC, EXTERNAL PWM MODE

When the DR pin is connected to VBIAS, in TAIL mode, the IC disables internal PWM generation and replicates the frequency and duty cycle of the signal at the PWM_IN pin onto GATEx. In FULL mode, the duty cycle is always 100%. Overtemperature or input overvoltage conditions derate LED current by controlling peak current in both STOP and TAIL modes. Voltage on the VTHTH pin controls the input voltage derating threshold.



Typical Application Circuit B1: Single IC Operation with External PWM to PWM_IN Pin and MODE Pulled High.
For the above configuration, DR pin voltage is always connected to the VBIAS pin.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

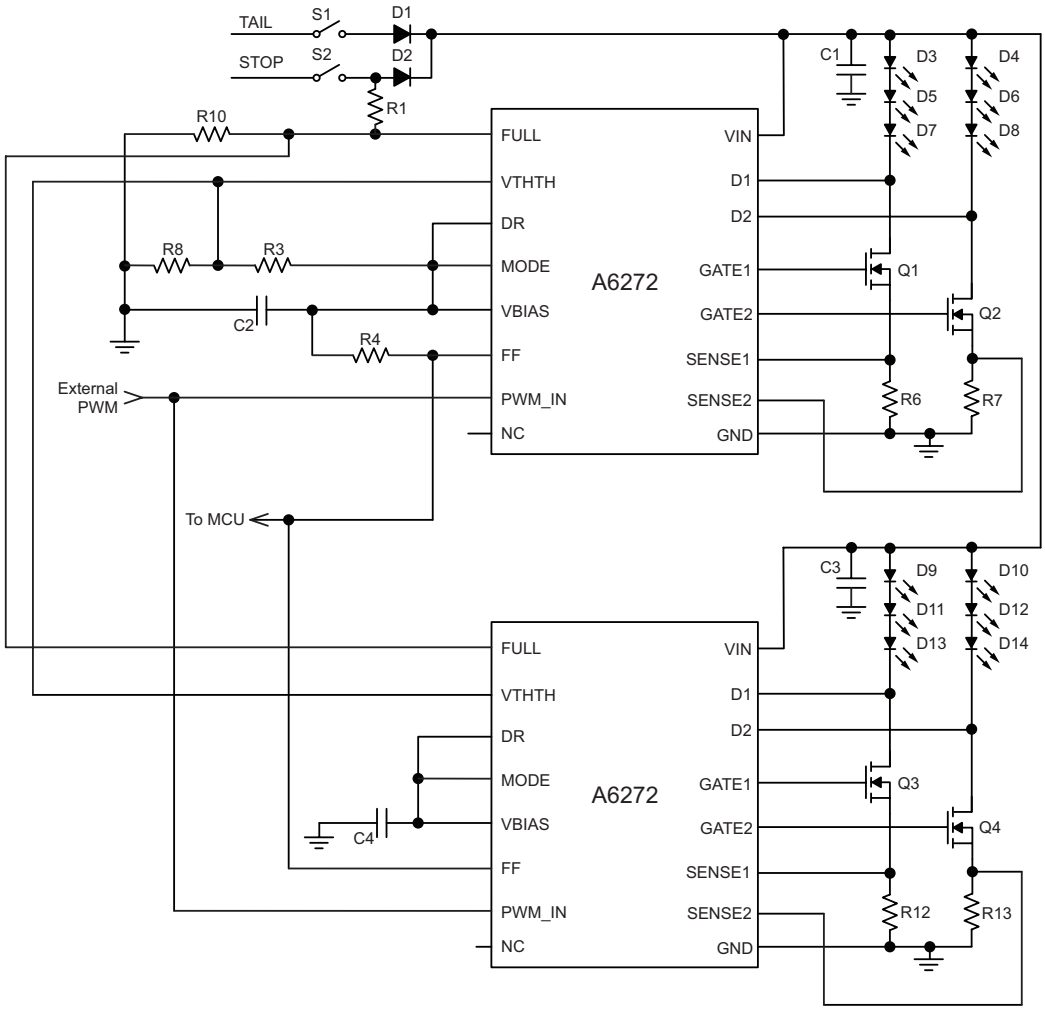
Downloaded from Arrow.com.

C. MULTIPLE ICS, IN PARALLEL MODE

All the ICs are configured for external PWM mode. PWM input from the MCU controls frequency and duty cycle in TAIL mode.

In STOP mode, duty cycle is always 100%.

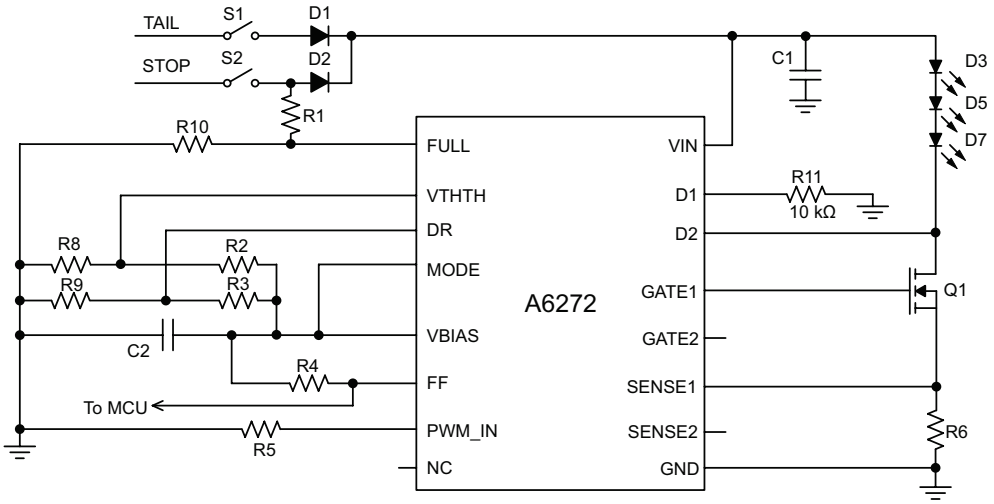
Each IC derates LED current independently, based on VIN pin voltage and junction temperature of the respective IC.



Typical Application Circuit C1: Parallel Operation with External PWM and MODE Pulled High

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

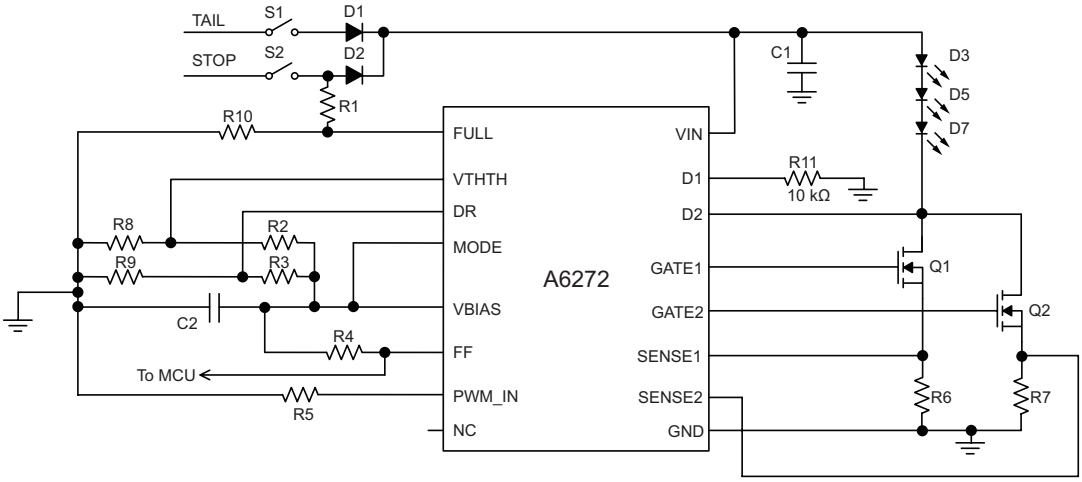
Downloaded from Arrow.com.



Typical Application Circuit D1: Single LED String Driven by a MOSFET (MODE = HIGH).

Connect unused Dx pin to GND through 10 kΩ resistor.

Keep unused GATEx and SENSEx pins open.



Typical Application Circuit E1: Single LED String Driven by Two MOSFETs for Higher Current Applications (MODE = HIGH).

Drains of Q1 and Q2 can be connected together for driving single high-current LED string. To avoid interaction of fault sensing on D1 and D2, connect one of Dx pin to GND through 10 kΩ resistor.

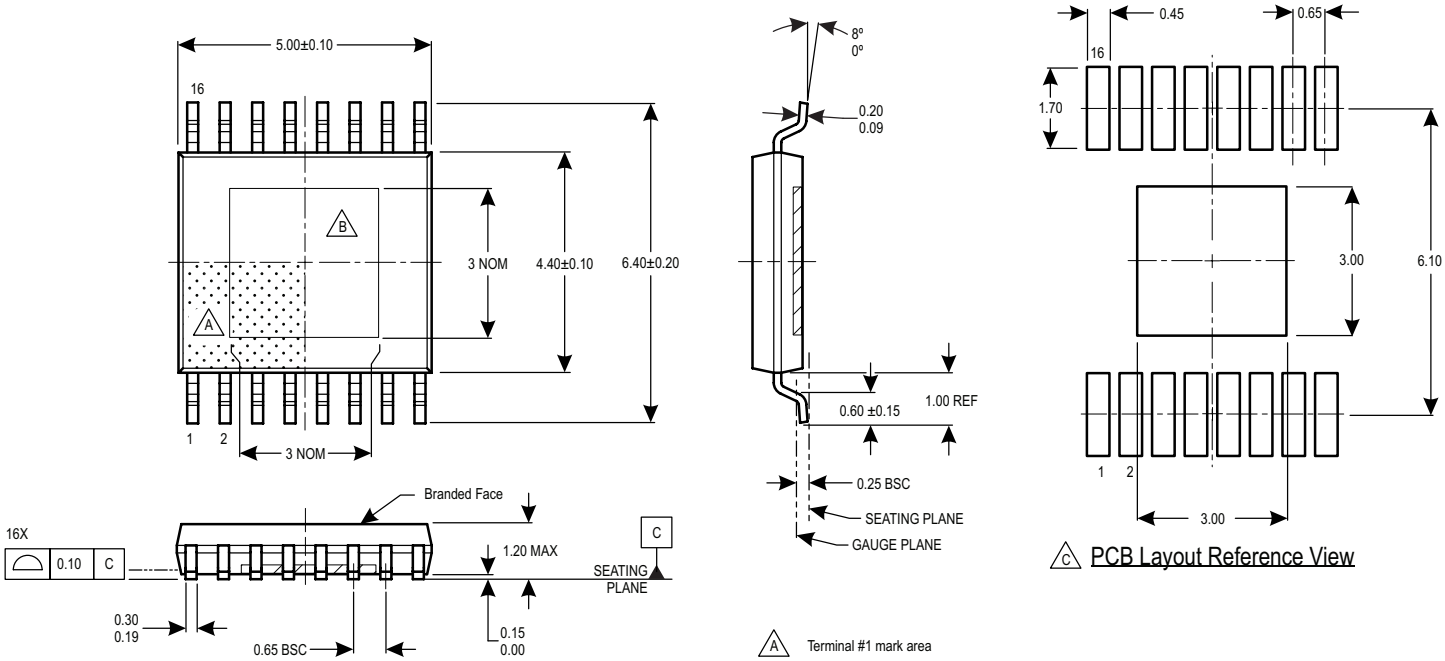
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference MO-153 ABT)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Figure 18: Package LP, 16-Pin TSSOP with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

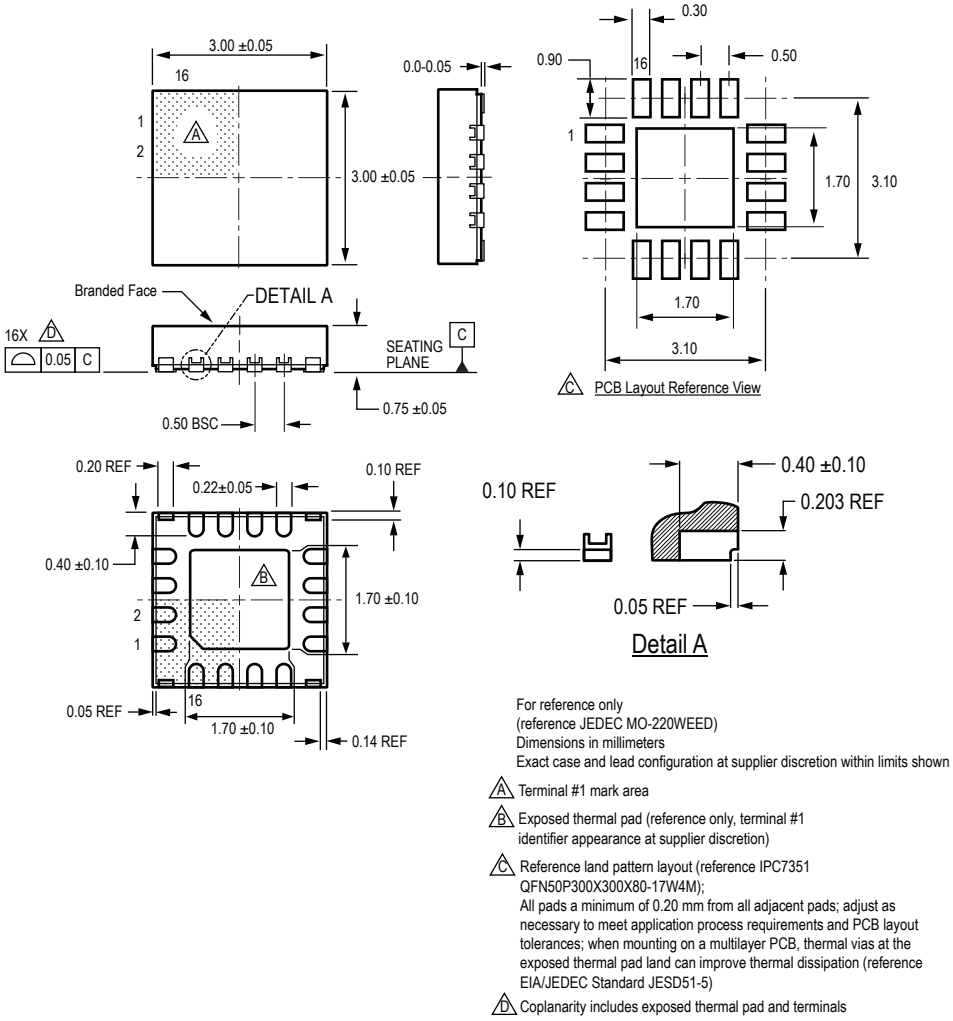


Figure 19: Package ES, 16-Pin TQFN with Exposed Thermal Pad and Wettable Flank

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.

Revision History

Revision	Revision Date	Description of Revision
–	June 1, 2016	Initial release
1	January 29, 2019	Product status updated to Not for New Design
2	February 20, 2020	Minor editorial updates
3	March 22, 2024	Product status updated to Last-Time Buy
4	September 12, 2024	Product status updated to Discontinued
5	October 3, 2025	Administrative correction for document control (content not modified)

Copyright 2025, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:

www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Downloaded from Arrow.com.