High Bandwidth, 6-Differential Channel 1:2 DP/PCIe Gen2 Display Mux, ATX Pinout

Features

- 6 Differential Channel, 1 to 2 demux that will support 5.0Gbps PCIexpress Gen2 signals on one path, and DP 1.1 signals on the second path
- Insertion Loss for high speed channels @ 5.0 Gbps: -5.0dB
- Low Bit-to-Bit Skew , 7ps max (between '+' and '-' bits)
- Latched Mux Select
- Matched paths for all PCIe signals
- Low Crosstalk for high speed channels: -35dB@2.5 GHz
- Low Off Isolation for high speed channels: -35dB@2.5 GHz
- V_{DD} Operating Range: 3.3V ± 10%
- ESD Tolerance: 8kV HBM on Display Port Path output
  3kV HBM on PCI-Express path output
- Low channel-to-channel skew, 35ps max
- Packaging (Pb-free & Green):
  – 56 TQFN (ZFE)

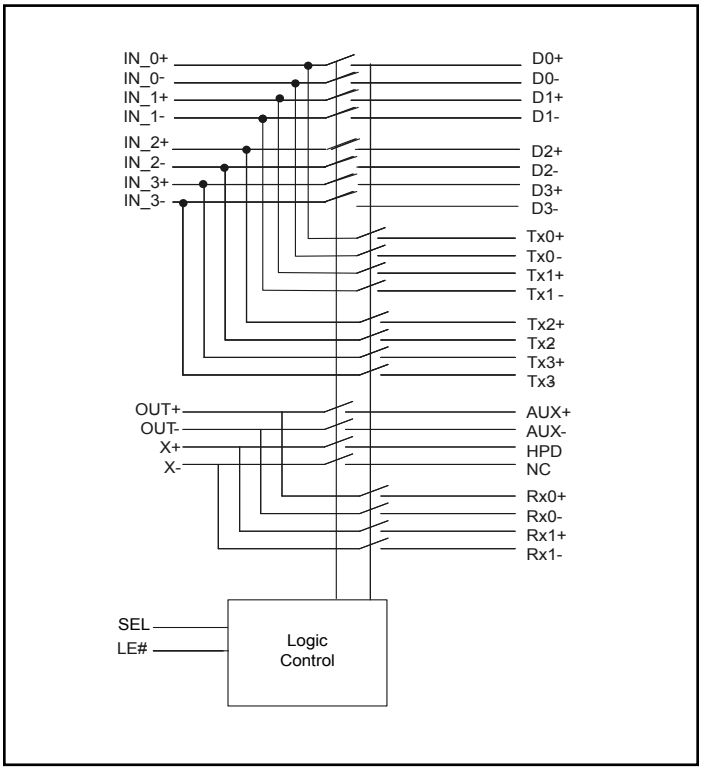
Description

Pericom Semiconductor's PI3PCIE2612-A one to two Mux/ Demux is targeted for next generation systems that combine PCI-Express gen-II signals with Display Port Signals.

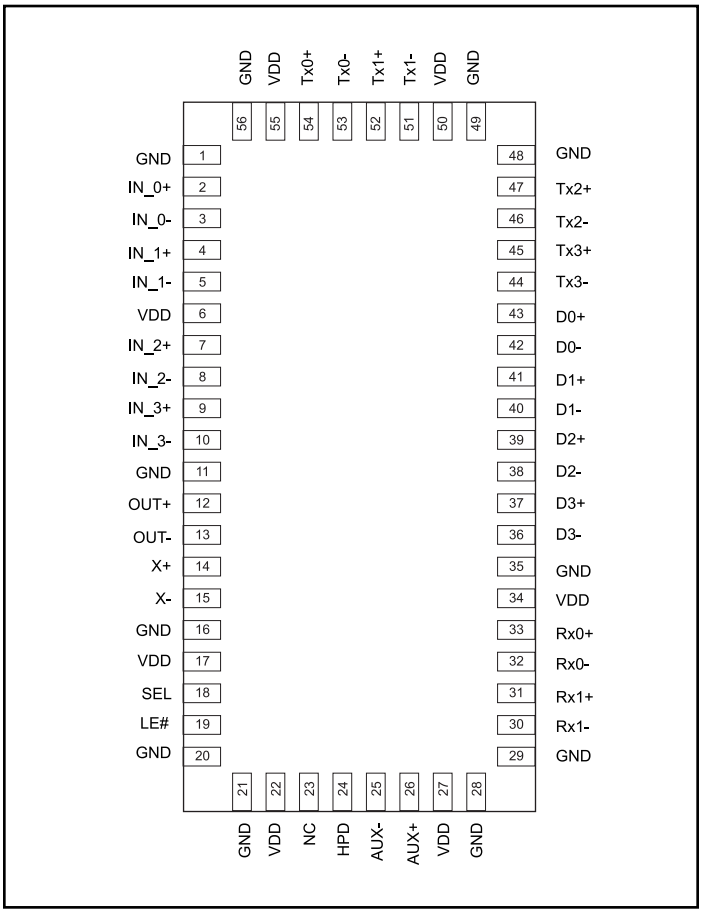
Application

Routing DP and PCIExpress Gen1 or Gen2 signals with low signal attenuation.

Block Diagram



Pin Diagram (top-side view)



Truth Table (SEL control)

Function	SEL
PCI-Express Gen2 path is active (Tx)	L
Digital Video Port is active (Dx)	H

Truth Table (Latch control)

LE#	Internal mux select
0	Respond to changes on SEL
1	Latched

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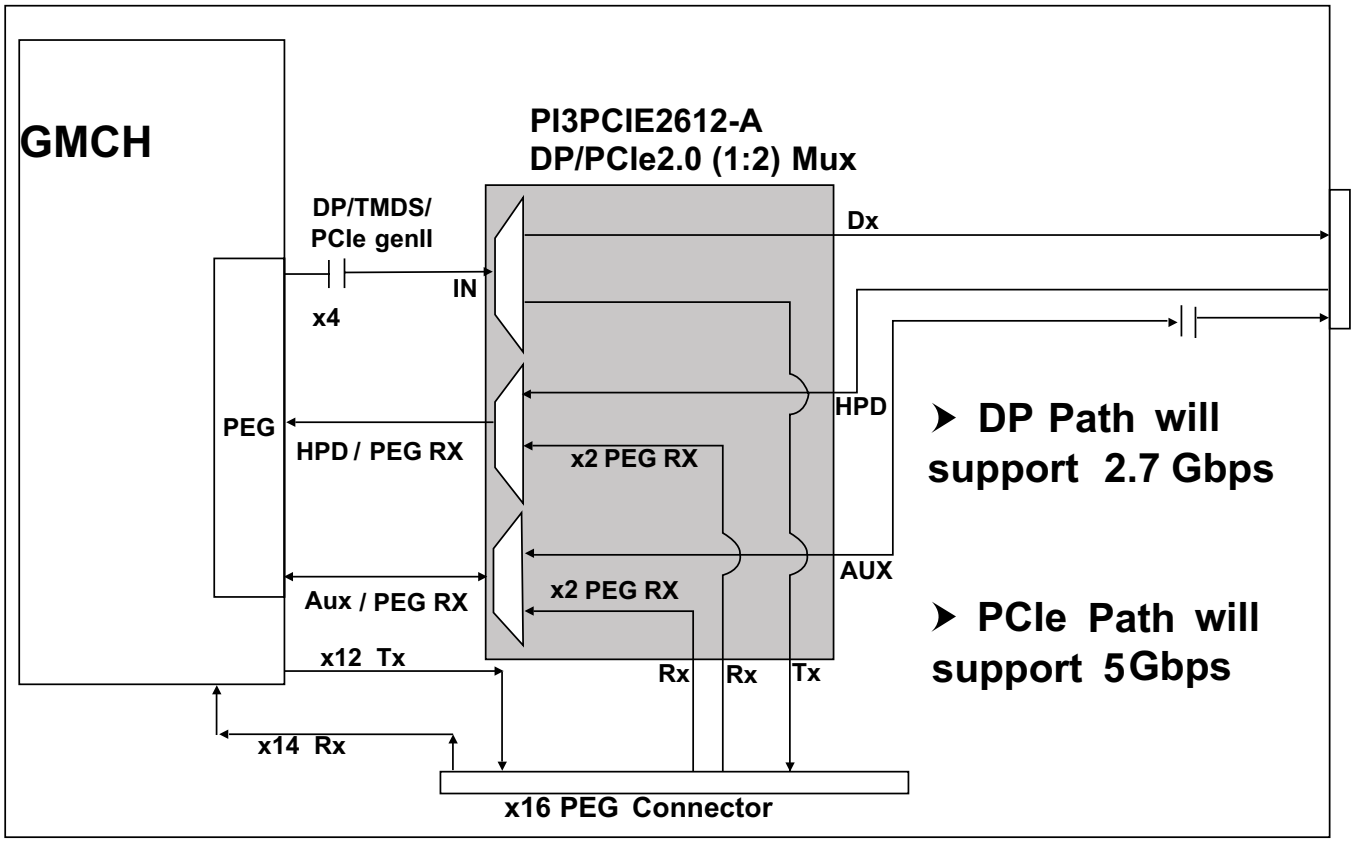
Application Example



Pin Description

Pin Number	Pin Name	Type	Description
26	AUX+	O	Differential input from HDMI/DP connector. AUX+ makes a differential pair with AUX-. AUX+ is passed through to the OUT+ pin when SEL = 1.
25	AUX-	O	Differential input from HDMI/DP connector. AUX- makes a differential pair with AUX+. AUX- is passed through to the OUT- pin when SEL = 1.
43, 42	D0+, D0-	O	Analog “pass through” output#1 corresponding to IN_0+ and IN_0-, when SEL = 1.
41, 40	D1+, D1-	O	Analog “pass through” output#1 corresponding to IN_1+ and IN_1-, when SEL = 1.
39, 38	D2+, D2-	O	Analog “pass through” output#1 corresponding to IN_2+ and IN_2-, when SEL = 1.
37, 36	D3+, D3-	O	Analog “pass through” output#1 corresponding to IN_3+ and IN_3-, when SEL = 1.

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Pin Number	Pin Name	Type	Description
1, 11, 16, 20, 21, 28, 29, 35, 48, 49, 56	GND	Power - Ground.	
24	HPD	I	The HPD signal comes from the HDMI or DP connector. This is a low frequency, 0V to 5V (HDMI) or 3.6V (DP) input signal at the connector. The HPD input at the mux is 3.6V max, so HDMI HPD must be shifted down from 5V before it is passed to the mux.
2	IN_0+	I	Differential input from GMCH PCIE outputs. IN_0+ makes a differential pair with IN_0-.
3	IN_0-	I	Differential input from GMCH PCIE outputs. IN_0- makes a differential pair with IN_0+.
4	IN_1+	I	Differential input from GMCH PCIE outputs. IN_1+ makes a differential pair with IN_1-.
5	IN_1-	I	Differential input from GMCH PCIE outputs. IN_1- makes a differential pair with IN_1+.
7	IN_2+	I	Differential input from GMCH PCIE outputs. IN_2+ makes a differential pair with IN_2-.
8	IN_2-	I	Differential input from GMCH PCIE outputs. IN_2- makes a differential pair with IN_2+.
9	IN_3+	I	Differential input from GMCH PCIE outputs. IN_3+ makes a differential pair with IN_3-.
10	IN_3-	I	Differential input from GMCH PCIE outputs. IN_3- makes a differential pair with IN_3+.
19	LE#	I	The latch gate is controlled by LE. 3.6V tolerant, low-voltage, single-ended input.
23	NC	Do Not Connect	
12	OUT+	O	Pass-through output from AUX+ input when SEL = 1. Pass-through output from Rx0+ input when SEL = 0.
13	OUT-	O	Pass-through output from AUX- input when SEL = 1. Pass-through output from Rx0- input when SEL = 0.
33	Rx0+	I/O	Differential input from PCIE connector or device. Rx0+ makes a differential pair with Rx0-. Rx0+ is passed through to the OUT+ pin when SEL = 0.
32	Rx0-	I/O	Differential input from PCIE connector or device. Rx0- makes a differential pair with Rx0+. Rx0- is passed through to the OUT- pin when SEL = 0.
31	Rx1+	I	Differential input from PCIE connector or device. Rx1+ makes a differential pair with Rx1-. Rx1+ is passed through to the X+ pin when SEL = 0.

(Continued)

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Pin Number	Pin Name	Type	Description
30	Rx1-	I	Differential input from PCIE connector or device. Rx1- makes a differential pair with Rx1+. Rx1- is passed through to the X- pin on a path that matches the Rx1+ to X+ path.
18	SEL	I	SEL controls the mux through a flow-through latch. 3.6V tolerant low-voltage single-ended output SEL = 0 for PCIE Mode SEL = 1 for DP Mode
54, 53	Tx0+,Tx0-	O	Analog “pass through” output#2 corresponding to IN_0+ and IN_0-, when SEL = 0.
52, 51	Tx1+, Tx1-	O	Analog “pass through” output#2 corresponding to IN_1+ and IN_1-, when SEL = 0.
47, 46	Tx2+, Tx2-	O	Analog “pass through” output#2 corresponding to IN_2+ and IN_2-, when SEL = 0.
45, 44	Tx3+, Tx3-	O	Analog “pass through” output#2 corresponding to IN_3+ and IN_3-, when SEL = 0.
6, 17, 22, 27, 34, 50, 55	VDD	Power	3.3V DC Supply, 3.3V +/- 10%
14	X+	I/O	HPD: Low frequency, 0V to 5V/3.3V (nominal) input signal at the connector. This signal comes from the HDMI/DP connector. X+: Analog “pass through” output corresponding to Rx1+.
15	X-	I	X- is an analog “pass-through” output corresponding to the Rx1- input. The path from Rx1- to X- must be matched with the path from Rx1+ to X+. X+ and X- form a differential pair when the pass-through mux mode is selected.

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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C
Supply Voltage to Ground Potential .....–0.5V to +4.6V
DC Input Voltage ..... –0.5V to V_{DD}
DC Output Current 120mA
Power Dissipation 0.5W

Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	3.3V Power Supply		3.0	3.3	3.6	V
I_{DD}	Total current from VDD 3.3V supply		0		2.5	mA
T_{CASE}	Case temperature range for operation within spec.		-40		85	Celcius

DC Electrical Characteristics (T_A = –40°C to +85°C, V_{DD} = 3.3V ± 10%)

Parameter	Description	Test Conditions	Min	Typ(1)	Max	Units
$V_{IH\text{-}EN}$(2)	Input high level		2.0		3.6	V
$V_{IL\text{-}EN}$(2)	Input Low Level		0		0.8	V
I_{IN_EN}(2)	Input Leakage Current	Measured with input at VIH-EN max and VIL-EN min	–10		10	uA
R_{ON}	On Resistance	V_{DD} = Min., V_{IN} = 1.3V, I_{IN} = 40mA			10	Ohm
C_{ON}	On Channel Capacitance	V_{IN} = 0, V_{DD} = 3.3V		3.0		pF

Note:
1. Typical values are at V_{DD} = 3.3V, T_A = 25°C ambient and maximum loading.
2. For SEL and LE# inputs

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Dynamic Electrical Characteristics for IN_x+/-, Rxy+/-, and Txy+/-

Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
DDIL	Differential Insertion Loss	f=1.2GHz f=2.5GHz f=5.0GHz f=7.5GHz		-1.5 -2.0 -5.0 -9.0		dB
$DDIL_{OFF}$	Differential Off Isolation	f= 0 to 3.0GHz f= 5.0GHz		-23.0 -20.0		
DDRL	Differential Return Loss	f= 0 to 2.8GHz f= 2.8 to 5.0GHz f= 5.0 to 7.5GHz		-14.0 -8.0 -4.0		
DDNEXT	Near End Crosstalk	f= 0 to 2.5GHz f= 2.5 to 5.0GHz f= 5.0 to 7.5GHz		-32.0 -26.0 -20.0		

Dynamic Electrical Characteristics for Dx+/-

Parameter	Description	Test Conditions	Min.	Typ.(1)	Max.	Units
$DDIL_{DP}$	Display Port Differential Insertion Loss	f= 0 to 1.35GHz f= 1.35 to 2.7GHz		-1.5 -4.5		dB
$DDRL_{DP}$	Display Port Differential Return Loss	f= 0 to 2.7GHz		-14		
$DDNEXT-_{DP}$	Display Port Near End Crosstalk	f= 0 to 2.7GHz		-32.0		

Switching Characteristics (T_A= -40º to +85ºC, V_{DD} = 3.3V±10%)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PZH}, t_{PZL}	Line Enable Time - SEL to D_X±, T_{XY}±, R_{XY}±, AUX±, HPD	See "Test Circuit for Electrical Chatacteristics"	0.5		12.0	ns
t_{PHZ}, t_{PLZ}	Line Disable Time - SEL to D_X±, T_{XY}±, R_{XY}±, AUX±, HPD	See "Test Circuit for Electrical Chatacteristics"	0.5		12.0	ns
t_{b-b}	Bit-to-bit skew within the same differential pair	See "Test Circuit for Electrical Chatacteristics"			7	ps
t_{ch-ch}	Channel-to-channel skew	See "Test Circuit for Electrical Chatacteristics"			35	ps

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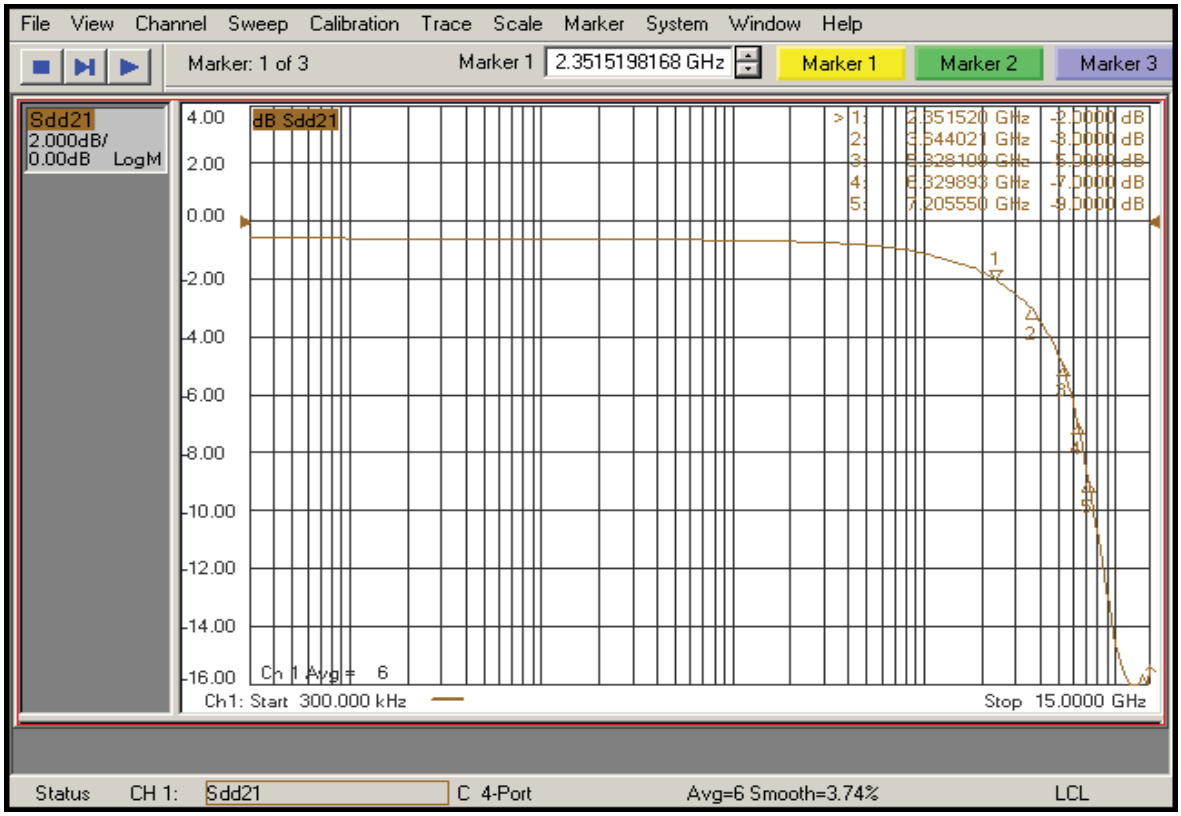
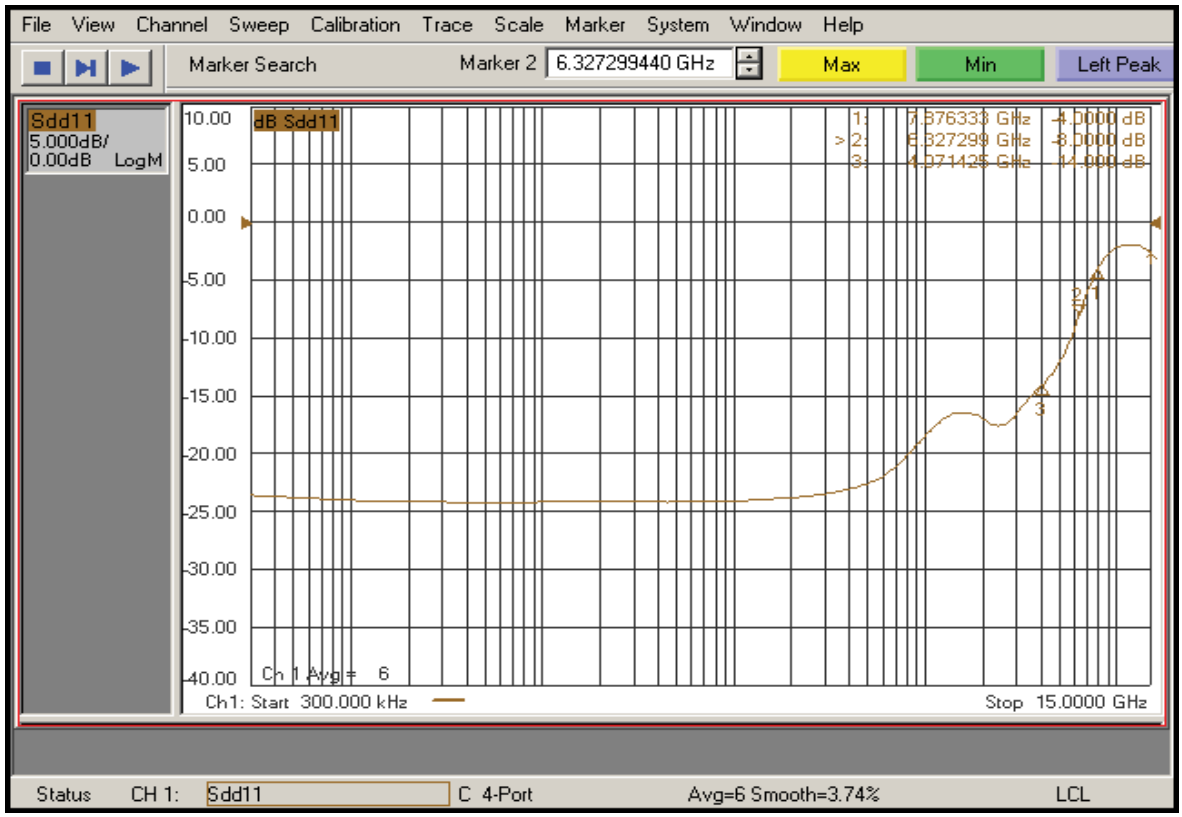


Differential Insertion Loss



Differential Return Loss

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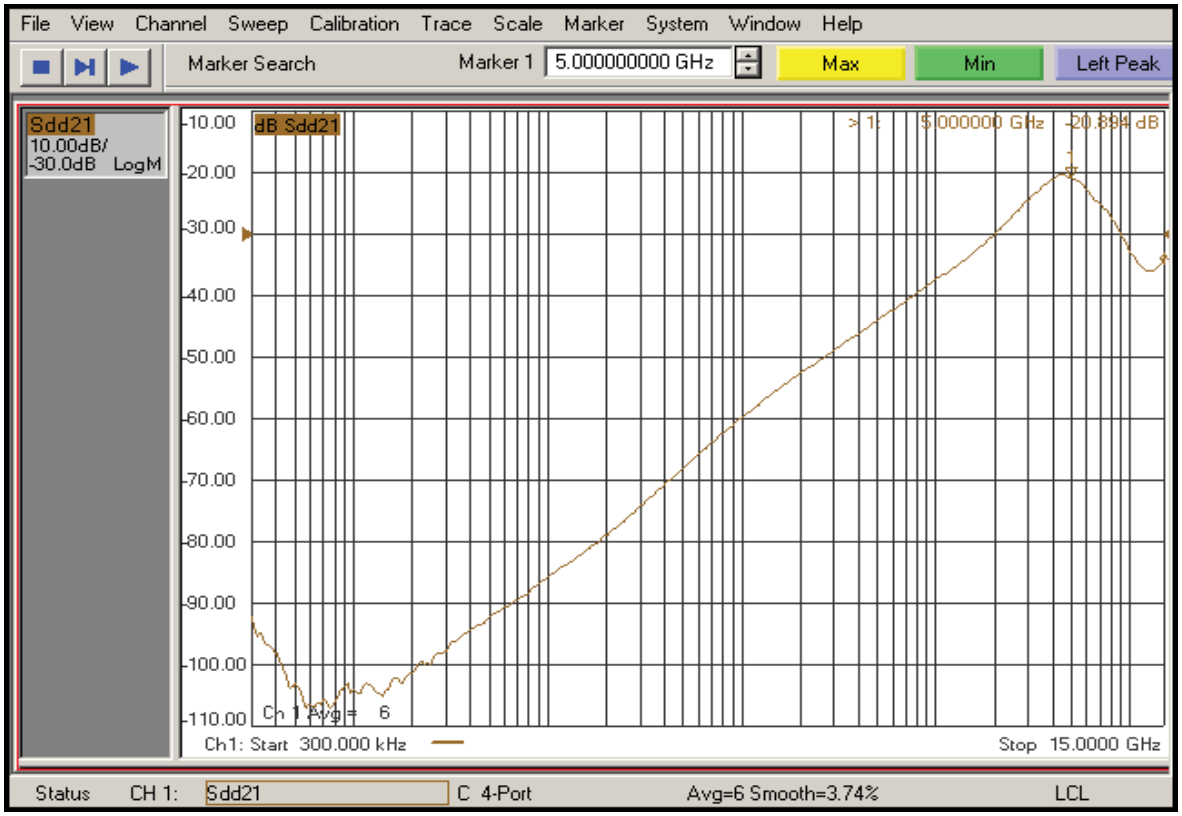
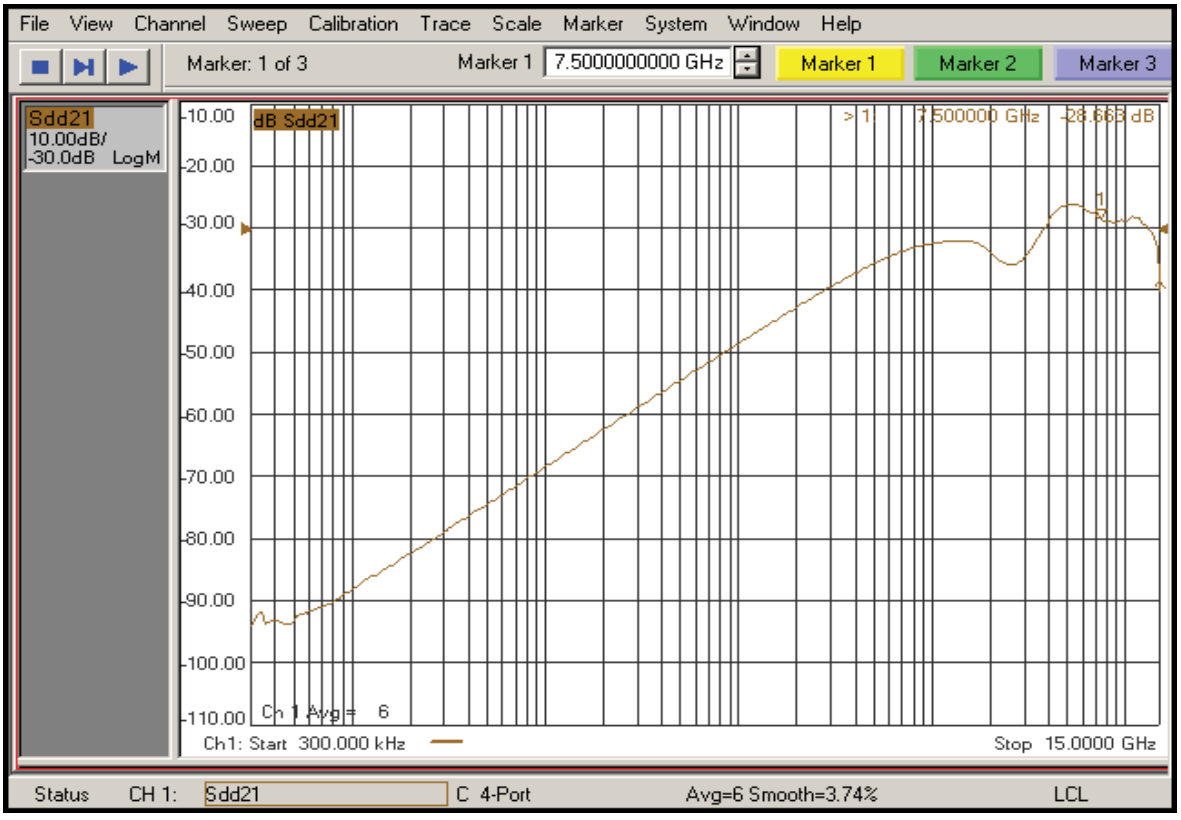


Off Isolation



Crosstalk

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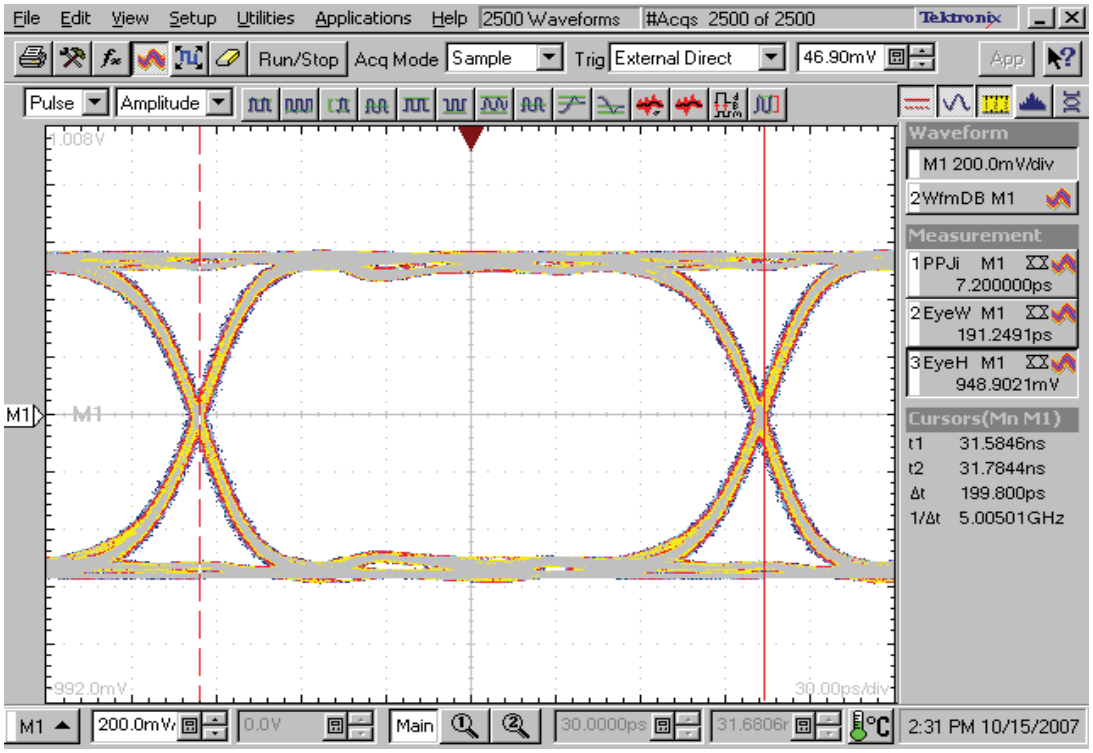
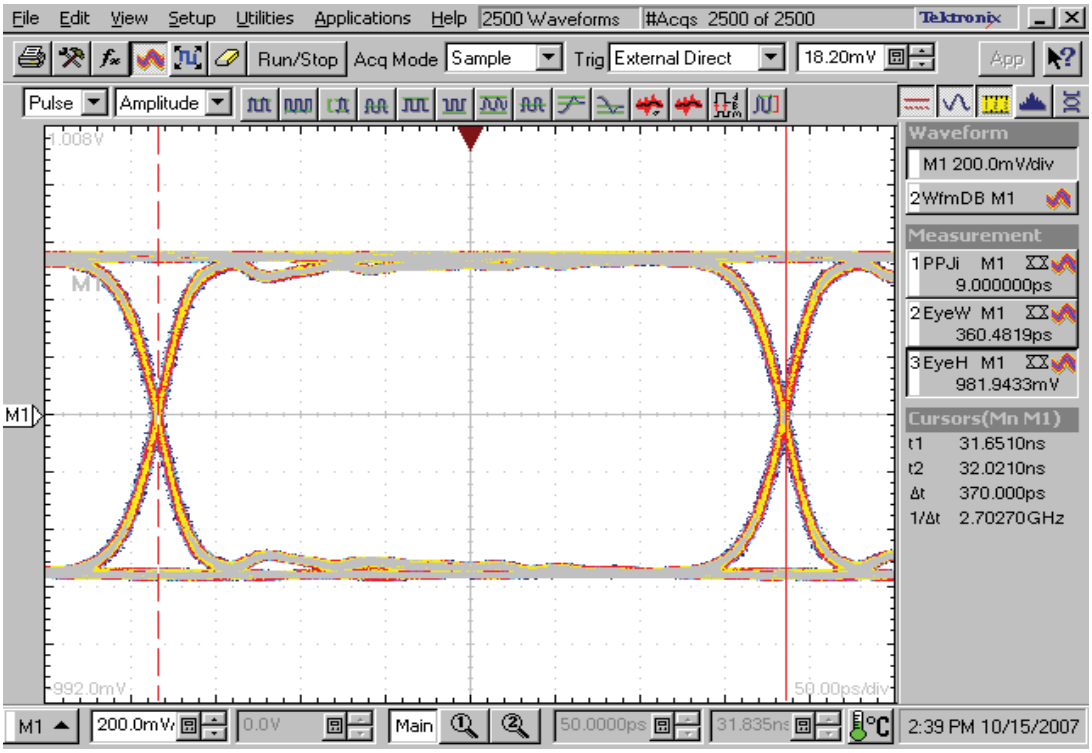


Tx Eye Diagram, 5.0 Gbps



Dx Eye Diagram, 2.7 Gbps

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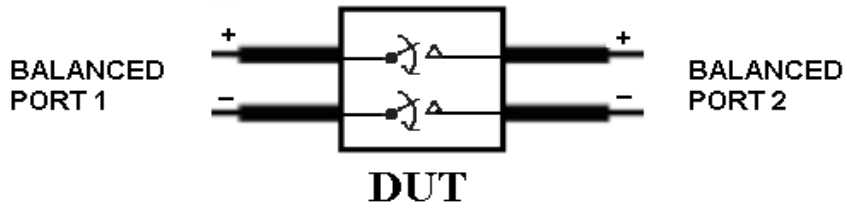
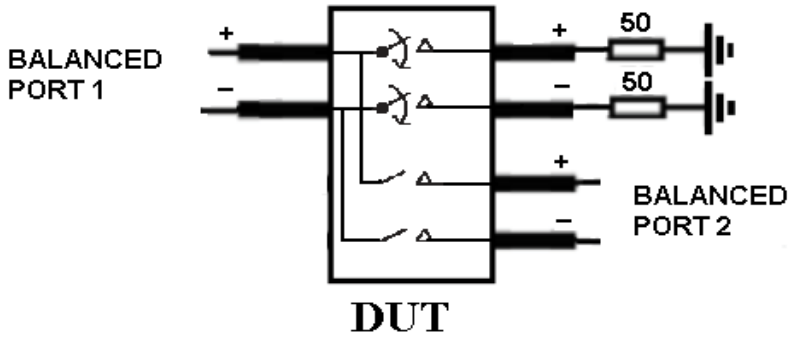
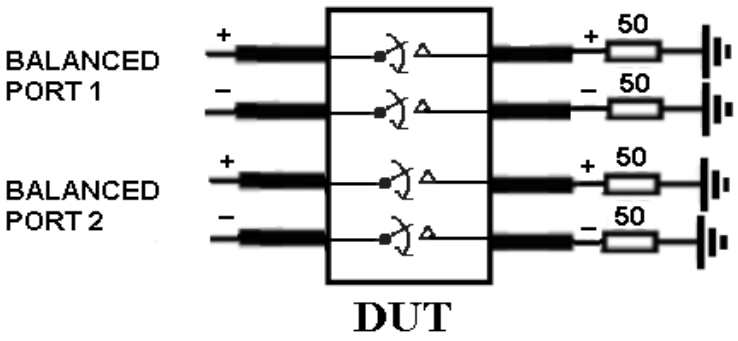
Differential Insertion Loss and Return Loss Test Circuit



Differential Off Isolation Test Circuit



Differential Near End Crosstalk Test Circuit



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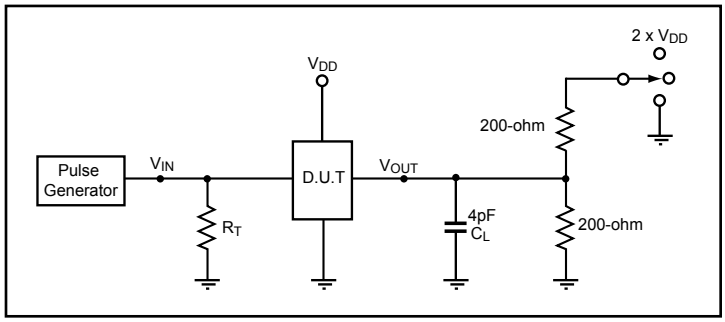
Test Circuit for Electrical Characteristics(1-5)



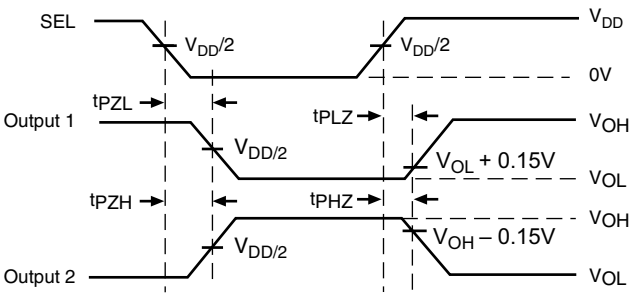
Switch Positions

Test	Switch
t_{PLZ}, t_{PZL}	2 x V_{DD}
t_{PHZ}, t_{PZH}	GND
Prop Delay	Open

Notes:

1. C_L = Load capacitance: includes jig and probe capacitance.
2. R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator
3. Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control. output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
4. All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O = 50\Omega$, $t_R \leq 2.5$ns, $t_F \leq 2.5$ns.
5. The outputs are measured one at a time with one transition per measurement.

Switching Waveforms



Voltage Waveforms Enable and Disable Times

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Applications Information

Differential Input Characteristics for IN_x+/- and Rxx+/- signals.

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	199.94	200.00	200.06	Ps	Defined by Gen2 spec.
$V_{RX-Diffp-p}$	Differential Input Peak to Peak Voltage	0.175		1.200	V	VRX-DIFFp-p = 2*|VRX-D+ - VRX-D-|. Applies to IN_D and RX_IN signals.
T_{RX-EYE}	Minimum Eye Width at IN_D input pair.	TBD			Tbit	
$V_{CM-AC-pp}$	AC Peak Common-Mode Input Voltage			100	mV	VCM-AC-pp = |VRX-D+ + VRX-D-| / 2 – VRX-CM-DC. VRX-CM-DC = DC(avg) of |VRX-D++ VRX-D-| / 2 VCM-AC-pp includes all frequencies above 30kHz.
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	W	Rx DC Differential Mode impedance.
Z_{RX-DC}	DC Input Impedance	40	50	60	W	Required IN_D+ as well as IN_D- DC impedance (50 W +/- 20% tolerance). Includes mux resistance.
$V_{RX-Bias}$	Rx input termination voltage	0		2.0	V	Intended to limit power-up stress on PCIE output buffers.
DDIL	Differential Insertion Loss	≥-[0.6*(f)+0.5] dB up to 2.5 GHz (for example, ≥-2 dB at f = 2.5 GHz); ≥-[1.2*(f-2.5)+2] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥-5 dB at f = 5 GHz); ≥-[1.6*(f-5)+5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-9 dB at f = 7.5 GHz);			dB	
DDRL	Differential Return Loss	≤ -14 dB up to 2.8 GHz; ≤ -8 dB up to 5 GHz; ≤ -4 dB up to 7.5 GHz.			dB	
DDNEXT	Near End Crosstalk	-32 dB max up to 2.5 GHz; -26 dB max up to 5.0 GHz; -20 dB max up to 7.5 GHz;			dB	
DDIL when switch is off	Differential Insertion Loss when switch is off	≤ -20 dB up to 3 GHz;			dB	

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PCIe Gen2 Output Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	W	Rx DC Differential Mode impedance.
Z_{RX-DC}	DC Input Impedance	40	50	60	W	Required IN_D+ as well as IN_D- DC impedance (50W +/- 20% tolerance). Includes mux resistance.
$V_{RX-Bias}$	Rx input termination voltage	0		2.0	V	Intended to limit power-up stress on PCIE output buffers.
DDIL	Differential Insertion Loss	≥-[0.6*(f)+0.5] dB up to 2.5 GHz (for example, ≥-2 dB at f = 2.5 GHz); ≥-[1.2*(f-2.5)+2] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥-5 dB at f = 5 GHz); ≥-[1.6*(f-5)+5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-9 dB at f = 7.5 GHz);			dB	
DDRL	Differential Return Loss	≤ -14 dB up to 2.8 GHz; ≤ -8 dB up to 5 GHz; ≤ -4 dB up to 7.5 GHz.			dB	
DDNEXT	Near End Crosstalk	-32 dB max up to 2.5 GHz; -26 dB max up to 5.0 GHz; -20 dB max up to 7.5 GHz;			dB	
DDIL when switch is off	Differential Insertion Loss when switch is off	≤ -20 dB up to 3 GHz;			dB	

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Display Port Output Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
Tbit	Unit Interval	333			ps	Normal Tbit at 2.7Gb/s=370ps. 333ps=370ps-10%
$V_{RX-Diffp-p}$	Differential Input Peak to Peak Voltage	0.340		1.38	V	VRX-DIFFp-p = 2*|VRX-D+ - VRX-D-|. Applies to IN_D and RX_IN signals.
T_{JIT}	Jitter added to high-speed signals			7.4	ps	Jitter budget for high-speed signals as they pass through the display mux. 7.4ps = 0.02 Tbit at 2.7Gb/s
DDIL	Differential Insertion Loss	≥-[0.75*(f)+0.5] dB up to 1.35 GHz; ≥-[2.2*(f-1.35)+1.5] dB for 1.35 GHz < f ≤ 2.7 GHz			dB	For example, ≥-1.5 dB at f = 1.35 GHz For example, ≥-4.5 dB at f = 2.7 GHz
DDRL	Differential Return Loss	≤ -14 dB up to 2.7 GHz			dB	
DDNEXT	Near End Crosstalk	-32 dB max up to 2.7 GHz			dB	

HPD Input Characteristics

Symbol	Parameter	Min	Nom	Max	Units	Comments
V_{IH-HPD}	Input high level			3.6	V	Low-speed input changes state on cable plug/unplug.
V_{IL-HPD}	HPD Input Low Level	0				V
I_{IN_HPD}	HPD input leakage current			|10|	uA	Measured with HPD at VIH-HPD max and VIL-HPD min
T_{HPD}	HPD_IN to HPD propagation delay.			200	ns	Time from HPD_IN changing state to HPD changing state. Includes HPD rise/fall time.
T_{RF-HPD}	HPD rise/fall time.	1		20	ns	Time required to transition from VOH-HPD to VOL-HPD or from VOL-HPD to VOH-HPD.

Termination Resistors

Symbol	Parameter	Min	Nom	Max	Units	Comments
R_{DDC}	DDC Termination Resistors	1.3K	1.5k	2.2k	W	Applies to both 3.3V and 5V pull up resistors.

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Switch Signal Integrity Requirements and Test Procedures for 5.0 Gb/s

Signal integrity requirements for 5.0 Gb/s applications of the switch are specified. Also included are the requirements of the test fixture for switch S-parameter measurements.

Signal Integrity Requirements

The procedures outlined in ANSI Electronics Industry Alliance (EIA) standards documents shall be followed:

- EIA 364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- EIA 364-90 – Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- EIA 364-108- Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems

Signal Integrity Requirements and Test Procedures for 5.0 Gb/s

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to a 100 ohms differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 1.12. 3. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.	≥-[0.6*(f)+0.5] dB up to 2.5 GHz (for example, ≥-2 dB at f = 2.5 GHz); ≥-[1.2*(f-2.5)+2] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥-5 dB at f = 5 GHz); ≥-[1.6*(f-5)+5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-9 dB at f = 7.5 GHz); Refer to Figure 1.
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to a 100 ohms differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 1.12. 3. The test fixture effect shall be removed. Refer to Note 1.	≤ -14 dB up to 2.8 GHz; ≤ -8 dB up to 5 GHz; ≤ -4 dB up to 7.5 GHz. Refer to Figure 2.
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs	-32 dB max up to 2.5 GHz; -26 dB max up to 5.0 GHz; -20 dB max up to 7.5 GHz; See Figure 3.
Differential Insertion Loss (DDIL) when switch is turned off	EIA 364-101	≤ -20 dB up to 3 GHz;

Notes:
1. The specified S parameters requirements are for switch component only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

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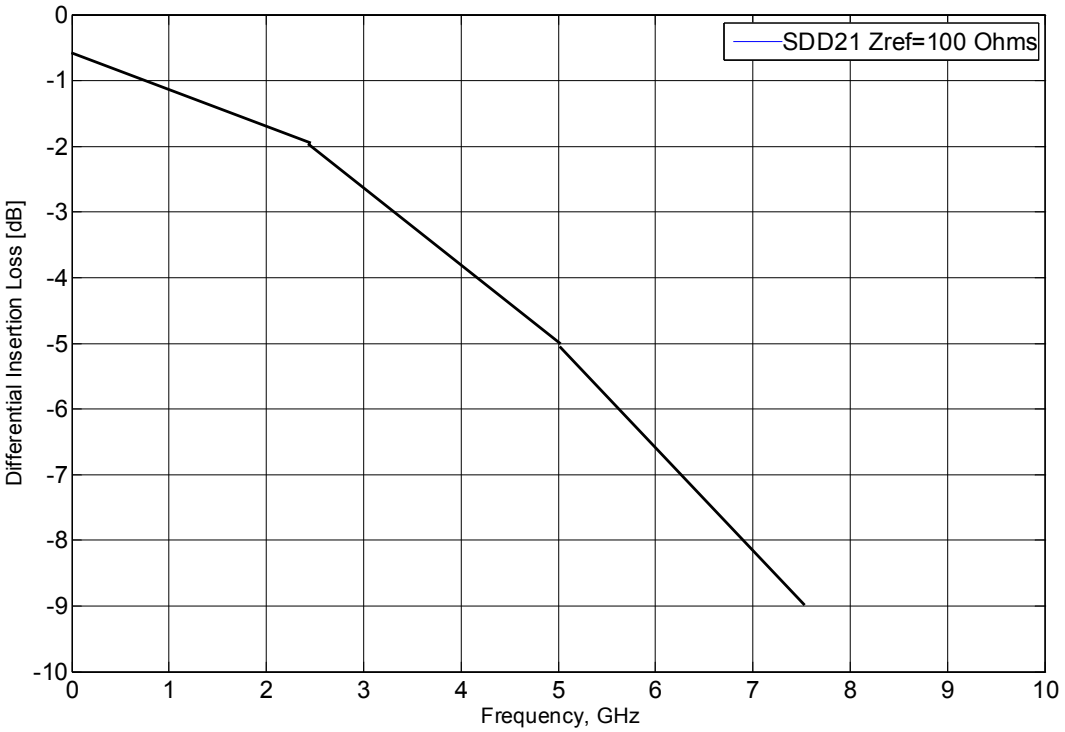

Figure 1: Illustration of differential insertion loss requirement.

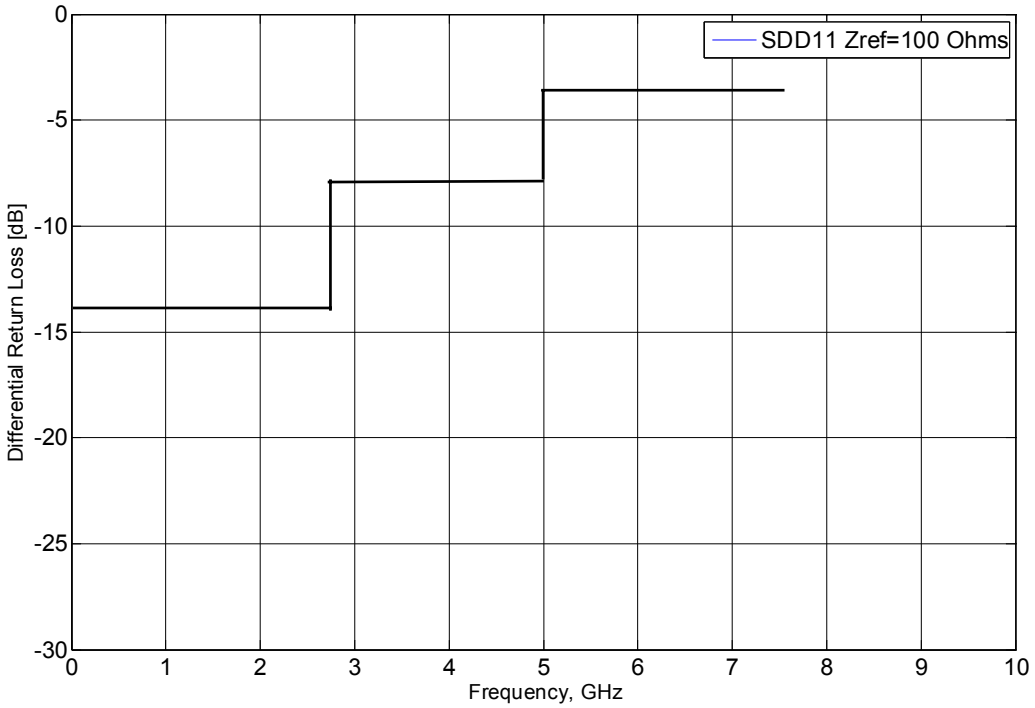

Figure 2: Illustration of differential return loss requirement.

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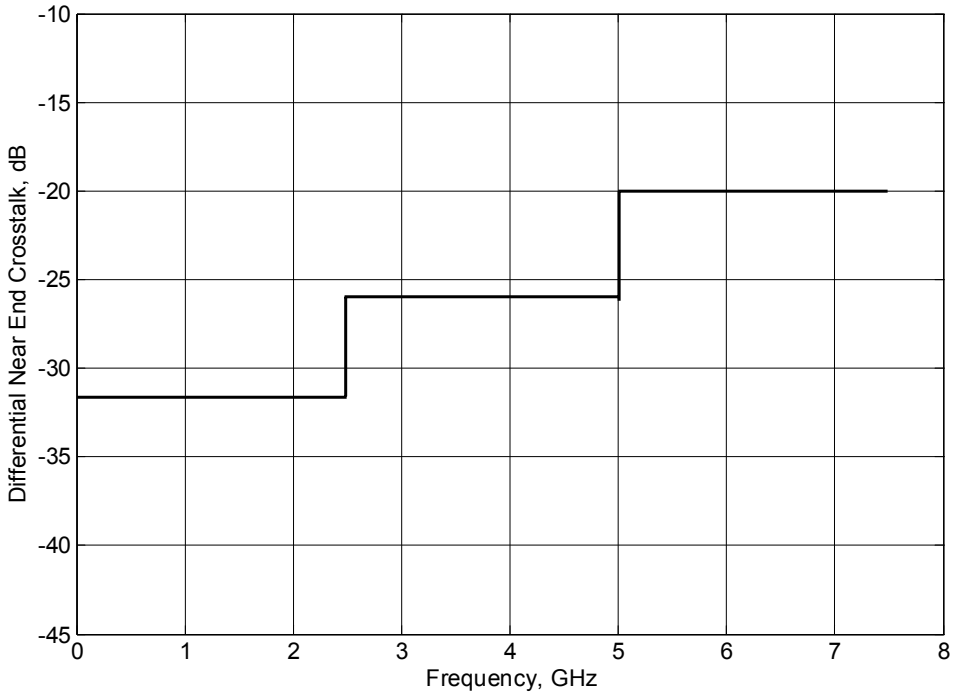

Figure 3: Illustration of different ial near end crosstalk requirement.

Switch Test Fixture Requirements

The test fixture for switch S-parameter measurement shall be designed and built to specific requirements, as described below, to ensure good measurement quality and consistency:

- The test fixture shall be a FR4-based PCB of the microstrip structure; the dielectric thickness or stackup shall be about 4 mils.
- The total thickness of the test fixture PCB shall be 1.57 mm (0.62”).
- The measurement signals shall be launched into the switch from the top of the test fixture, capturing the through-hole stub effect.
- Traces between the DUT and measurement ports (SMA or microprobe) should be uncoupled from each other, as much as possible. Therefore, the traces should be routed in such a way that traces will diverge from each other exiting from the switch pin field.
- The trace lengths between the DUT and measurement port shall be minimized. The maximum trace length shall not exceed 1000 mils. The trace lengths between the DUT and measurement port shall be equal.
- All of the traces on the test board and add-in card must be held to a characteristic impedance of 50 Ohms with a tolerance of +/- 7%.
- SMA connector is recommended for ease of use. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 60 ps rise time should be within 50+/-7 ohms.

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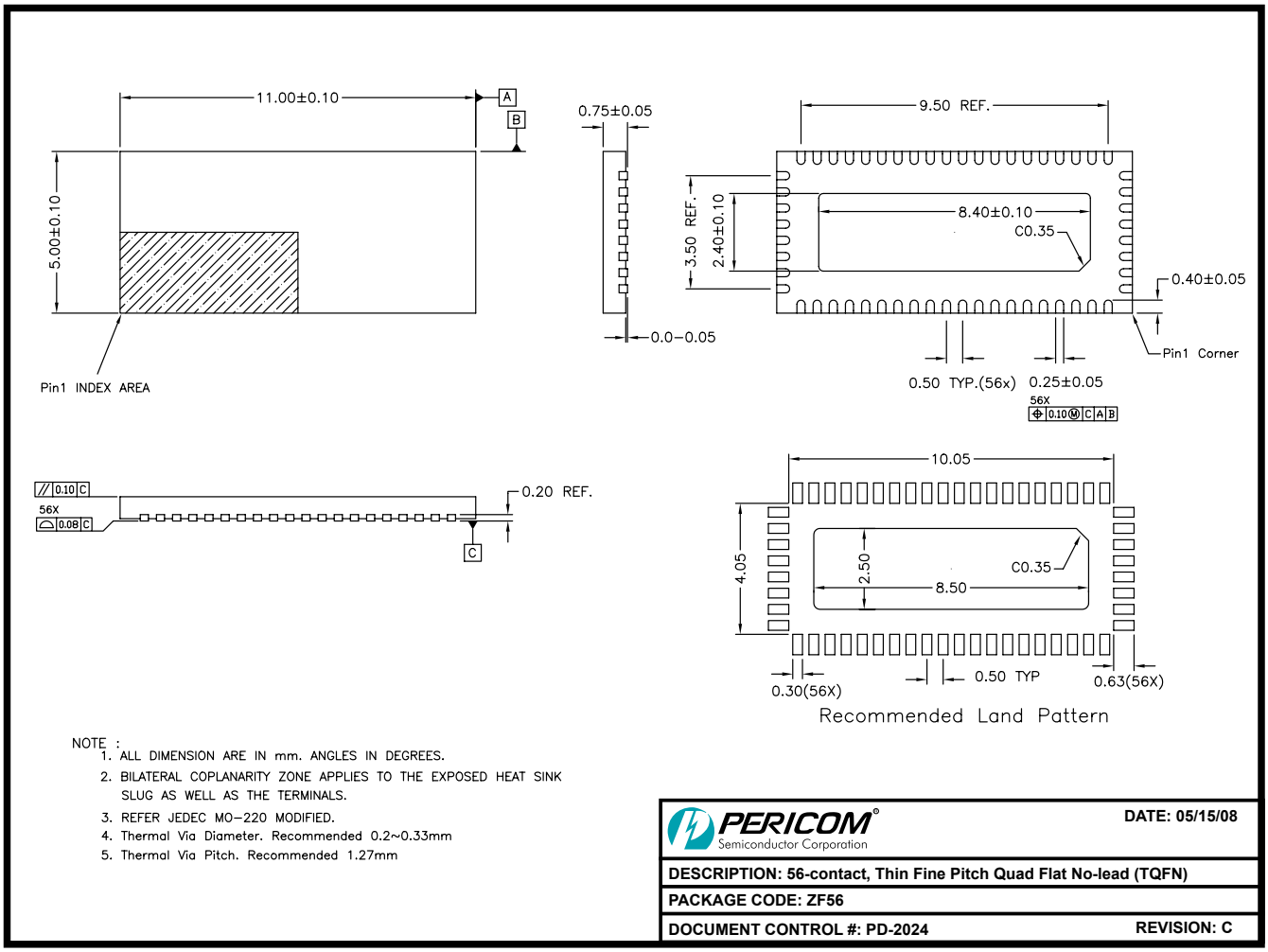
Packaging Mechanical: 56-Contact TQFN (ZFE)



08-0208

Ordering Information

Ordering Code	Package Code	Package Description
PI3PCIE2612-AZFE	ZF	Pb-free & Green, 56-contact TQFN

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging

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