

# Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

## High-Performance Silicon-Gate CMOS

### MC74HC541A, MC74HCT541A

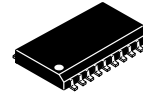
The MC74HC541A/MC74HCT541A is identical in pinout to the LS541. The MC74HC541A inputs are compatible with Standard CMOS outputs. External pull-up resistors make them compatible with LSTTL outputs. The MC74HCT541A may be used as a level converter for interfacing TTL or NMOS outputs to high speed CMOS inputs.

The HC541A/HCT541A is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. This device features inputs and outputs on opposite sides of the package and two ANDed active-low output enables.

The HC541A is similar in function to the HC540A, which has inverting outputs.

#### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance With the JEDEC Standard No. 7 A Requirements
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- -Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

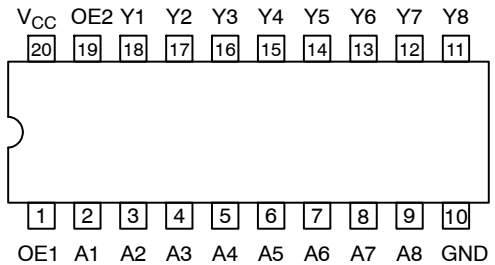


SOIC-20  
DW SUFFIX  
CASE 751D

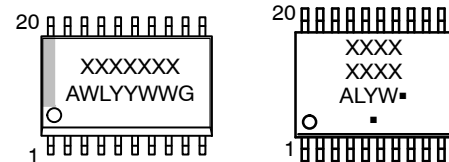


TSSOP-20  
DT SUFFIX  
CASE 948E

#### PIN ASSIGNMENT



#### MARKING DIAGRAMS



XXXXXXXX = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### FUNCTION TABLE

Inputs			Output Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

X = Don't Care

Z = High Impedance

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# MC74HC541A, MC74HCT541A

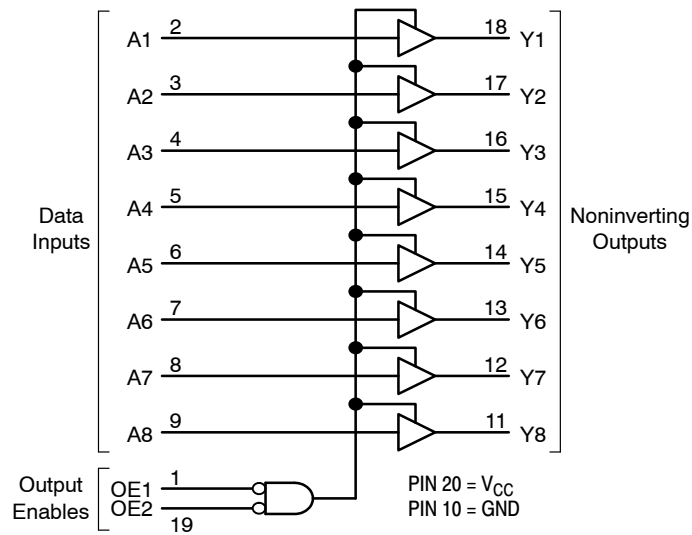


Figure 1. Logic Diagram

# MC74HC541A, MC74HCT541A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	−0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage	−0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage	−0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Diode Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Input Diode Current, Per Pin	±35	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
I <sub>IK</sub>	Input Clamp Current (V <sub>IN</sub> < 0 or V <sub>IN</sub> > V <sub>CC</sub> )	±20	mA
I <sub>OK</sub>	Output Clamp Current (V <sub>OUT</sub> < 0 or V <sub>OUT</sub> > V <sub>CC</sub> )	±20	mA
T <sub>STG</sub>	Storage Temperature Range	−65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 1) <div>SOIC−20W WQFN20 QFN20 TSSOP−20</div>	<div>96 99 111 150</div>	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 25°C <div>SOIC−20W WQFN20 QFN20 TSSOP−20</div>	<div>1302 1256 1127 833</div>	mW
MSL	Moisture Sensitivity	Level 1	–
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V <sub>ESD</sub>	ESD Withstand Voltage (Note 2) Human Body Model Charged Device Model	<div>&gt; 4000 &gt; 1000</div>	V
I <sub>LATCHUP</sub>	Latchup Performance (Note 3)	±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
2. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
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### MC74HC

$V_{CC}$	DC Supply Voltage	2.0	6.0	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Note 4)	0	$V_{CC}$	V
$T_A$	Operating Free-Air Temperature	-55	+125	°C
$t_r, t_f$	Input Rise or Fall Time	$V_{CC} = 2.0\text{ V}$ $V_{CC} = 4.5\text{ V}$ $V_{CC} = 6.0\text{ V}$	0 1000 500 400	ns

### MC74HCT

$V_{CC}$	DC Supply Voltage	4.5	5.5	V
$V_{IN}, V_{OUT}$	DC Input Voltage, Output Voltage (Note 4)	0	$V_{CC}$	V
$T_A$	Operating Free-Air Temperature	-55	+125	°C
$t_r, t_f$	Input Rise or Fall Time	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

# MC74HC541A, MC74HCT541A

## DC CHARACTERISTICS (MC74HC541A)

Symbol	Parameter	Condition	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55 to 25°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>OUT</sub> = 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>OUT</sub> = V <sub>CC</sub> - 0.1 V  I <sub>OUT</sub>   ≤ 20 μA	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>IN</sub> = V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>IN</sub> = V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 3.6 mA	3.0	2.48	2.34	2.20	
		I <sub>OUT</sub>   ≤ 6.0 mA	4.5	3.98	3.84	3.70	
		I <sub>OUT</sub>   ≤ 7.8 mA	6.0	5.48	5.34	5.20	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>IN</sub> = V <sub>IH</sub>  I <sub>OUT</sub>   ≤ 3.6 mA	3.0	0.26	0.33	0.40	
		I <sub>OUT</sub>   ≤ 6.0 mA	4.5	0.26	0.33	0.40	
		I <sub>OUT</sub>   ≤ 7.8 mA	6.0	0.26	0.33	0.40	
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	Output in High Impedance State V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# MC74HC541A, MC74HCT541A

## AC CHARACTERISTICS (MC74HC541A)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55 to 25°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 3)	2.0 3.0 4.5 6.0	80 30 18 15	100 40 23 20	120 55 28 25	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 3)	2.0 3.0 4.5 6.0	110 45 25 21	140 60 31 26	165 75 38 31	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 3)	2.0 3.0 4.5 6.0	110 45 25 21	140 60 31 26	165 75 38 31	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C <sub>IN</sub>	Maximum Input Capacitance		10	10	10	pF
C <sub>OUT</sub>	Maximum 3-State Output Capacitance (High Impedance State Output)		15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Buffer) (Note 5)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V, V <sub>EE</sub> = 0 V	pF
		35	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

# MC74HC541A, MC74HCT541A

## DC CHARACTERISTICS (MC74HCT541A)

Symbol	Parameter	Condition	V <sub>CC</sub> V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	4.5	3.98	3.84	3.70	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 6.0 mA	4.5	0.26	0.33	0.40	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum 3-State Leakage Current	Output in High Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	5.5	±0.5	±5.0	±10.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4	40	160	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA		≥ −55°C	25 to 125°C		mA
			5.5	2.9	2.4		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Total Supply Current = I<sub>CC</sub> + ΣΔI<sub>CC</sub>.

## AC CHARACTERISTICS (MC74HCT541A)

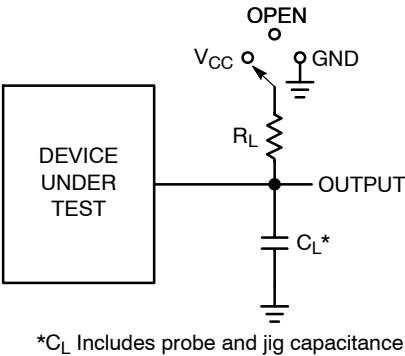
Symbol	Parameter	Guaranteed Limit			Unit
		-55 to 25°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A to Output Y (Figures 2 and 3)	23	28	32	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 3)	30	34	38	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 2 and 3)	30	34	38	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 2 and 3)	12	15	18	ns
C <sub>in</sub>	Maximum Input Capacitance	10	10	10	pF
C <sub>out</sub>	Maximum 3-State Output Capacitance (Output in High Impedance State)	15	15	15	pF

C <sub>PD</sub>	Power Dissipation Capacitance (Per Buffer)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		55	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

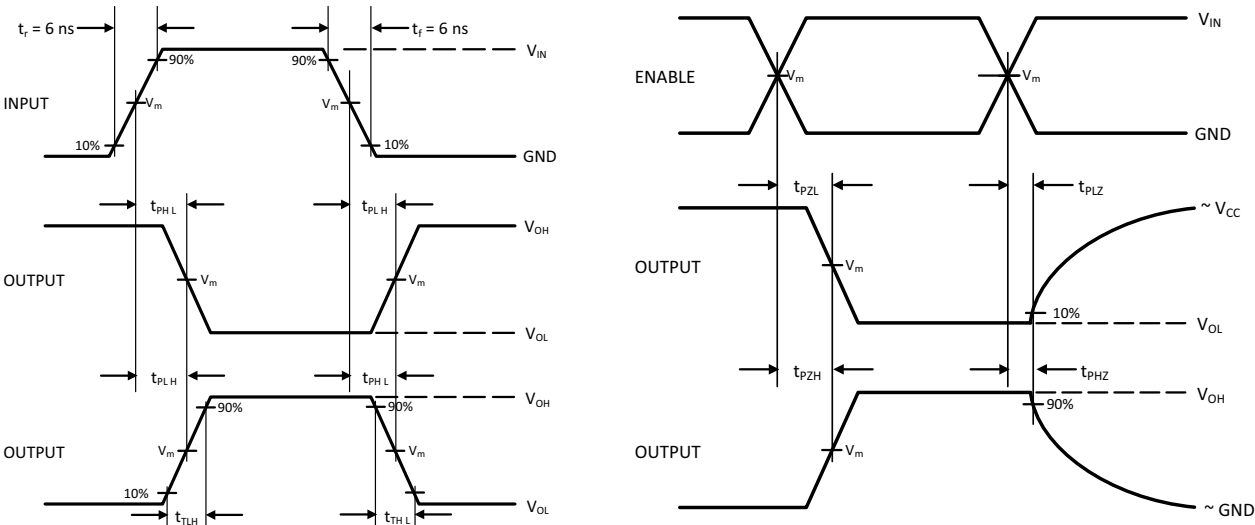
\*Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

MC74HC541A, MC74HCT541A



Test	Switch Position	C <sub>L</sub>	R <sub>L</sub>
t <sub>PLH</sub> / t <sub>PHL</sub>	Open	50 pF	1 kΩ
t <sub>PLZ</sub> / t <sub>PZL</sub>	V <sub>CC</sub>		
t <sub>PHZ</sub> / t <sub>PZH</sub>	GND		

Figure 2. Test Circuit



Device	V <sub>IN</sub> , V	V <sub>m</sub> , V
MC74HC541A	V <sub>CC</sub>	50% x V <sub>CC</sub>
MC74HCT541A	3 V	1.3 V

Figure 3. Switching Waveforms

# MC74HC541A, MC74HCT541A

## PIN DESCRIPTIONS

### INPUTS

#### A1, A2, A3, A4, A5, A6, A7, A8 (PINS 2, 3, 4, 5, 6, 7, 8, 9)

Data input pins. Data on these pins appear in non-inverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

#### OE1, OE2 (PINS 1, 19)

Output enables (active-low). When a low voltage is applied to both of these pins, the outputs are enabled and the

device functions as a non-inverting buffer. When a high voltage is applied to either input, the outputs assume the high impedance state.

### OUTPUTS

#### Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8 (PINS 18, 17, 16, 15, 14, 13, 12, 11)

Device outputs. Depending upon the state of the output enable pins, these outputs are either non-inverting outputs or high-impedance outputs.

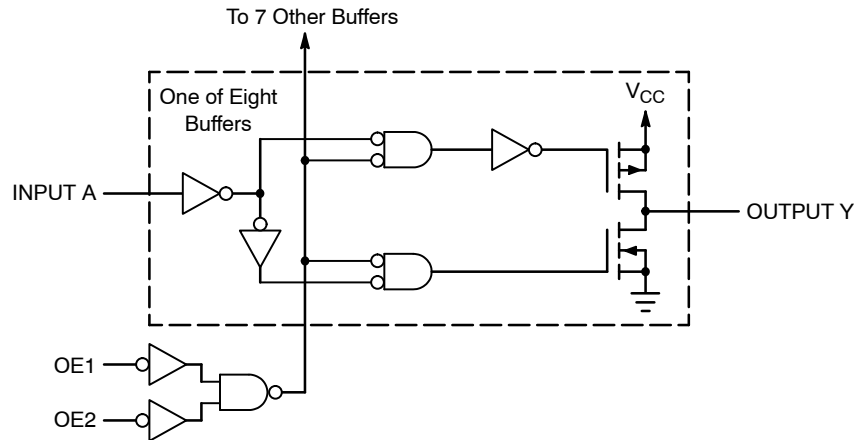


Figure 4. Logic Detail

## ORDERING INFORMATION

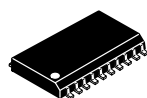
Device	Marking	Package	Shipping <sup>†</sup>
MC74HC541ADWG	HC541A	SOIC-20 Wide	38 Units / Rail
MC74HC541ADWR2G	HC541A	SOIC-20 Wide	1000 / Tape & Reel
MC74HC541ADWR2G-Q*	HC541A	SOIC-20 Wide	1000 / Tape & Reel
MC74HC541ADTG	HC 541A	TSSOP-20	75 Units / Rail
MC74HC541ADTR2G	HC 541A	TSSOP-20	2500 / Tape & Reel
MC74HC541ADTR2G-Q*	HC 541A	TSSOP-20	2500 / Tape & Reel
MC74HCT541ADWG	HCT541A	SOIC-20 Wide	38 Units / Rail
MC74HCT541ADWR2G	HCT541A	SOIC-20 Wide	1000 / Tape & Reel
MC74HCT541ADTR2G	HCT 541A	TSSOP-20	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*-Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.



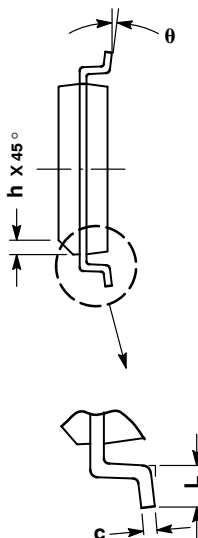
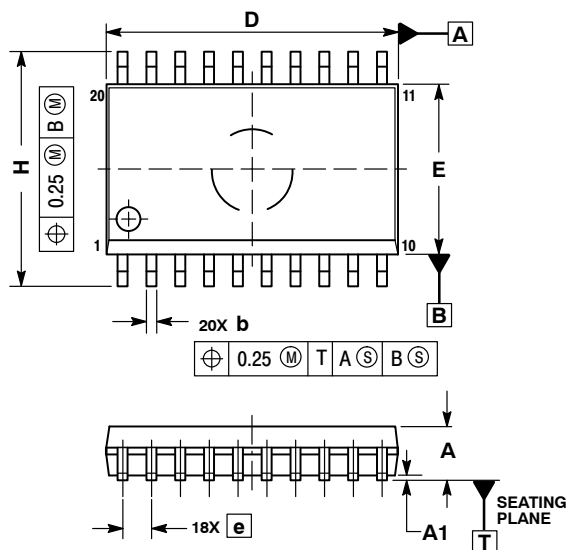
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015

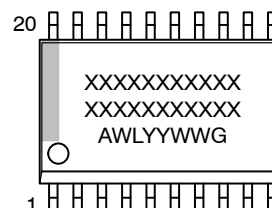


## NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

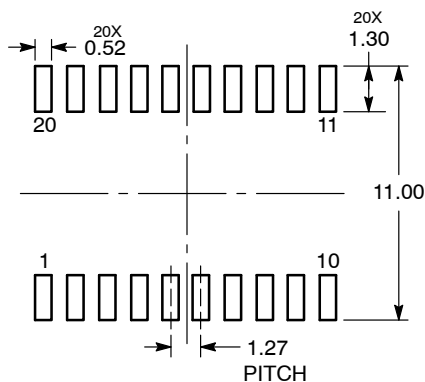
DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

## GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

## RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

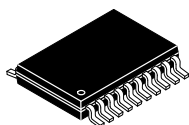
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

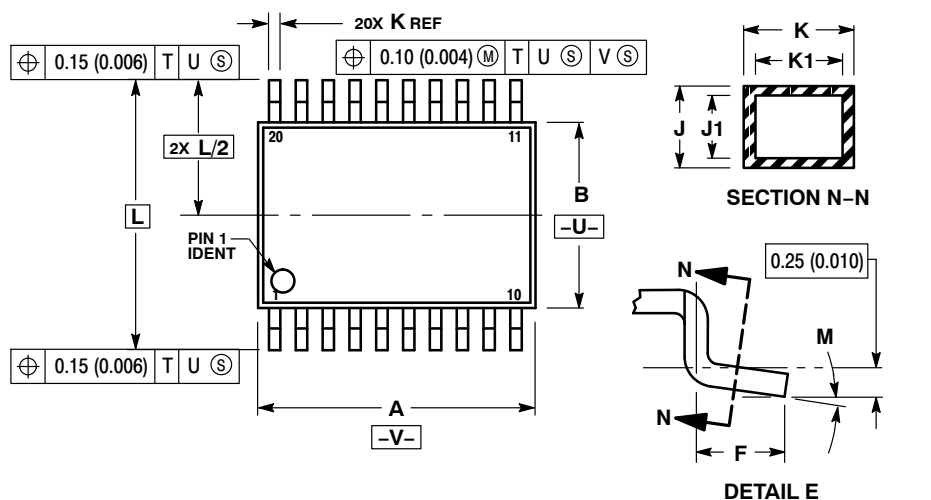
ON Semiconductor®



SCALE 2:1

TSSOP-20 WB  
CASE 948E  
ISSUE D

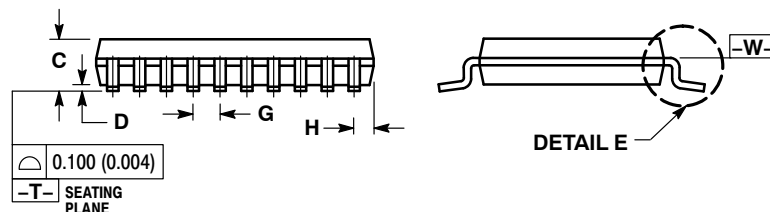
DATE 17 FEB 2016



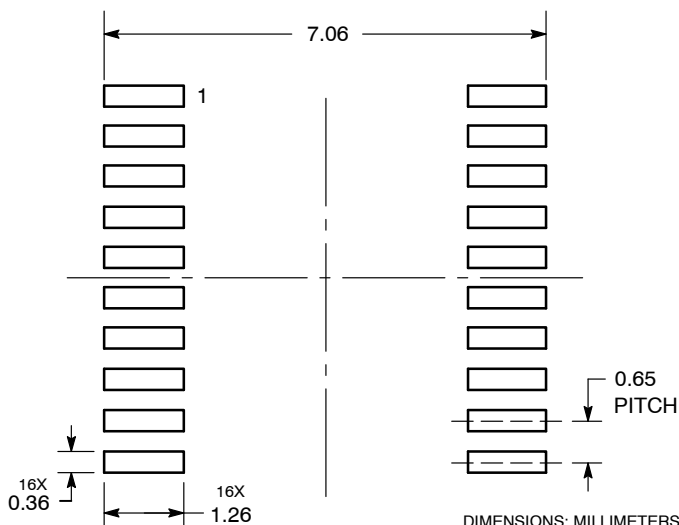
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

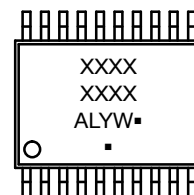
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



## SOLDERING FOOTPRINT



## GENERIC MARKING DIAGRAM\*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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