EQCO125X40 Family

EQCO125X40, EQCO125T40, EQCO62X20, EQCO31X20

12.5 Gbps Asymmetric Equalizer/Driver/Repeater Product Brief

Features

- Equalizer for up to 40m of coaxial cable at 12.5 Gbps or up to 130m at 1.25 Gbps using Belden 1694A cable
- Same chip used at Device (Camera) and Host (Frame Grabber) for asymmetric full-duplex communication
- Lower Cost version EQCO125T40 for Device (Camera) side only
- Cable types supported are 75Ω coax, 50Ω coax, and 100Ω STP (Shielded Twisted Pair)
- Simultaneous signaling over a single cable:
  - Up to 12.5 Gbps downlink
  - 21 or 42 Mbps uplink
  - Power over Coax
- Can also be used as a stand-alone cable repeater with simultaneous power, downlink and uplink over a single cable
- Integrated termination resistors for differential signaling
- CDR (Clock-Data Recovery) restores signal integrity in both directions
- Both Uplink and Downlink include equalizer, CDR and Cable driver (see Figure 1-2)
- Reference-clock free operation (no crystal or clock needed)
- Low power consumption / single supply @ 1.25V
- 16-pin, 0.65 mm pin pitch, 4 mm QFN package
- Small PCB footprint for EQCO125X40 Family with few off-chip components
- Industrial temperature range
- Pb-free and RoHS compliant

Applications

- CoaXPress compliant systems, supports all CoaXPress standards and speeds
- Links for high-definition Cameras
- Links between FPGAs
- High-speed capture cards over long cable lengths
- Machine Vision, Military, Aerospace, Medical, Broadcast and Surveillance cameras, Intelligent Traffic Systems
- When a single cable carrying power, video data and camera control stream is needed

General Description

The EQCO125T40 is a single chip (equalizer, driver, reclocker) that repeats high-speed 8b/10b coded data signals with a downstream bit-rate between 1.25 to 12.5 Gbps. From a cable or PCB trace pair, the signal is received by an auto-adaptive equalizer that compensates for higher-frequency losses in the preceding channel. A reference-less Clock-Data Recovery (CDR) subsequently self-adapts to the incoming bit-rate and resets the jitter back to a low value for maintaining signal integrity. A cable driver launches this clean signal back onto a cable or PCB trace pair. When placed in series as a repeater, a signal can travel through several EQCO125X40 Family devices to the destination. The EQCO125T40 CDR restores signal integrity at each link along the way.

The high-speed direction (or downlink) has a simultaneous complementary uplink, operating at 20.833 Mbps or 41.666 Mbps 8b/10b coded signaling. This uplink also includes an equalizer, a reference-less CDR and a cable driver, operating with a transparent full-duplex and self-adaptive downlink.

The EQCO125X40 Family can be used as a CoaXPress transmitter inside a camera, as a CoaXPress receiver inside a frame grabber and as a CoaXPress repeater inside an active coax cable or link. It can also be used as a generic high-speed signaling transport for any 8b/10b application. In general it can be regarded as an ideal means for using the high bit-rate ports on an FPGA in real-world applications. This allows the high-speed signal to get an increase in signal integrity along its signaling path at strategic places: e.g. when changing the signaling nature from single-ended to differential or vice-versa, after long runs of cable, or recovering the signal from skin effect and/or dielectric losses. The CDR resets accumulated jitter due to small impedance mismatches, non-ideal connectors, PCB-vias, etc., and yields better signal integrity. This is also useful when the signal chain includes an optical link.

TYPICAL LINK PERFORMANCE

	Typical maximum cable length for Belden (m)			
Bit-rate (Gbps)	**1694A**	**4694R**	**4855R**	**4731R**
1.25	130	137	75	210
2.5	110	118	64	180
3.125	100	108	60	160
5	65	70	40	105
6.25	55	60	33	90
10	40	45	24	65
12.5	40	45	24	65

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1.0 BASIC APPLICATION INFORMATION

The EQCO125X40 Family repeater chip is designed to simultaneously transmit and receive signals on a single cable or PCB trace pair. In one direction an 8b/10b coded downlink signal is transmitted between 1.25 Gbps and 12.5 Gbps. In the opposite direction a lower speed 8b/10b coded uplink signal is transmitted at 20.833 Mbps or 41.666 Mbps. The EQCO125X40 has an integrated high-speed equalizer, reclocker and cable driver. The uplink channel also has an integrated receiver, reclocker and driver. Figure 1-1 illustrates a typical EQCO125X40 link set-up.

The downlink signal is transmitted with 600 mV transmit amplitude. As this signal is attenuated by the coax (or STP) over distance, it is recovered by the equalizer and reclocker. The low-speed uplink is transmitted with a lower amplitude of 130 mV to limit the crosstalk with the downlink channel.

The downlink channel is intended for NRZ 8b/10b data with bit-rates between 1.25 Gbps and 12.5 Gbps. CoaXPress standard speeds of CXP-1 (1.25 Gbps), CXP-2 (2.5 Gbps), CXP-3 (3.125 Gbps), CXP-5 (5 Gbps), CXP-6 (6.25 Gbps), CXP-10 (10 Gbps) and CXP-12 (12.5 Gbps) are all supported as well as all generic 8b/10b applications.

The low-speed uplink is intended for NRZ 8b/10b data with bit-rates between 20 Mbps and 42 Mbps with a single-ended 1.25V LVTTL input and output. CoaXPress standard speeds of 20.833 Mbps and 41.666 Mbps are supported.

On top of the downlink channel and the low-speed uplink, the system allows power transmission over the coax by using external inductors. These external inductors give the communication channel a high-pass characteristic. The uplink receiver inside the EQCO125X40 chip recovers the signal lost by this high-pass filter. Appropriate inductors should be selected for correct operation of the link. Operation has only been tested with the inductor combination used in Microchip's reference design, even though other components might be suitable.

FIGURE 1-1: TYPICAL EQCO125X40 FAMILY LINK SET-UP

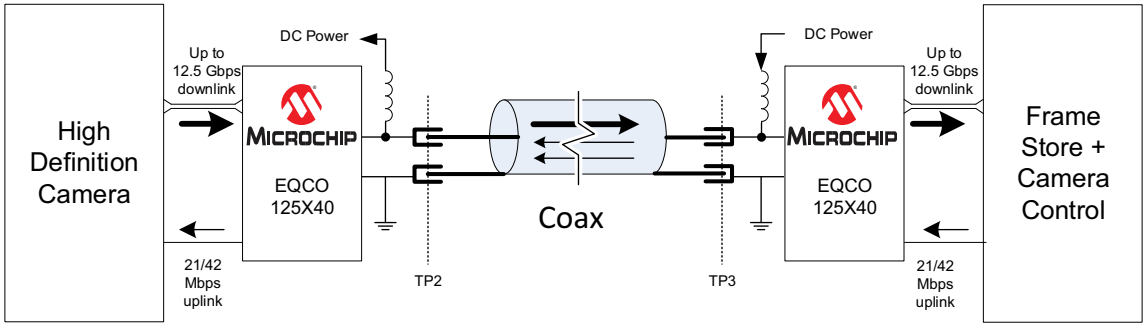


FIGURE 1-2: EQCO125X40 FAMILY BLOCK DIAGRAM SHOWING ELECTRICAL CONNECTIONS

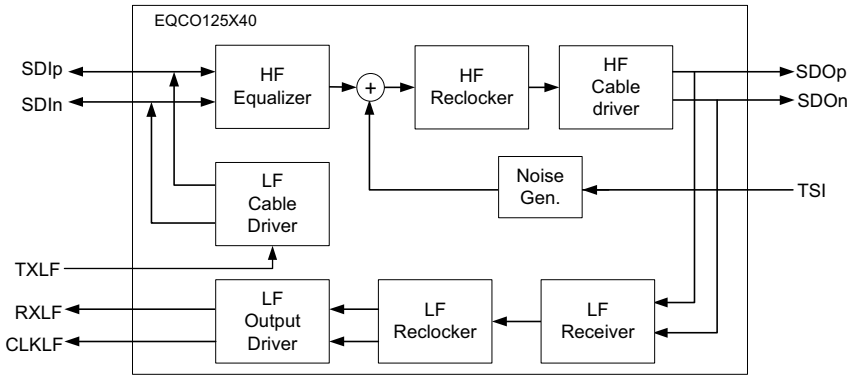


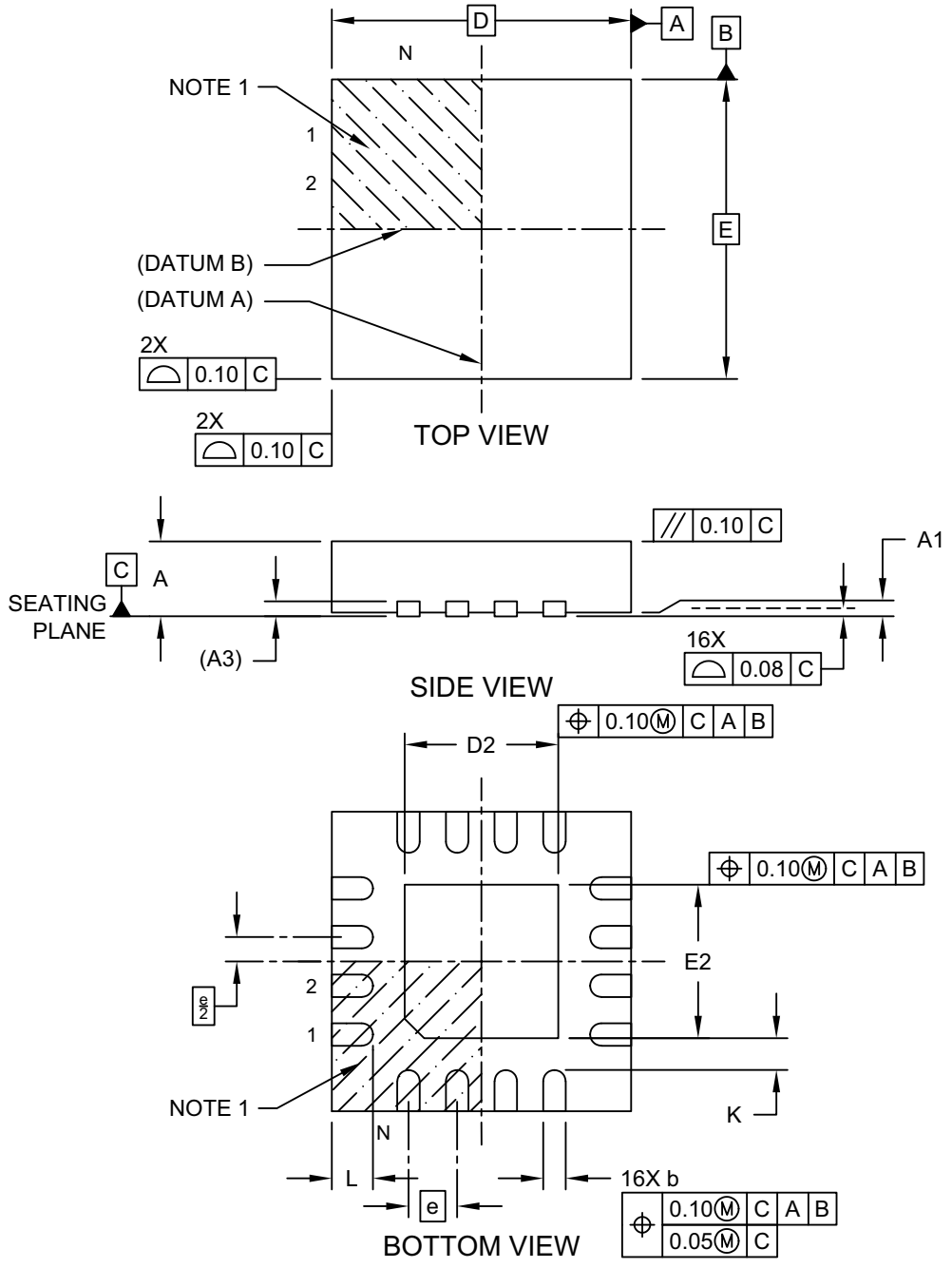
TABLE 1-1: EQCO125X40 FAMILY OF PRODUCTS

Part Number	HF Speed	LF Speed	Device Support	Host Support
EQCO125X40	All CoaXPress speeds up to 12.5 Gbps	20.833 Mbps and 41.666 Mbps	X	X
EQCO125T40	All CoaXPress speeds up to 12.5 Gbps	20.833 Mbps and 41.666 Mbps	X	
EQCO62X20	All CoaXPress speeds up to 6.25 Gbps	20.833 Mbps	X	X
EQCO31X20	All CoaXPress speeds up to 3.125 Gbps	20.833 Mbps	X	X

PACKAGING INFORMATION

16-Lead Plastic Quad Flat, No Lead Package (3DW) - 4x4x1 mm Body [QFN] Exposed Pad 2.05x2.05 mm

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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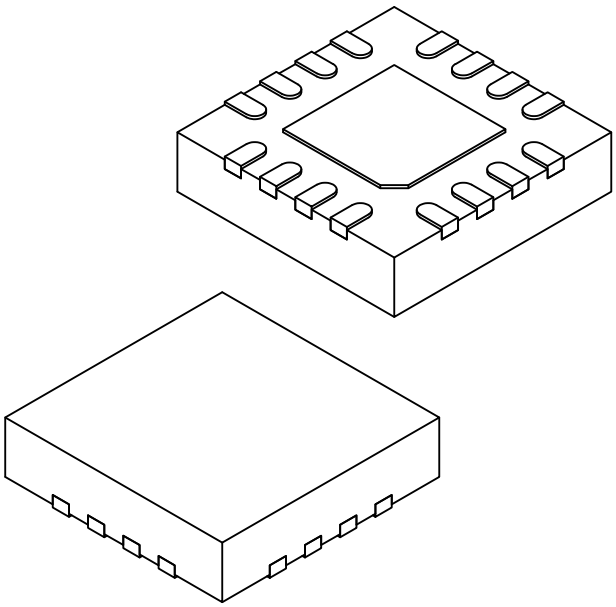

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	1.95	2.05	2.15
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	1.95	2.05	2.15
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.45	0.55	0.65
Terminal-to-Exposed-Pad	K		0.425 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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