PRM™ Regulator

PRM2313S60E54H0T00



High-Efficiency Converter

Features & Benefits

- 48.0V input (38.0 – 60.0V), non-isolated ZVS buck-boost regulator
- 30.0 – 54.0V adjustable output range
- Single-ended remote sense
- 800W output power
- 97.7% typical efficiency at full load
- PRM2313 SM-ChiP package

Typical Applications

- DC Power Distribution
- High-Performance Computing Systems (HPC)

Product Ratings	
V_{IN} = 38.0 – 60.0V	P_{OUT} = 800W
V_{OUT} = 48.0V (30.0 – 54.0V Trim)	I_{OUT} = 16.67A

Product Description

The SM-ChiP™ ZVS Buck-Boost Regulator is a high-efficiency regulator integrating control, power FETs, magnetics and support components within a high density SM-ChiP package. By utilizing a Zero-Voltage Switching (ZVS) topology, the regulator is able to provide a high efficiency over the line and load range for a large step-down voltage range.

Minimal external components are required for operation, making this product ideal for driving high-efficiency non-isolated NBMs to power low-voltage rails to run low-power regulators, LDOs, as well as loads that require precise regulation such as hard drives or bias rails.

The SM-ChiP package is compatible with standard pick-and-place and surface-mount assembly processes. In the application, it provides superior thermal management with simple cooling methods.

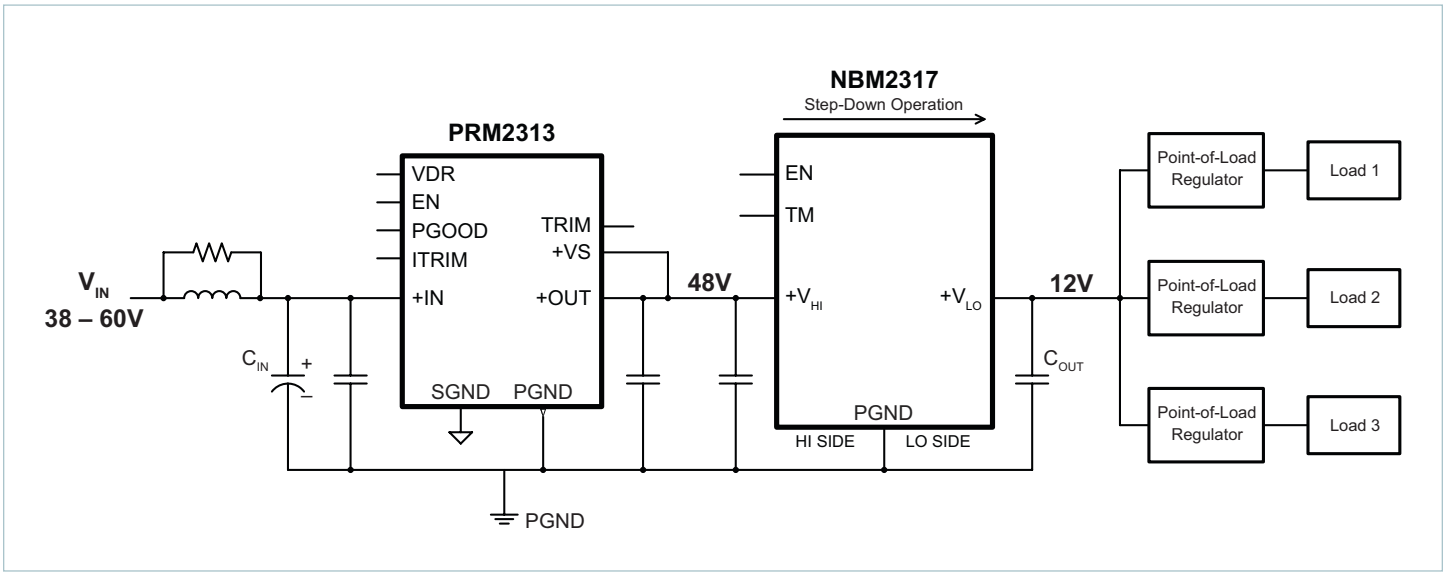
Package Information

- 22.8 x 13.8 x 7.4mm SM-ChiP™
- Weight: 9.0g

Note: Product images may not highlight current product markings and cosmetic features.

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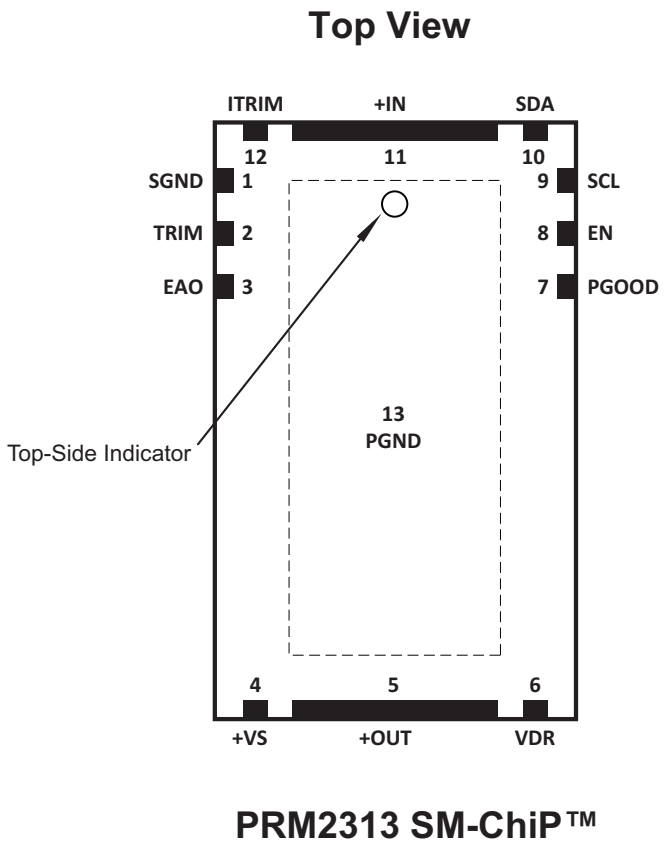
Typical Application



Typical application: 48V to 12V regulator

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Terminal Configuration



Terminal Descriptions

Terminal Number	Signal Name	Type	Function
1	SGND	Signal	**Signal Ground:** reference for control signals; internally connected to PGND
2	TRIM	Signal	**Trim:** output voltage trim adjust
3	EAO	Signal	**Error Amplifier Output:** load-share connection; EAOs are interconnected for parallel operation
4	+VS	Signal	**Voltage Sense:** positive voltage sense; connect to the PRM output
5	+OUT	Power	**Positive Output:** power terminal
6	VDR	Signal	**Bias Supply Output:** see Application Description for important considerations
7	PGOOD	Signal	**Power Good:** Open drain with internal pull-up; high when regulator is operating and V_{OUT} is in regulation, otherwise pulls low
8	EN	Signal	**Enable:** when input asserted active or left floating, regulator is enabled
9	SCL	Signal	Factory use only
10	SDA	Signal	Factory use only
11	+IN	Power	**Positive Input:** power terminal
12	ITRIM	Signal	**Current Trim:** current limit adjust input
13 [c]	PGND	Power	**Power Ground:** power return for +IN and +OUT current

[c] Terminal 13 represents the package top and bottom conductive plating. Refer to product outline for additional details.

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Part Ordering Information

Part Number	Temperature Grade	Option		Tray Size
PRM2313S60E54H0**T**0**0**	**T** = –40 to 125°C	**0** = 48.0V nominal output		66 parts per tray

Storage and Handling Information

Note: For compressive loading refer to Application Note AN:036, "Recommendations for Maximum Compressive Force of Heat Sinks."
For handling and assembly processing, and for rework considerations refer to Application Note AN:701, "SM-ChiP Reflow Soldering Recommendations."

Attribute	Comments	Specification
Storage Temperature Range		–40 to 125°C
Operating Internal Temperature Range (T_{INT})		–40 to 125°C
Weight		9.0g
Package Plating		ENiG: 100 – 300µin Ni, 2 – 5µin Au
MSL Rating		MSL 4, 245°C maximum reflow temperature
ESD Rating	Human Body Model ANSI/ESDA/JEDEC JS-001-2017	Class 1C (>1kV to 2kV) HBM
	Charged Device Model ANSI/ESDA/JEDEC JS-002-2014	Class 1C (>200 to 500V) CDM

Reliability and Agency Approvals

Attribute	Comments	Value	Unit
MTBF	Telcordia Issue 2, Method I Case 3, Gound Benign, Controlled	15.9	MHrs
	MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer Profile	6.84	
Agency Approvals/Standards			
	cTÜVus, UL 62368-1, CAN/CSA No. C22.2 62368-1, EN 62368-1		
	UKCA, electrical equipment (safety) regulations		
	CE Marked to the Low Voltage Directive and RoHS Recast Directive, as applicable		

Absolute Maximum Ratings

The ABSOLUTE MAXIMUM ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to device. Electrical specifications do not apply when operating beyond rated operating conditions. Operating beyond rated operating conditions for an extended period of time may affect device reliability. Positive terminal currents represent current flowing out of the terminal.

Parameter	Comments	Min	Max	Unit
+IN to PGND	Continuous, non-operating	–0.3	75	V
+OUT to PGND	Continuous, non-operating	–0.3	60	V
VDR to SGND		–0.3	5.5	V
			+150 / –0	mA
PGOOD to SGND		–0.3	5.5	V
			±20	mA
EN to SGND		–0.3	5.5	V
SCL to SGND		–0.3	5.5	V
SDA to SGND		–0.3	5.5	V
TRIM to SGND		–0.3	5.5	V
ITRIM to SGND		–0.3	5.5	V
EAO to SGND		–0.3	5.5	V
+VS to SGND		–0.3	60	V
SGND			±0.5	A
Output Current			40	A

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Electrical Specifications

Specifications apply over all line and load conditions, and trim from 30.0 to 54.0V, unless otherwise noted.
Boldface specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specifications						
Input Voltage Range	V_{IN}	Continuous, operating	**38.0**	54.0	**60.0**	V
Input Voltage Slew Rate	dV_{IN}/dt	0V ≤ V_{IN} ≤ 60.0V	**0.001**		**1000**	V/ms
No-Load Power Dissipation	P_{NL}	Enabled, V_{IN} = 54.0V		0.24	**0.400**	W
Input Quiescent Current	I_{QC}	Disabled, V_{IN} = 54.0V		6.9	**10**	mA
Input Capacitance (Internal)	C_{IN_INT}	Effective value, V_{IN} = 54.0V		4.8		µF
Input Capacitance (Internal) ESR	R_{C-IN}	Effective value, V_{IN} = 54.0V		1.0		mΩ
Power Output Specifications						
Output Voltage Set Point	V_{OUT_SET}	No load, no connection to TRIM	**47.7**	48.2	**48.7**	V
Output Voltage Trim Range	V_{OUT}		**30.0**	48.0	**54.0**	V
Output Voltage Load Regulation	$V_{OUT-REG-LOAD}$				**0.3**	%
Output Voltage Line Regulation	$V_{OUT-REG-LINE}$				**0.1**	%
Output Voltage Temperature Regulation	$V_{OUT-REG}$				**2.1**	%
Total Regulation Error	$V_{OUT-REG-TOTAL}$	(Line/Load/Temp regulation and set point accuracy)			**2.5**	%
Rated Output Power	P_{OUT}	V_{OUT} ≥ 48.0V			**800**	W
Rated Output Current	I_{OUT}	V_{OUT} ≤ 48.0V			**16.67**	A
Rated Output Power, Peak	P_{OUT_PK}	V_{OUT} ≥ 48.0V, ≤10ms pulse width, ≤10% duty cycle			**900**	W
Rated Output Current, Peak	I_{OUT_PK}	V_{OUT} ≤ 48.0V, ≤10ms pulse width, ≤10% duty cycle			**18.75**	A
Switching Frequency	F_{SW}	V_{IN} = 54.0V, V_{OUT} = 48.0V, I_{OUT} = 16.67A, T_{INT} = 25°C	**1.225**	1.250	**1.275**	MHz
		Over rated line, average load, trim and temperature, exclusive of burst mode	**0.900**		**1.275**	MHz
Output Turn-On Delay	t_{ON}	From V_{IN} first crossing $V_{IN-UVLO+}$ to soft-start ramp		100		µs
		From EN release to soft-start ramp, V_{IN} pre-applied		100		µs
Output Voltage Rise Time	$t_{RISE-VOUT}$	From soft start begin to V_{OUT} settled to within 5%	**6.0**	8.0	**10.0**	ms
Efficiency, Ambient	η_{AMB}	V_{IN} = 54.0V, V_{OUT} = 48.0V, I_{OUT} = 16.67A, T_{CASE} = 25°C	97.5	98.0		%
		V_{IN} = 54.0V, V_{OUT} = 48.0V, I_{OUT} = 8.3A, T_{CASE} = 25°C	97.2	97.6		%
Efficiency, Hot	η_{HOT}	V_{IN} = 54.0V, V_{OUT} = 48.0 V, I_{OUT} = 16.67A, T_{CASE} = 100°C	97.5	97.9		%
		V_{IN} = 54.0V, V_{OUT} = 48.0 V, I_{OUT} = 8.3A, T_{CASE} = 100°C	97.3	97.6		%
Output Discharge Current	I_{OD}	V_{OUT} > 0.5V, discharge current = CC; otherwise 500Ω resistive	**8**	10	**15**	mA
Output Voltage Ripple	V_{OUT_PP}	V_{IN} = 54.0V, V_{OUT} = 48.0V, I_{OUT} = 16.67A, $C_{OUT-EXT}$ = 0µF, 20MHz BW		2.2		V_{P-P}
Output Inductance (Parasitic)	$L_{OUT-PAR}$	Frequency at 1MHz, simulated terminal model		2.5		nH

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Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, and trim from 30.0 to 54.0V, unless otherwise noted.
Boldface specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specifications (Cont.)						
Output Capacitance (Internal)	$C_{OUT-INT}$	Effective value, V_{OUT} = 48.0V		4.8		µF
Output Capacitance (Internal) ESR	R_{COUT}	Effective value, V_{OUT} = 48.0V		1		mΩ
PRM Load Capacitance (PRM Output)	$C_{LOAD-PRM}$	At PRM output; excludes reflected capacitance from NBM™ output	**0**		**63**	µF
PRM Load Capacitance (Total Effective)	$C_{LOAD-TOTAL_EFF}$	Total effective value at PRM output, including reflected capacitance from NBM output			**130**	µF
12V Load Capacitance (NBM Output)	$C_{LOAD-NBM}$	At K = ¼ NBM out	**0**		**1000**	µF
Load Transient Voltage Deviation	V_{TRANS}	10% <-> 100% load step, 10A/µs, 0µF $C_{OUT-EXT}$, deviation from initial set point		1.6	**3.0**	V
Load Transient Recovery Time	t_{TRANS}	10% <-> 100% load step, 10A/µs, 0µF $C_{OUT-EXT}$, deviation from initial set point		200		µs
Array Operation						
Maximum Array Size		Maximum number of parallel devices			**3**	PRMs
Array De-Rating	$\%_{IOUT_ARRAY}$	Percentage derating from rated current when operated in array as specified	**10**			%
Current Sharing Difference	$\%_{IOUT_SHARE}$	maximum array size, equal input, outptut and EAO voltages at full load; less than 10°C case temperature difference		10	**13**	%
Powertrain Faults						
Input Undervoltage Turn-ON	V_{IN_UVLO+}	Powertrain recovery	**34.0**	35.8	**37.6**	V
Input Undervoltage Hysteresis	$V_{IN_UVLO_HYST}$	$(V_{IN_UVLO+}) – (V_{IN_UVLO–})$	**1.5**	1.8	**2.1**	V
Input Overvoltage Turn-ON	V_{IN_OVLO-}	Powertrain recovery	**62.8**	66.1	**69.4**	V
Input Overvoltage Hysteresis	$V_{IN_OVLO_HYST}$	$(V_{IN_OVLO+}) – (V_{IN_OVLO–})$		1.3		V
Output Overvoltage Turn-OFF Threshold	V_{OUT_OVT}	Rising threshold, powertrain shut down	**56.8**	57.9	**60.0**	V
Output Overvoltage Hysteresis	V_{OUT_OVH}			1.2		V
Minimum Current-Limited Output Voltage	V_{OUT_UVP}				**8**	V
Output Overcurrent Shut Down (Slow)	I_{OUT_SCL}	10µs time constant	**20.6**			A
Controller Programmed Temperature Shut Down [a]	T_{CSD}	Detected at control IC	**125**			°C
EAO Overload Limit	V_{EAO_OL}		**3.18**	3.30	**3.43**	V
EAO Overload Timeout	t_{OL}	EAO continuously above EAO_LIMIT	**900**	1024	**1100**	µs
Trim Voltage Overvoltage Threshold	V_{TRIM_OV}	$V_{TRIM} > V_{TRIM_OV}$	1.94	2.04	2.14	V
Output Voltage Negative Fault Threshold	V_{OUT_NEG}		**–0.45**	–0.25	**–0.15**	V
Fault Response Time	t_{PROT}	OVLO, UVLO, ENABLE, OTP, TRIM_OV		2.0		µs
Fault Recovery Time	$t_{PROT-RECOVERY}$	OVLO, UVLO, OTP		30		ms

[a] Programmed temperature shutdown does not protect the device, and exceeding the maximum Internal Operating Temperature can lead to failure. Users should utilize the thermal tools provided in the datasheet to maintain maximum internal temperature within the Operating Temperature range.

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Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, and trim from 30.0 to 54.0V, unless otherwise noted.
Boldface specifications apply over the temperature range of –40°C ≤ T_{INT} ≤ 125°C. All other specifications are at T_{INT} = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
VDR						
VDR Voltage	V_{VDR}	Internally Generated	**4.84**	5.1	**5.36**	V
VDR Input Undervoltage Turn-On	$V_{IN_VDR_UVLO+}$		**6.6**	6.9	**7.2**	V
VDR Turn-On Hysteresis	$V_{IN_VDR_UVLO_HYST}$			0.5		V
VDR Turn-On Delay	t_{ON_VDR}	V_{IN} start from < 1V, V_{IN} > $V_{IN_VDR_UVLO+}$ to VDR high		5.8		ms
VDR Start-Up Current	I_{VDR_STDBY}	Available source current during start up, VDR low			**10**	mA
VDR Source Current	I_{VDR_ON}	Available source current, VDR high, after t_{ON_VDR}			**80**	mA
Enable: EN						
Enable Internal Pull-Up Voltage		Floating, no external pull up		2		V
Enable Bias Current	I_{EN}			50		µA
Enable High Threshold	EN_{IH}				**1.1**	V
Enable Low Threshold	EN_{IL}		**0.7**			V
Enable Threshold Hysteresis	EN_{HYS}		**100**	200	**300**	mV
Power Good: PGOOD						
PGOOD High Leakage	$PGOOD_{ILH}$	V_{PGOOD} = V_{VDR}			10	µA
PGOOD Output Low	$PGOOD_{OL}$	I_{PGOOD} = 4mA			0.4	V
PGOOD TRIM Low Rise		TRIM threshold for PGOOD High	1.41	1.45	1.48	V
PGOOD TRIM Low Fall		TRIM threshold for PGOOD Low	1.36	1.41	1.46	V
PGOOD TRIM Threshold Hysteresis				35		mV
Transconductance Error Amplifier						
Voltage at V_{TRIM} (Reference Voltage)	V_{TRIM}	Voltage reference, V_{TRIM} = V_{EAO}	**1.67**	1.70	**1.73**	V
Maximum EAO Output Voltage	V_{EAO_MAX}		**3.5**	3.6	**4.0**	V
Minimum EAO Output Voltage	V_{EAO_MIN}			0.05	**0.15**	V
V_{EAO} Pulse Skip Threshold	V_{EAO_PST}	Powertrain stops switching		0.6		V
Transconductance	gm_{EAO}	Factory set		2.3		mS
EAO Current Sourcing	I_{EAO_OUT}			370		µA
EAO Current Sinking	I_{EAO_SINK}			330		µA
Current Limit: ITRIM						
ITRIM Threshold Voltage	V_{ITRIM_SET}	No connection to ITRIM	**1.05**	1.075	**1.100**	V
Output Current Limit Set Point	I_{LIMIT_CC}	Constant current limit, no connection to ITRIM; see applications section for important information on using ITRIM	**29**	30.5	**32.0**	A
Effective Internal Current Sense Gain	G_{ISENSE}	Current llmit active, V_{ITRIM} / I_{OUT}, I_{OUT} > 40% rated load	**31.5**	35	**38.5**	mV / A
I_{LIMIT} Range	I_{LIMIT_RANGE}	Permitted current limit set range	**4**		**16.67**	A
Output Current Limit Response Time	t_{ILIMIT_CC}	Detection to recovery to within 1% of current limit set point		12		ms

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Specified Operating Area

The following figures present performance data in a typical application environment.

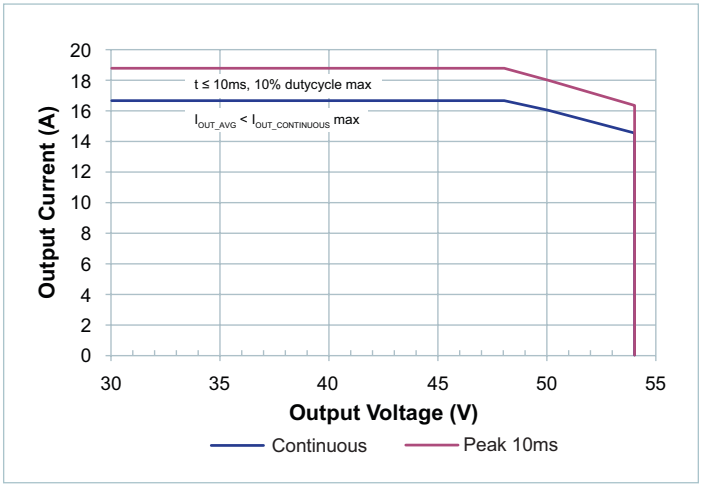


Figure 1 — *Specified operating area vs. output voltage*

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Thermal Operating Area

The following figures present performance data in a typical application environment.

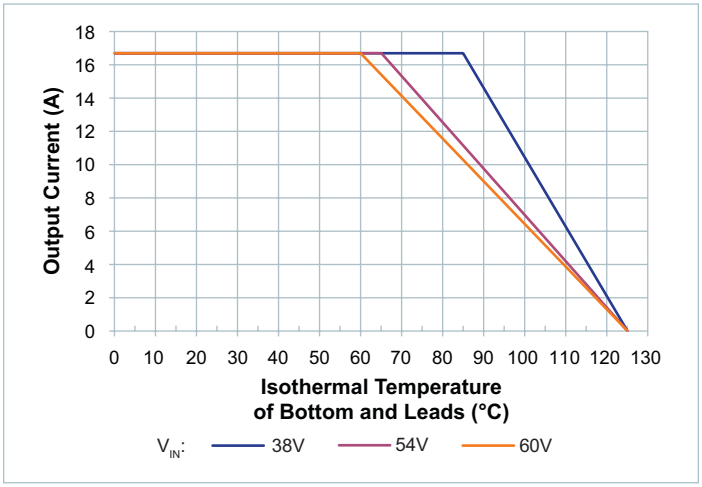


Figure 2 — *Thermal specified operating area at V_{OUT} = 30V: max system I_{OUT} vs. temperature at bottom and leads*

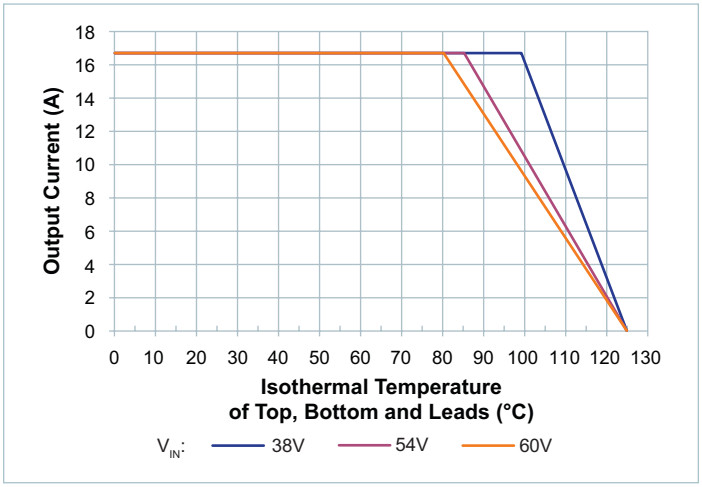


Figure 3 — *Thermal specified operating area at V_{OUT} = 30V: max system I_{OUT} vs. temperature, at top, bottom and leads*

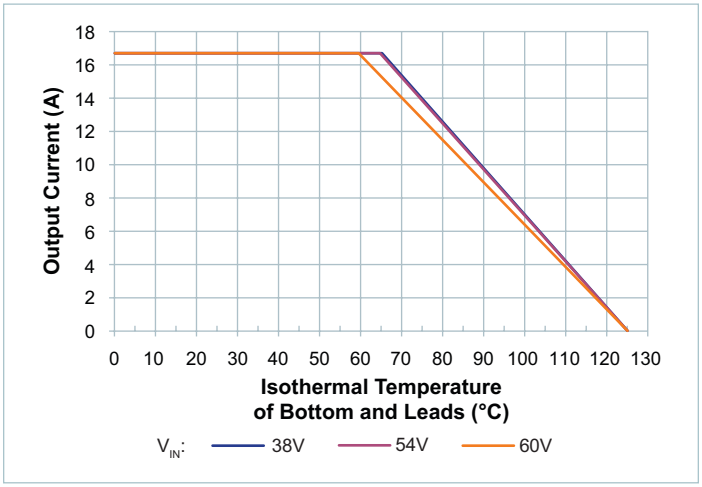


Figure 4 — *Thermal specified operating area at V_{OUT} = 48V: max system I_{OUT} vs. temperature at bottom and leads*

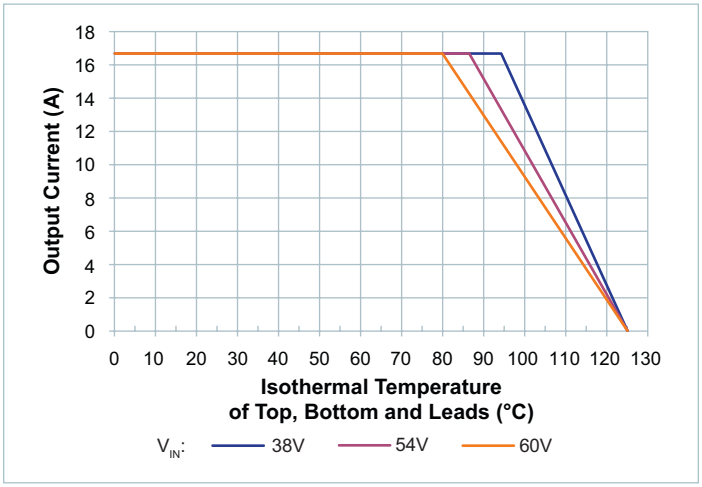


Figure 5 — *Thermal specified operating area at V_{OUT} = 48V: max system I_{OUT} vs. temperature, at top, bottom and leads*

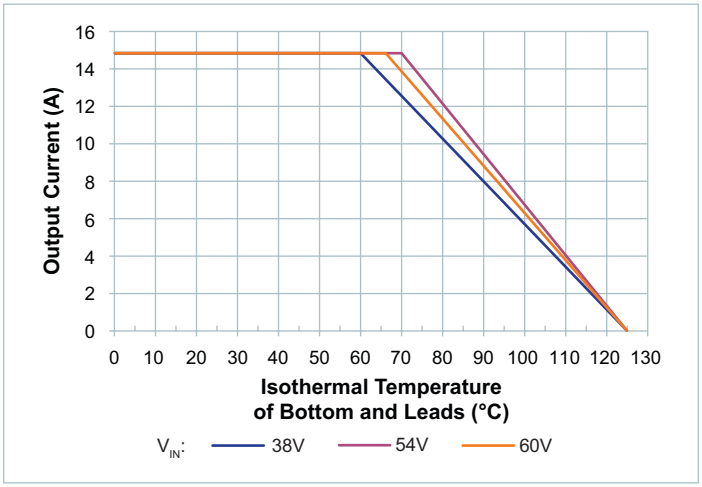


Figure 6 — *Thermal specified operating area at V_{OUT} = 54V: max system I_{OUT} vs. temperature at bottom and leads*

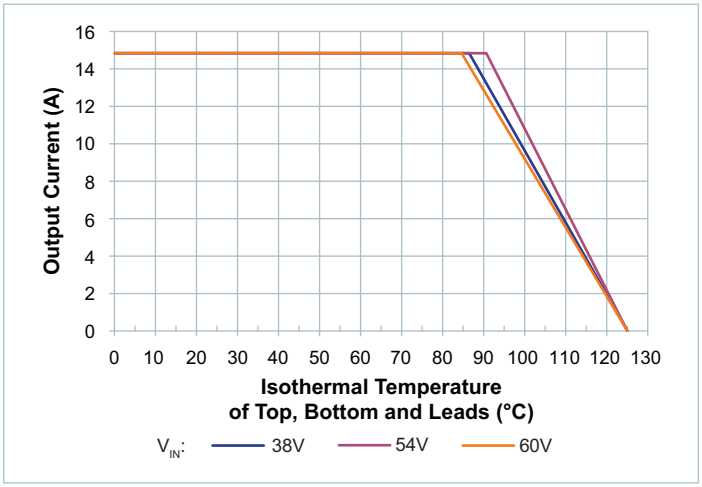


Figure 7 — *Thermal specified operating area at V_{OUT} = 54V: max system I_{OUT} vs. temperature, at top, bottom and leads*

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Typical Performance Characteristics

The following figures present performance data in a typical application environment.

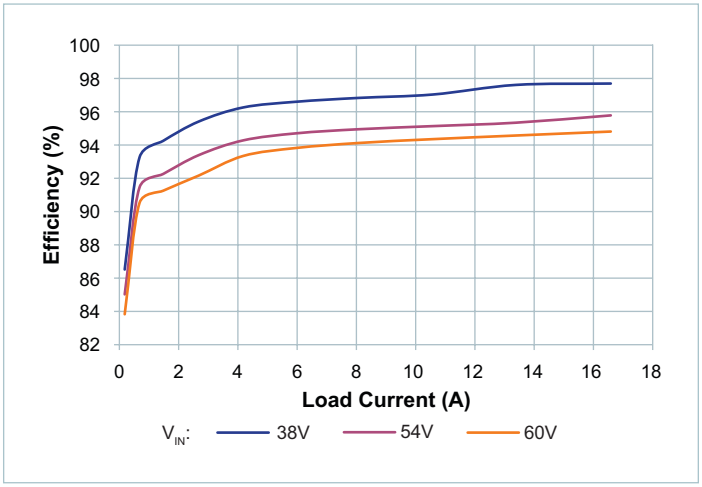


Figure 8 — *Efficiency at 25°C case temperature, V_{OUT} = 30.0V*

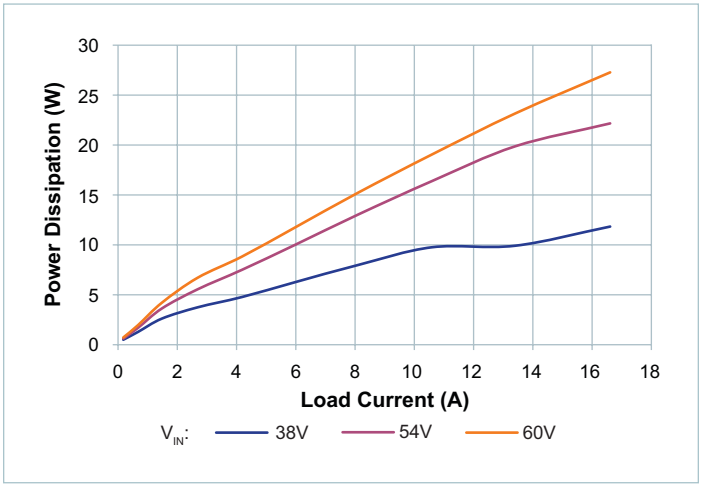


Figure 9 — *Power dissipation at 25°C case temperature, V_{OUT} = 30.0V*

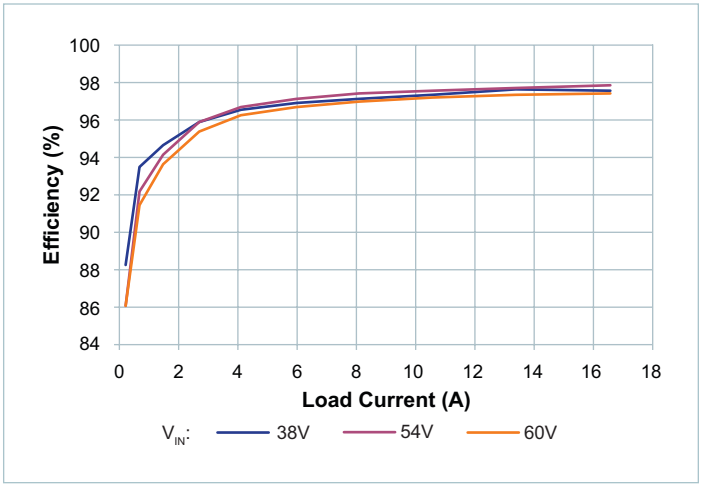


Figure 10 — *Efficiency at 25°C case temperature, V_{OUT} = 48.0V*

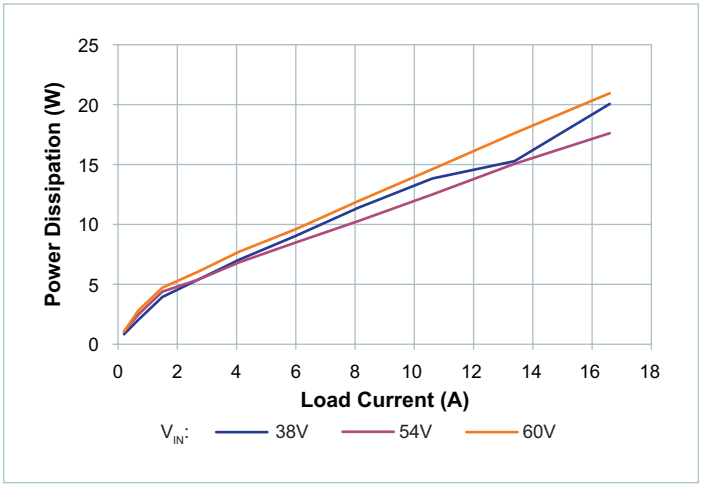


Figure 11 — *Power dissipation at 25°C case temperature, V_{OUT} = 48.0V*

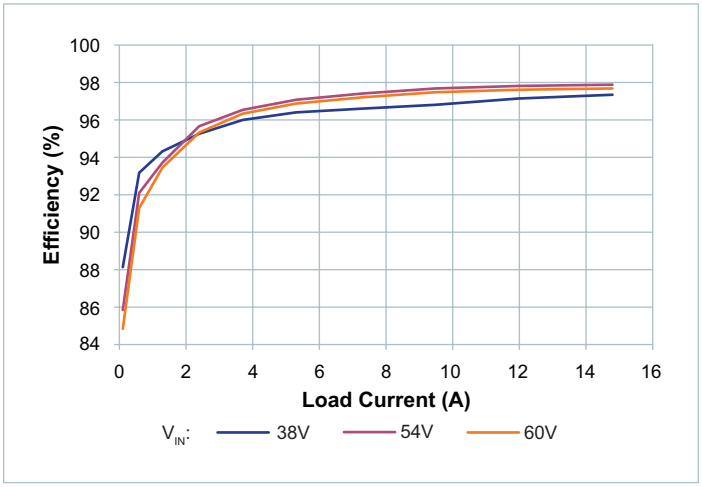


Figure 12 — *Efficiency at 25°C case temperature, V_{OUT} = 54.0V*

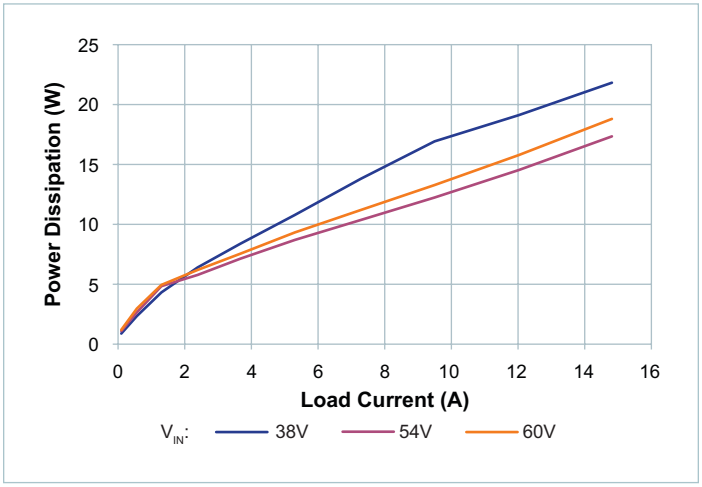


Figure 13 — *Power dissipation at 25°C case temperature, V_{OUT} = 54.0V*

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Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

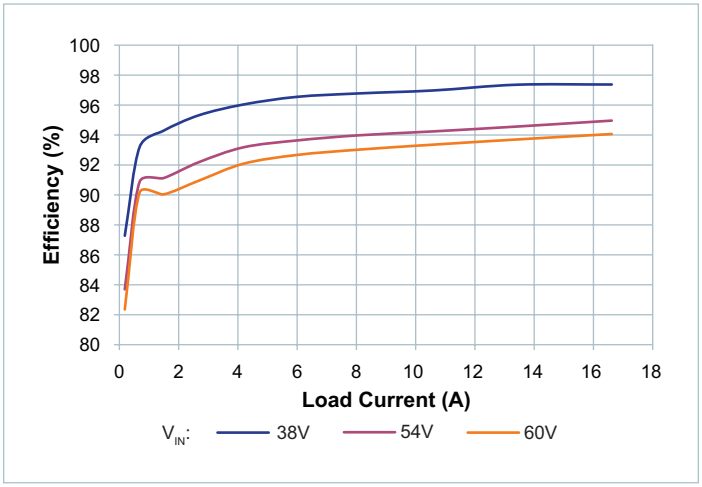


Figure 14 — *Efficiency at –40°C case temperature, V_{OUT} = 30.0V*

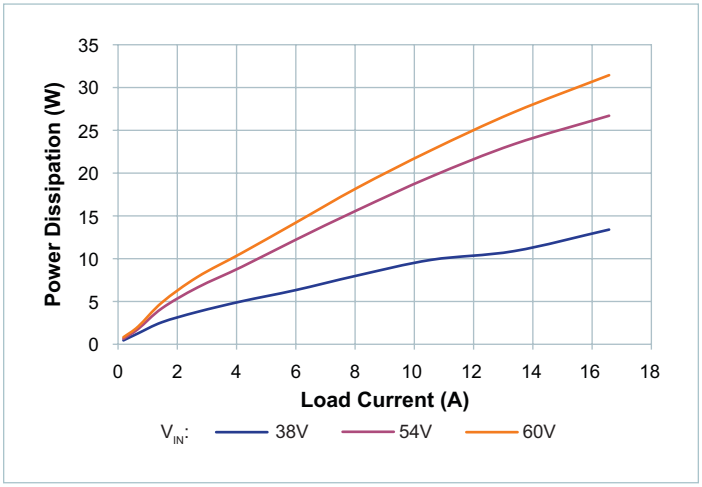


Figure 15 — *Power dissipation at –40°C case temperature, V_{OUT} = 30.0V*

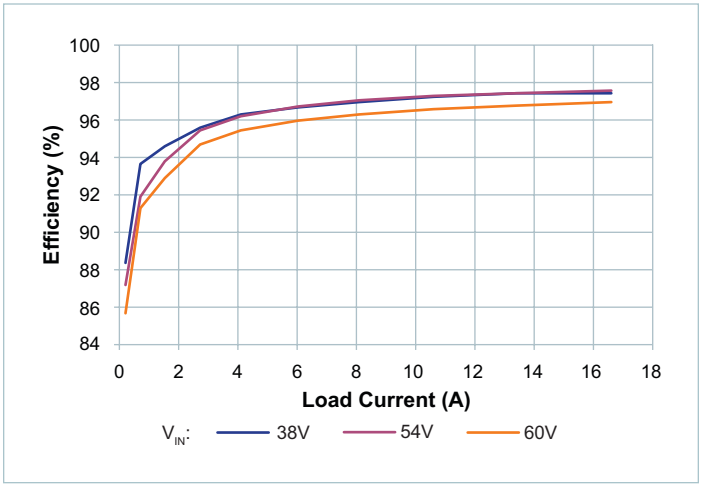


Figure 16 — *Efficiency at –40°C case temperature, V_{OUT} = 48.0V*

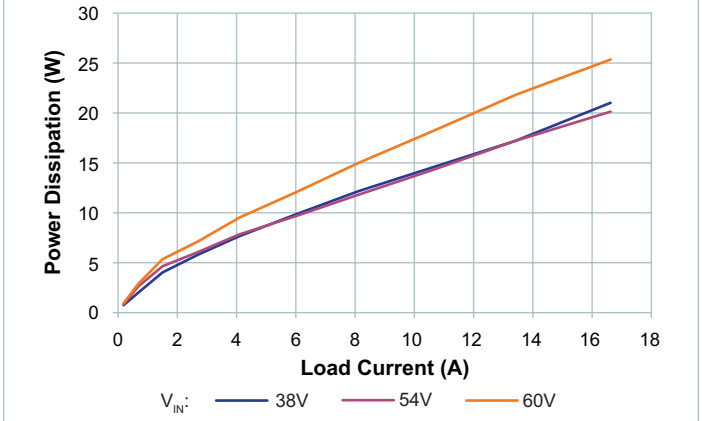


Figure 17 — *Power dissipation at –40°C case temperature, V_{OUT} = 48.0V*

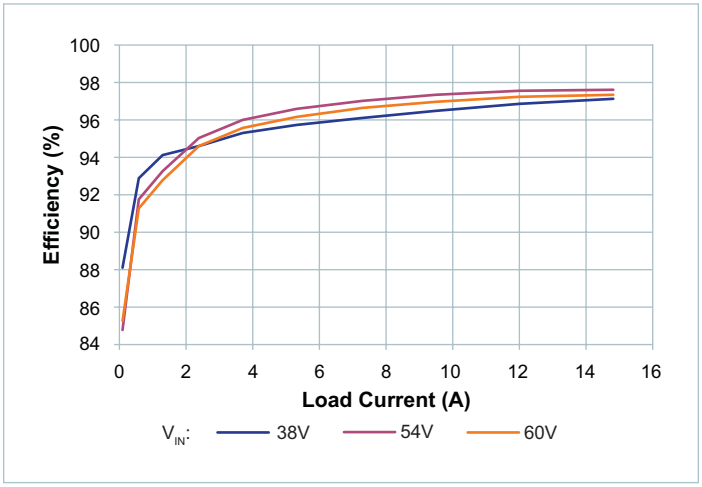


Figure 18 — *Efficiency at –40°C case temperature, V_{OUT} = 54.0V*

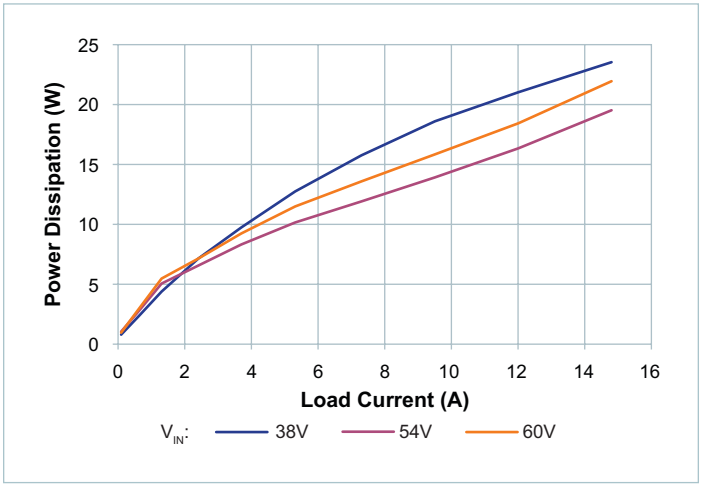


Figure 19 — *Power dissipation at –40°C case temperature, V_{OUT} = 54.0V*

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Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

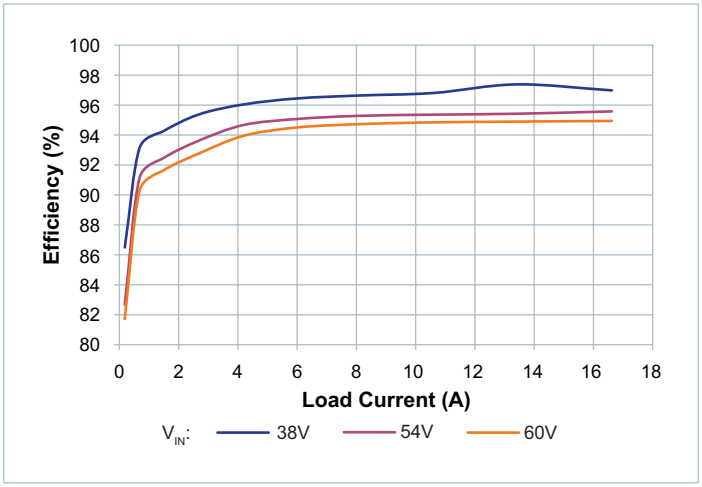


Figure 20 — *Efficiency at 100°C case temperature, V_{OUT} = 30.0V*

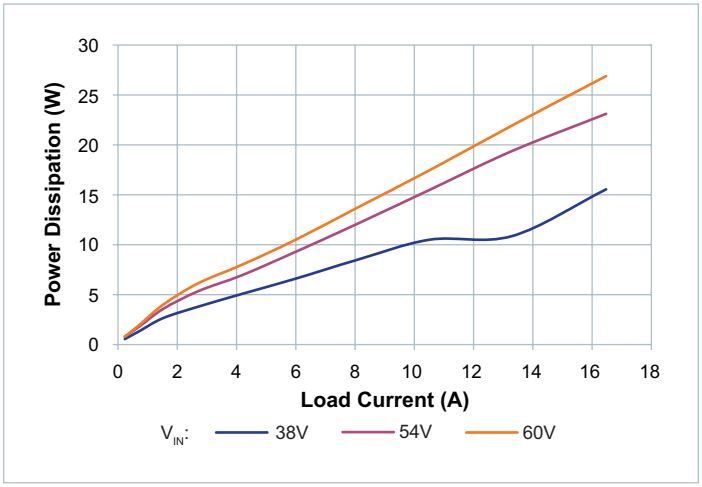


Figure 21 — *Power dissipation at 100°C case temperature, V_{OUT} = 30.0V*

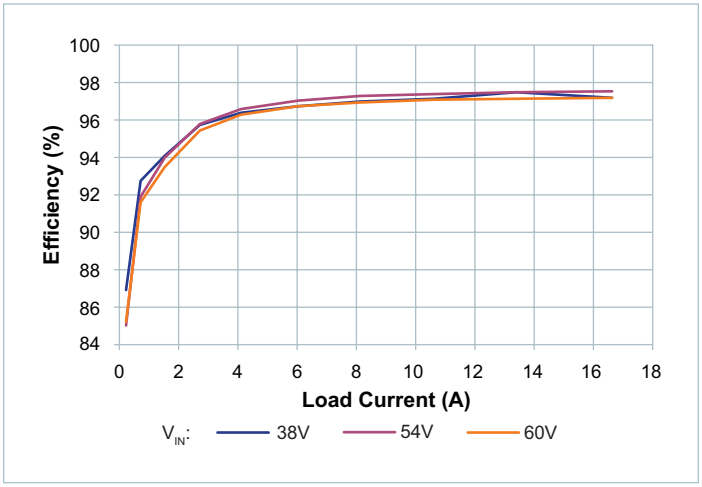


Figure 22 — *Efficiency at 100°C case temperature, V_{OUT} = 48.0V*

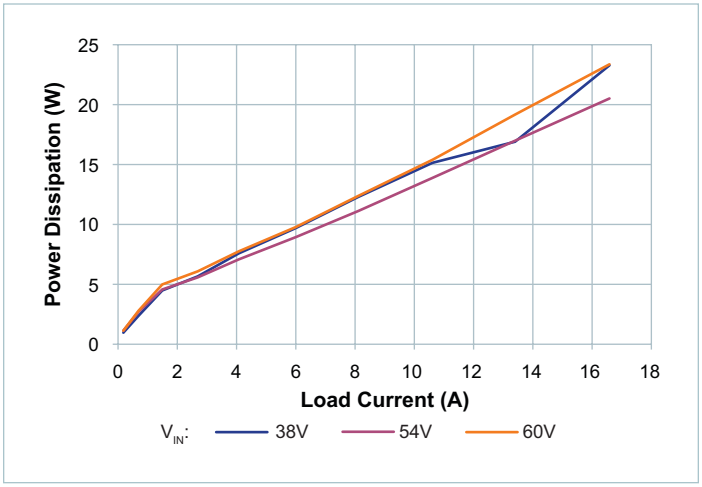


Figure 23 — *Power dissipation at 100°C case temperature, V_{OUT} = 48.0V*

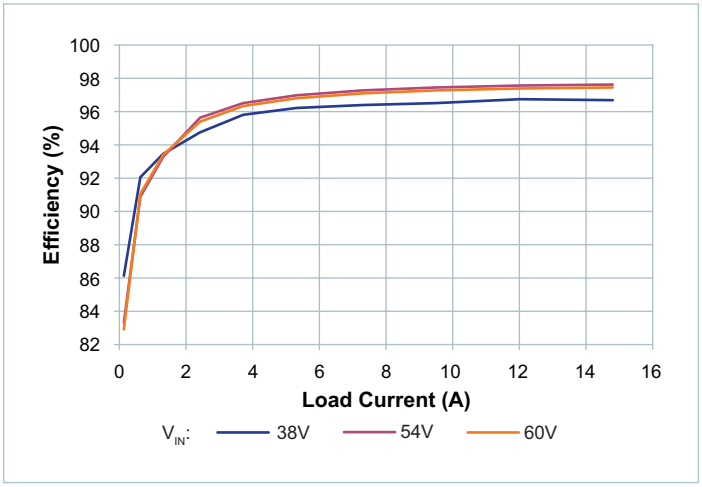


Figure 24 — *Efficiency at 100°C case temperature, V_{OUT} = 54.0V*

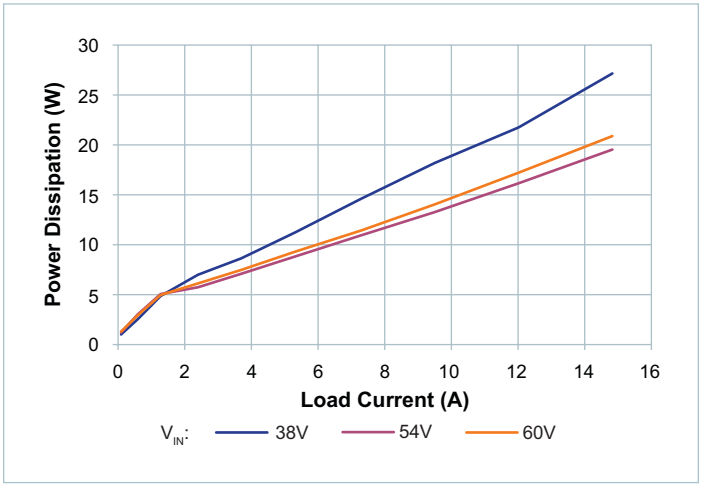


Figure 25 — *Power dissipation at 100°C case temperature, V_{OUT} = 54.0V*

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Typical Performance Characteristics (Cont.)

The following figures present performance data in a typical application environment.

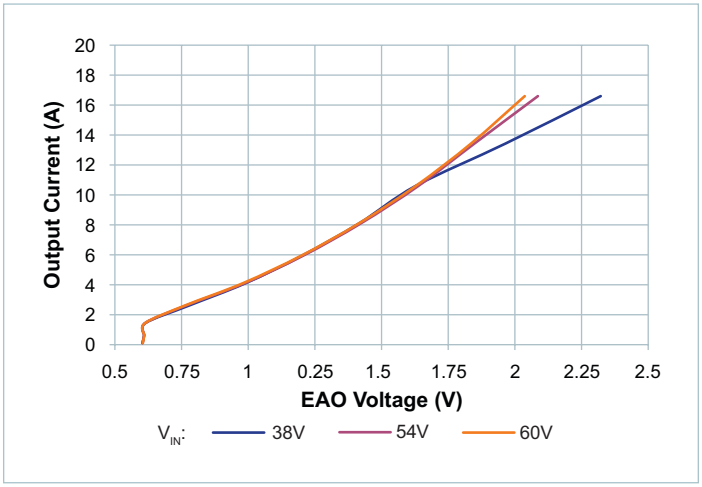


Figure 26 — *Output current vs. EAO voltage at 25°C case temperature, V_{OUT} = 30.0V*

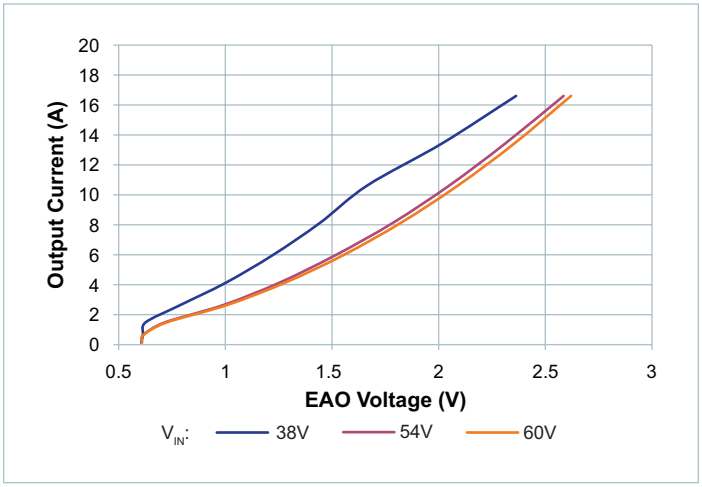


Figure 27 — *Output current vs. EAO voltage at 25°C case temperature, V_{OUT} = 48.0V*

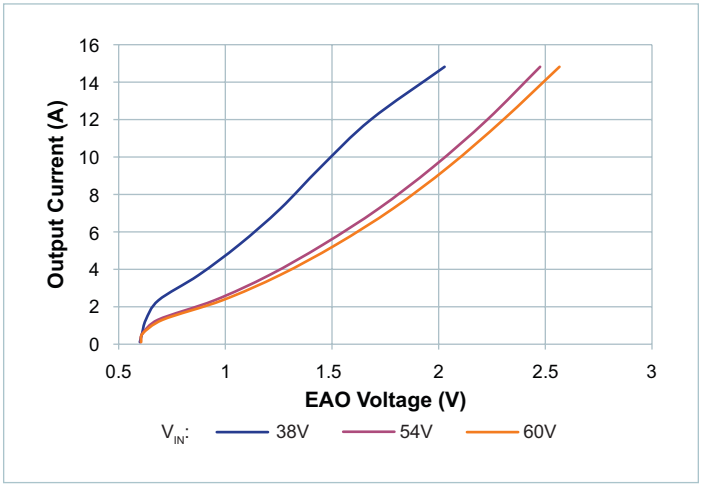


Figure 28 — *Output current vs. EAO voltage at 25°C case temperature, V_{OUT} = 54.0V*

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Terminal Descriptions

VDR Bias Regulator

The VDR internal bias regulator is an internally-generated 5V supply, which is intended primarily to power the internal controller and driver circuitry. VDR can be loaded up to I_{VDR_ON} once the device has completed start up. During start up the load on VDR must be limited to I_{VDR_STDBY}.

+IN – Input Power

The +IN terminal is the power rail input to the PRM. External filtering and decoupling techniques are application-specific. Low-ESR ceramic capacitors are recommended at the input terminal to power ground.

EAO – Modulator

EAO is the error amplifier output and is used for current sharing when parts are operated in an array.

The error amplifier is a wide-bandwidth Transconductance Amplifier (TCA). Here it is important to note that the compensation components are pre-programmed by the factory and are internal to the device.

EN – Enable

The EN terminal of the regulator is referenced to SGND and permits the user to turn the regulator on or off. The EN polarity is a positive logic assertion.

If the EN terminal is left floating or asserted high, the regulator output is enabled. When EN is asserted low, the regulator will complete the current switching cycle and enter a low-power state until EN is released.

PGOOD – Power Good

The PGOOD terminal functions as a power-good indicator. PGOOD is high when the regulator is operating and V_{OUT} is within regulation; otherwise it pulls low.

ITRIM – Current Trim

ITRIM sets the constant current limit set point.

By default constant current limit is set outside of the device ratings and a resistor must be placed from ITRIM to SGND to bring the current limit set point within the permitted current limit range. The current limit set point must be set below the rated current of the device and above the pulse-skip threshold current if used.

+VS – Positive Voltage Sense

+VS is the positive voltage sense and connects the internal voltage sense divider to the desired voltage sense location. +VS is not internally connected and a connection must be made to the PRM output.

TRIM

TRIM is the internal error amplifier inverting terminal. The output voltage is set by internal resistors, but can be adjusted by external resistors connected to TRIM.

SCL, SDA

For factory use only.

SGND – Signal Ground

SGND provides an internal Kelvin connection to PGND. SGND must be used as the reference for all signal and control terminals.

PGND

PGND is the common power return.

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Thermal Design

Thermal management of PRM internal power dissipation is critical to reliable operation, and ample cooling is preferred since efficiency and reliability are better at lower internal temperatures. Figure 29 shows a thermal impedance model that can estimate the maximum temperature of the highest temperature component for a given electrical and thermal operating condition.

The circuit model assumes each of those areas identified as thermal boundaries are isothermal although not necessarily the same temperature as the other boundary areas. Use of non-conductive TIM (Thermal Interface Material) is required to prevent shorting conductive surfaces on case.

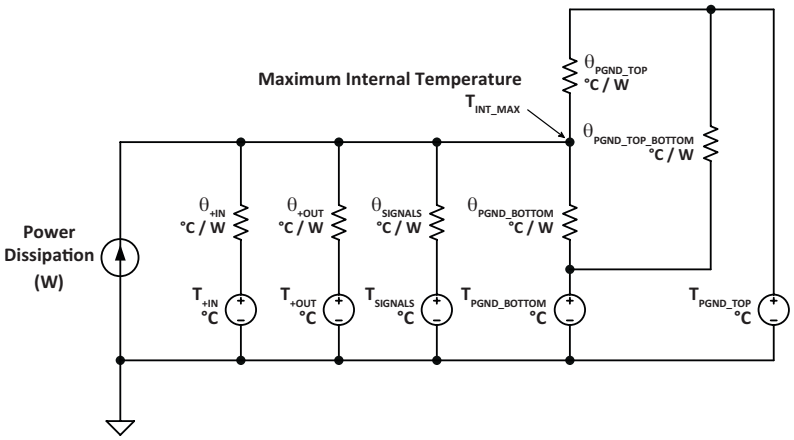


Figure 29 — *Thermal model*

Symbol	Thermal Impedance (°C / W)	Definition of Estimated Thermal Resistance
θ_{PGND_TOP}	3.6	from the hottest component inside the PRM to the top PGND terminal
θ_{+IN}	57	from the hottest component inside the PRM to the circuit board it is mounted on at the +IN terminal
θ_{+OUT}	61	from the hottest component inside the PRM to the circuit board it is mounted on at the +OUT terminal
$\theta_{SIGNALS}$	23	from the hottest component inside the PRM to the circuit board it is mounted on at the SIGNAL terminals
θ_{PGND_BOTTOM}	3.9	from the hottest component inside the PRM to the circuit board it is mounted on at the PGND THERMAL AND ELECRICAL PAD
$\theta_{PGND_TOP_BOTTOM}$	17	between the top PGND terminal and the PGND THERMAL AND ELECTRICAL PAD

Table 1 — *Thermal impedances*

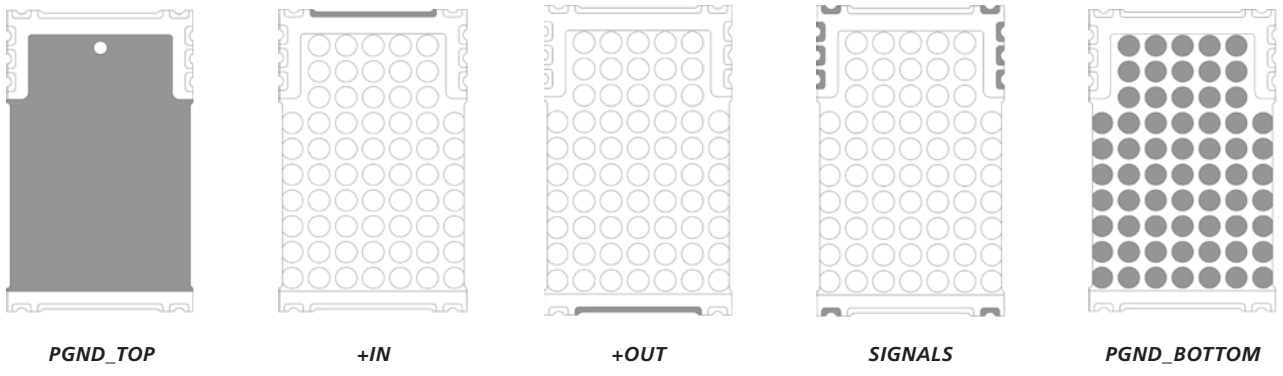
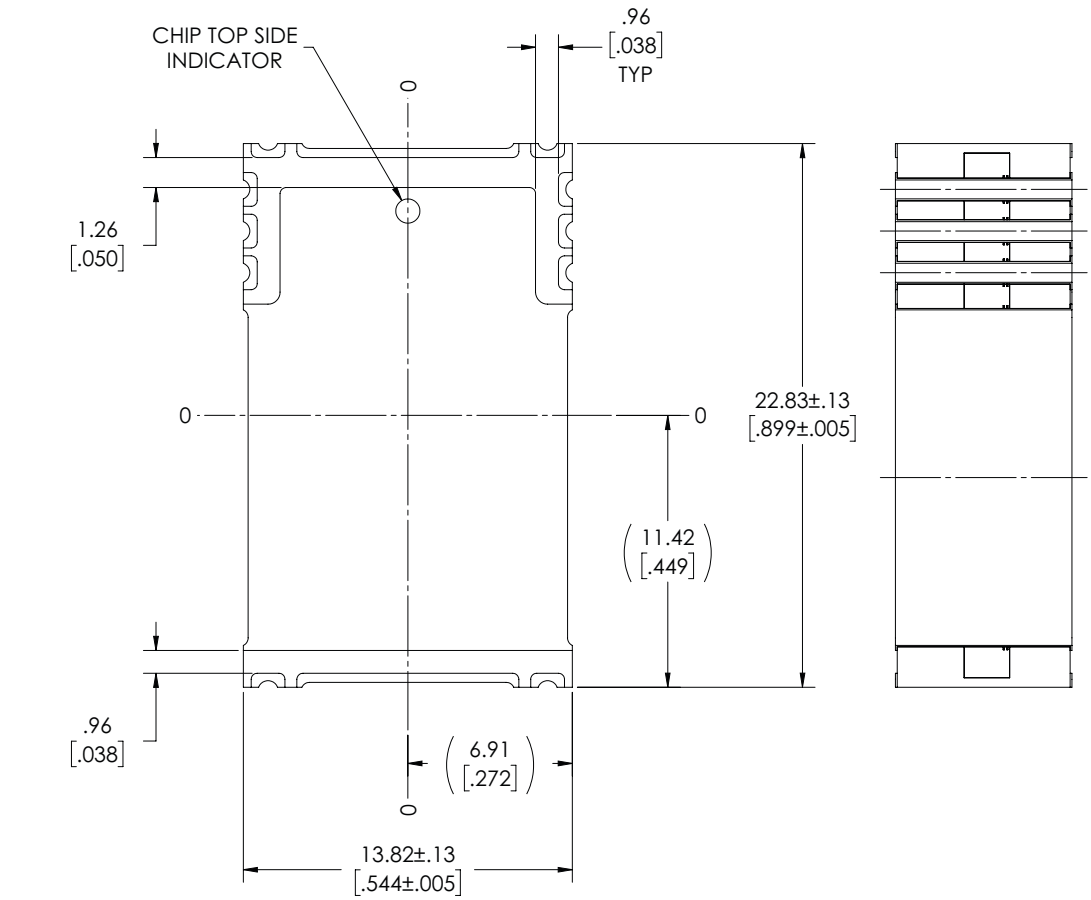


Figure 30 — *Thermal model boundary conditions; area defined as shaded*

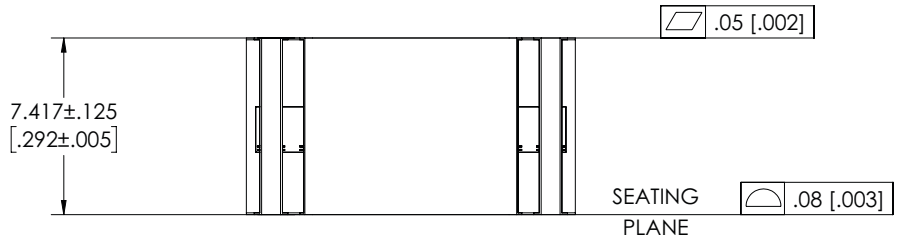
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Outline Drawing Top & Side View

2313 PRM TC2_3
(Reference DWG # 47574 Rev 4)



TOP VIEW (COMPONENT SIDE)

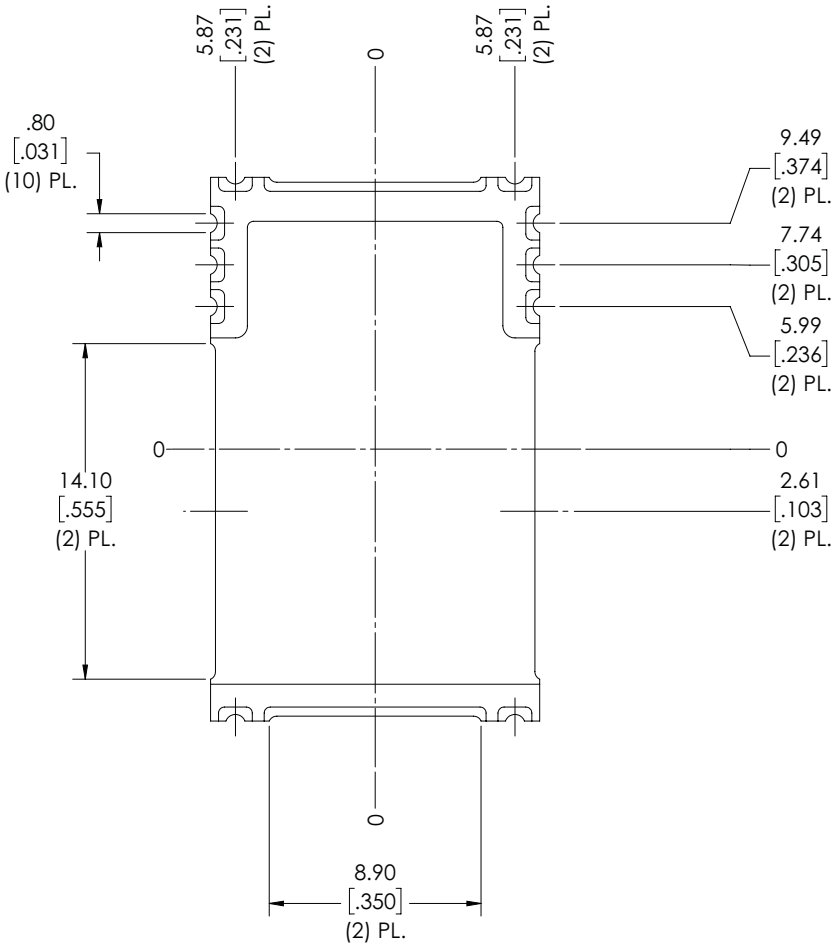


NOTES:
1- UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MM [INCH]
2- TOLERANCES ARE:
DECIMALS
X.XX [X.XX] = ±0.25 [0.01]
X.XXX [X.XXX] = ±0.127 [0.005]
ANGLES = ±1°

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Outline Drawing Bottom View

2313 PRM TC2_3
(Reference DWG # 47574 Rev 4)

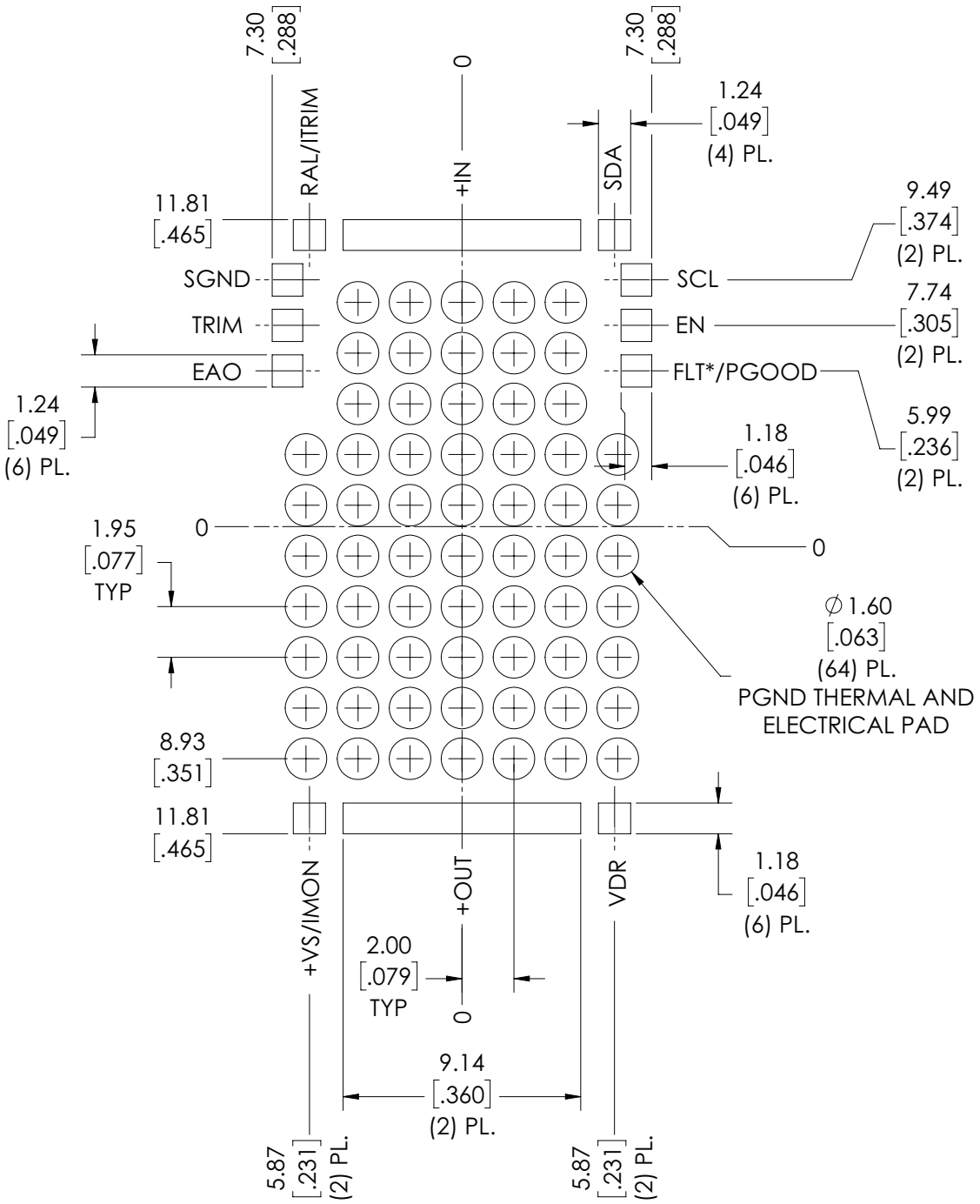


BOTTOM VIEW

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Recommended Land Pattern (Component Side)

2313 PRM TC2_3
(Reference DWG # 47574 Rev 4)



RECOMMENDED LAND PATTERN
(COMPONENT SIDE)

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Revision History

Revision	Date	Description	Page Number(s)
1.0	01/07/19	Initial release	n/a
1.1	02/20/20	Corrected absolute maximum ratings for +OUT to PGND, +VS to SGND Added output overvoltage turn off specification	4 6
1.2	03/17/20	Corrected $\overline{\text{FLT}}$ terminal name to PGOOD Added PGOOD electrical specifications and description Updated thermal operating area bottom+leads charts	2, 3, 4, 19 7, 15 9
1.3	12/01/21	Updated and revised format of storage & handling, reliability and agency approvals Updated absolute max rating for +IN Updated orientation of terminal configuration, thermal boundaries, outline drawing	1, 4 4 3, 15, 16, 17, 18
1.4	12/20/24	Updated agency approvals Updated power and current rating notes/conditions	1, 4 5

Note: page removed in revision 1.3.

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