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REVISION HISTORY

6/04—Data Sheet Changed from Rev. 0 to Rev. A

Updated Format.....	Universal
Changes to Table 1 .....	3
Changes to Thermal Overload Protection Section .....	10
Updated Outline Dimensions .....	12
Changes to Ordering Guide .....	12

10/01—Revision 0: Initial Version

## SPECIFICATIONS<sup>1, 2</sup>

$V_{IN} = 6.0\text{ V}$ ,  $C_{IN} = C_{OUT} = 1\text{ }\mu\text{F}$ ,  $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise noted.

**Table 1.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
OUTPUT							
Voltage Accuracy <sup>3</sup>	V <sub>OUT</sub>	V <sub>IN</sub> = V <sub>OUTNOM</sub> + 0.5 V to 6 V, I <sub>L</sub> = 0.1 mA to 1.5 A, T <sub>J</sub> = 25°C	−0.9		+0.9	%	
		V <sub>IN</sub> = V <sub>OUTNOM</sub> + 0.5 V to 6 V, I <sub>L</sub> = 0.1 mA to 1.5 A, T <sub>J</sub> = −40°C to +125°C	−1.5		+1.5	%	
		V <sub>IN</sub> = V <sub>OUTNOM</sub> + 0.5 V to 6 V, I <sub>L</sub> = 100 mA to 1.5 A, T <sub>J</sub> = 150°C	−1.9		+1.9	%	
Line Regulation	V <sub>DROP</sub>	V <sub>IN</sub> = V <sub>OUTNOM</sub> + 0.5 V to 6 V, T <sub>J</sub> = 25°C		0.04		mV/V	
Load Regulation		I <sub>L</sub> = 0.1 mA to 1.5 A, T <sub>J</sub> = 25°C		0.004		mV/mA	
Dropout Voltage		V <sub>OUT</sub> = 98% of V <sub>OUTNOM</sub>					
		I <sub>L</sub> = 1.5 A		230	480	mV	
		I <sub>L</sub> = 1 A		180	380	mV	
		I <sub>L</sub> = 500 mA		150	300	mV	
		I <sub>L</sub> = 100 mA		100		mV	
Peak Load Current	I <sub>LDPK</sub>	V <sub>IN</sub> = V <sub>OUTNOM</sub> + 1 V		2.0		A	
Output Noise	V <sub>NOISE</sub>	f = 10 Hz–100 kHz, C <sub>L</sub> = 10 μF, I <sub>L</sub> = 1.5 A		95		μV rms	
GROUND CURRENT							
In Regulation	I <sub>GND</sub>	I <sub>L</sub> = 1.5 A		13	40	mA	
		I <sub>L</sub> = 1 A		9	25	mA	
		I <sub>L</sub> = 500 mA		5	15	mA	
		I <sub>L</sub> = 100 mA		1	3	mA	
		I <sub>L</sub> = 0.1 mA		130	200	μA	
In Dropout	I <sub>GND</sub>	V <sub>IN</sub> = V <sub>OUTNOM</sub> − 100 mV, I <sub>L</sub> = 0.1 mA		100	300	μA	

<sup>1</sup> All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC) methods.

<sup>2</sup> Application stable with no load.

<sup>3</sup>  $V_{IN} = 2.8\text{ V}$  for models with  $V_{OUTNOM} \leq 2.3\text{ V}$ .

## ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified, all voltages are referenced to GND.

**Table 2.**

Parameter	Rating
Input Supply Voltage	–0.3 V to +8.5 V
Power Dissipation	Internally Limited
Operating Ambient Temperature Range	–40°C to +85°C
Operating Junction Temperature Range	–40°C to +150°C
$\theta_{JA}$ Four-Layer Board	62.3°C/W
$\theta_{JC}$	26.8°C/W
Storage Temperature Range	–65°C to +150°C
Lead Temperature Range (Soldering 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

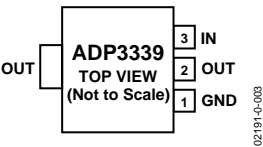
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTE: PIN 2 AND TAB ARE INTERNALLY CONNECTED

Figure 3. 3-Lead SOT-223 Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	GND	Ground Pin.
2	OUT	Output of the Regulator. Bypass to Ground with a 1 $\mu$ F or larger capacitor.
3	IN	Regulator Input. Bypass to Ground with a 1 $\mu$ F or larger capacitor.

## TYPICAL PERFORMANCE CHARACTERISTICS

TA = 25°C unless otherwise noted.

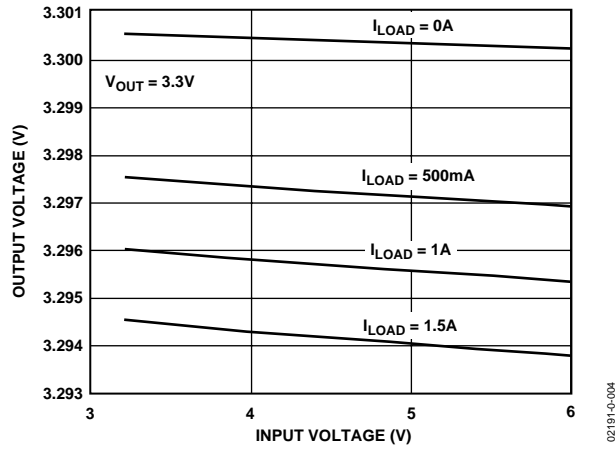


Figure 4. Output Voltage vs. Input Voltage

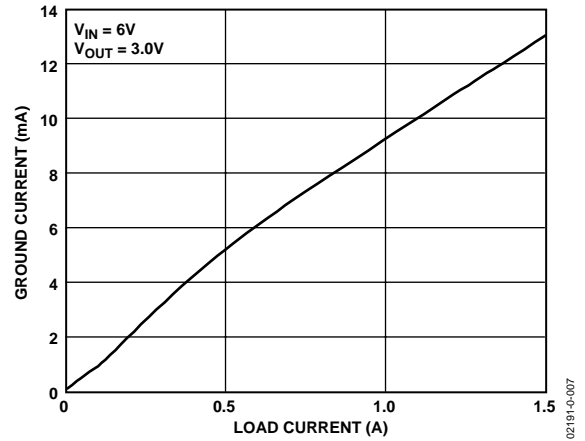


Figure 7. Ground Current vs. Load Current

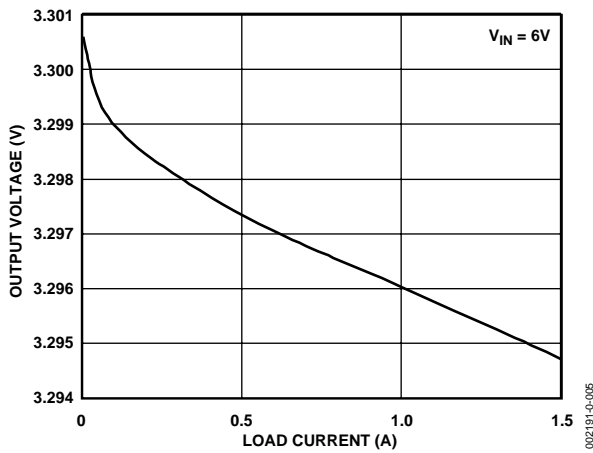


Figure 5. Output Voltage vs. Load Current

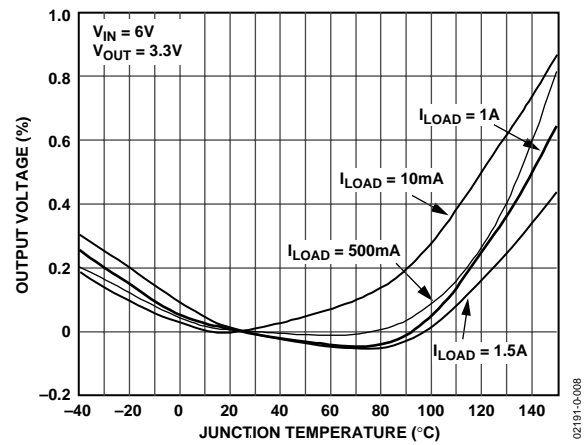


Figure 8. Output Voltage Variation % vs. Junction Temperature

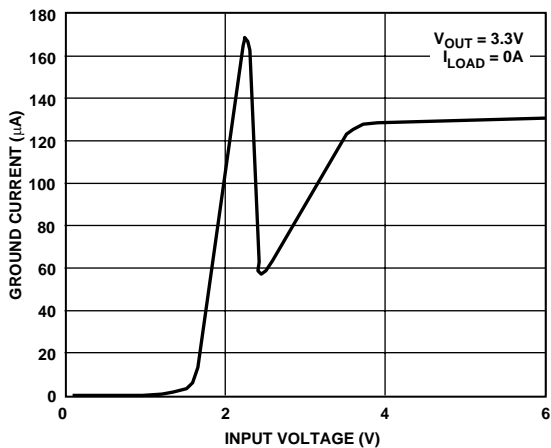


Figure 6. Ground Current vs. Supply Voltage

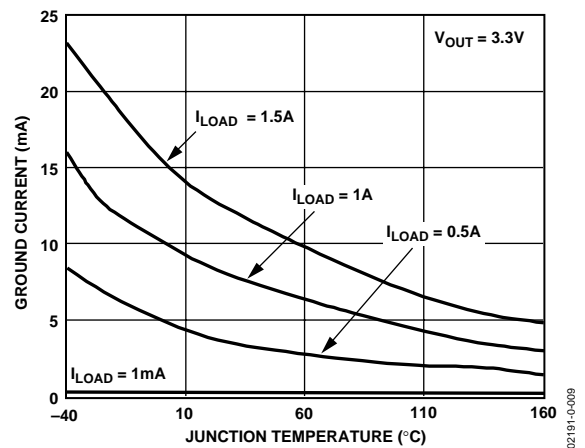


Figure 9. Ground Current vs. Junction Temperature

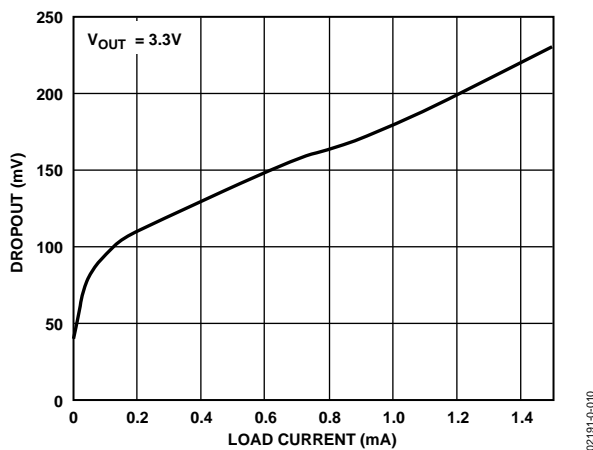


Figure 10. Dropout Voltage vs. Load Current

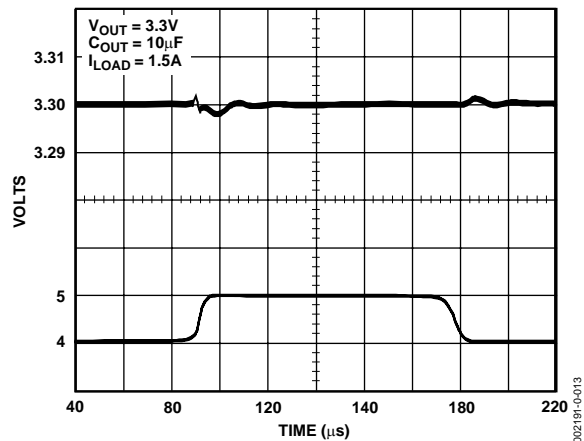


Figure 13. Line Transient Response

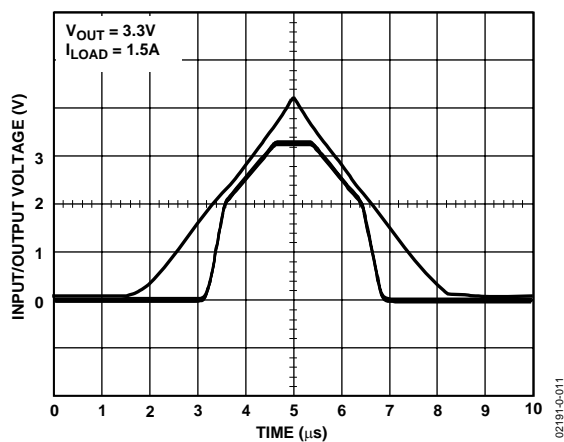


Figure 11. Power-Up/Power-Down

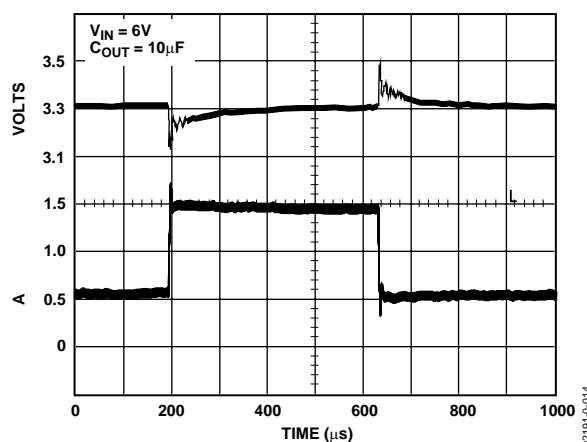


Figure 14. Load Transient Response

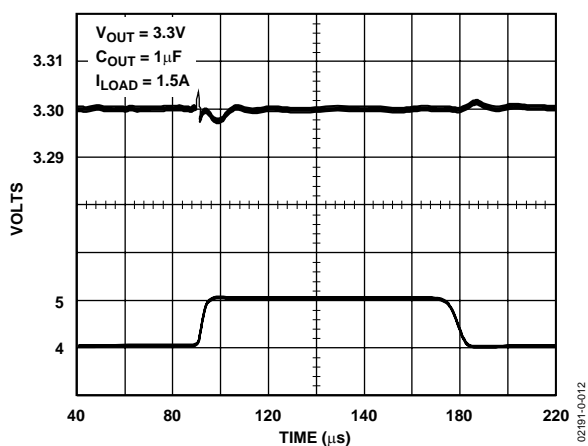


Figure 12. Line Transient Response

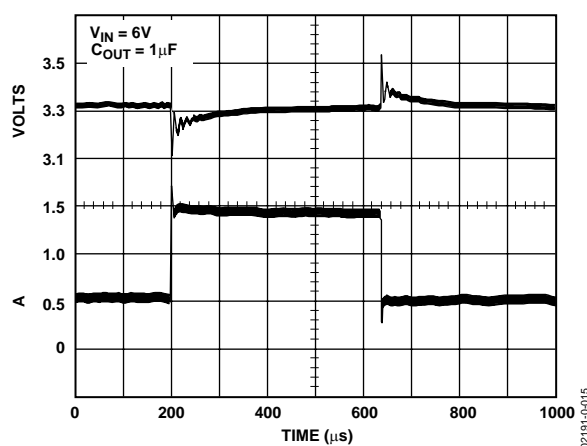


Figure 15. Load Transient Response

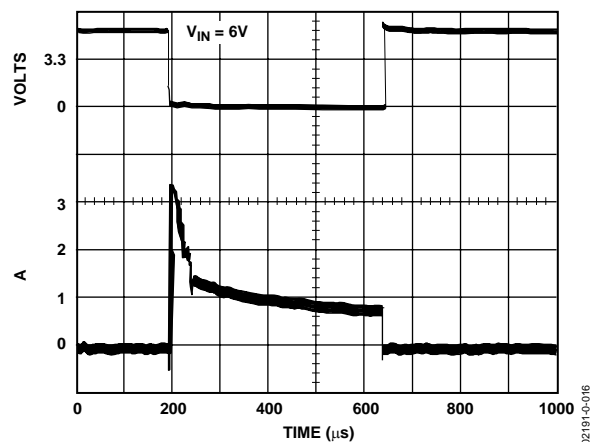


Figure 16. Short-Circuit Current

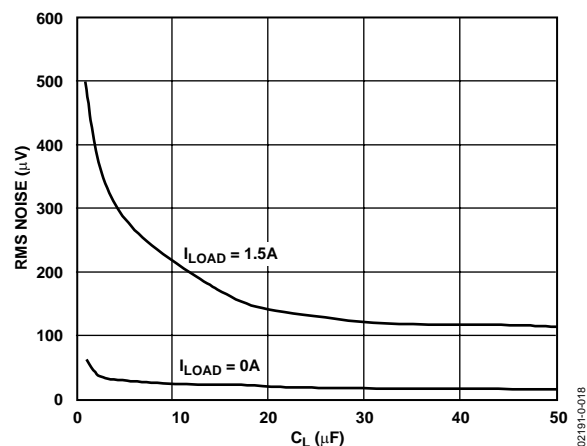


Figure 18. RMS Noise vs.  $C_L$  (10 Hz to 100 kHz)

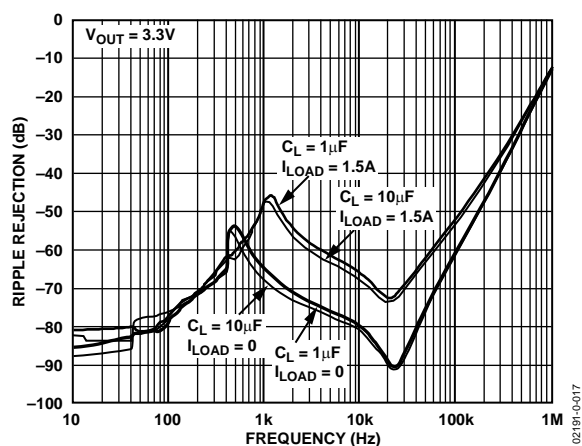


Figure 17. Power Supply Ripple Rejection

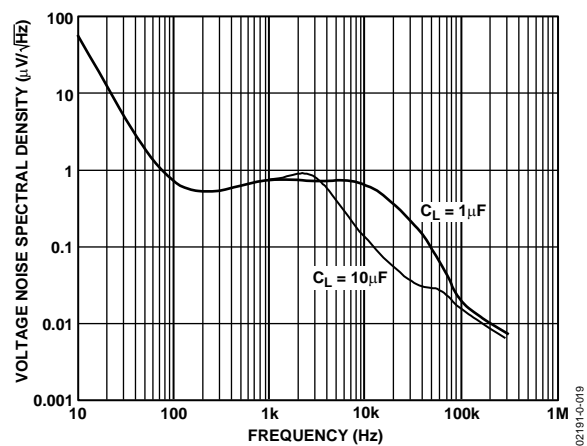


Figure 19. Output Noise Density



## THEORY OF OPERATION

The ADP3339 anyCAP LDO uses a single control loop for regulation and reference functions. The output voltage is sensed by a resistive voltage divider, consisting of R1 and R2, which is varied to provide the available output voltage option. Feedback is taken from this network by way of a series diode (D1) and a second resistor divider (R3 and R4) to the input of an amplifier.

A very high gain error amplifier is used to control this loop. The amplifier is constructed in such a way that equilibrium produces a large, temperature-proportional input offset voltage that is repeatable and very well controlled. The temperature-proportional offset voltage is combined with the complementary diode voltage to form a virtual band gap voltage that is implicit in the network, although it never appears explicitly in the circuit. Ultimately, this patented design makes it possible to control the loop with only one amplifier. This technique also improves the noise characteristics of the amplifier by providing more flexibility on the trade-off of noise sources that leads to a low noise design.

The R1, R2 divider is chosen in the same ratio as the band gap voltage to the output voltage. Although the R1, R2 resistor divider is loaded by diode D1 and a second divider consisting of R3 and R4, the values can be chosen to produce a temperature-stable output. This unique arrangement specifically corrects for the loading of the divider, thus avoiding the error resulting from base current loading in conventional circuits.

The patented amplifier controls a new and unique noninverting driver that drives the pass transistor, Q1. The use of this special noninverting driver enables the frequency compensation to include the load capacitor in a pole-splitting arrangement to achieve reduced sensitivity to the value, type, and ESR of the load capacitance.

Most LDOs place very strict requirements on the range of ESR values for the output capacitor because they are difficult to stabilize due to the uncertainty of load capacitance and resistance. Moreover, the ESR value required to keep conventional LDOs stable changes depending on load and temperature. These ESR limitations make designing with LDOs more difficult because of their unclear specifications and extreme variations over temperature.

With the ADP3339 anyCAP LDO, this is no longer true. It can be used with virtually any good quality capacitor, with no constraint on the minimum ESR. This innovative design allows the circuit to be stable with just a small 1  $\mu\text{F}$  capacitor on the output. Additional advantages of the pole-splitting scheme include superior line noise rejection and very high regulator gain, which lead to excellent line and load regulation. An impressive  $\pm 1.5\%$  accuracy is guaranteed over line, load, and temperature.

Additional features of the circuit include current limit and thermal shutdown.

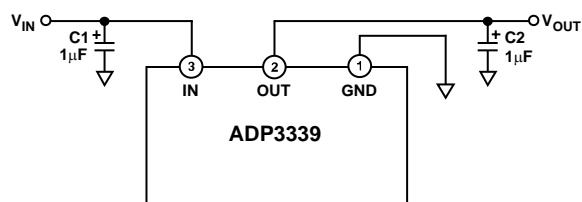


Figure 20. Typical Application Circuit

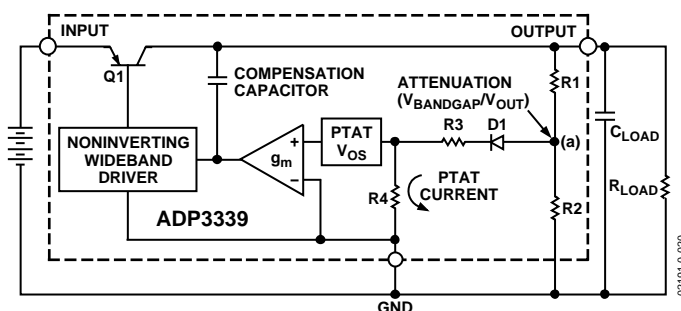


Figure 21. Functional Block Diagram

## APPLICATION INFORMATION

### CAPACITOR SELECTION

#### Output Capacitor

The stability and transient response of the LDO is a function of the output capacitor. The ADP3339 is stable with a wide range of capacitor values, types, and ESR (anyCAP). A capacitor as low as 1  $\mu\text{F}$  is all that is needed for stability. A higher capacitance may be necessary if high output current surges are anticipated, or if the output capacitor cannot be located near the output and ground pins. The ADP3339 is stable with extremely low ESR capacitors ( $\text{ESR} \approx 0$ ) such as multilayer ceramic capacitors (MLCC) or OSCON. Note that the effective capacitance of some capacitor types falls below the minimum over temperature or with dc voltage.

#### Input Capacitor

An input bypass capacitor is not strictly required but is recommended in any application involving long input wires or high source impedance. Connecting a 1  $\mu\text{F}$  capacitor from the input to ground reduces the circuit's sensitivity to PC board layout and input transients. If a larger output capacitor is necessary, a larger value input capacitor is also recommended.

### OUTPUT CURRENT LIMIT

The ADP3339 is short-circuit protected by limiting the pass transistor's base drive current. The maximum output current is limited to about 3 A. See Figure 16.

### THERMAL OVERLOAD PROTECTION

The ADP3339 is protected against damage due to excessive power dissipation by its thermal overload protection circuit. Thermal protection limits the die temperature to a maximum of 160°C. Under extreme conditions (i.e., high ambient temperature and power dissipation) where the die temperature starts to rise above 160°C, the output current is reduced until the die temperature has dropped to a safe level.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For normal operation, the device's power dissipation should be externally limited so the junction temperature does not exceed 150°C.

### CALCULATING POWER DISSIPATION

Device power dissipation is calculated as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + (V_{IN} \times I_{GND})$$

Where  $I_{LOAD}$  and  $I_{GND}$  are load current and ground current, and  $V_{IN}$  and  $V_{OUT}$  are the input and output voltages, respectively.

Assuming worst-case operating conditions are  $I_{LOAD} = 1.5 \text{ A}$ ,  $I_{GND} = 14 \text{ mA}$ ,  $V_{IN} = 3.3 \text{ V}$ , and  $V_{OUT} = 2.5 \text{ V}$ , the device power dissipation is

$$P_D = (3.3 \text{ V} - 2.5 \text{ V}) \times 1500 \text{ mA} + (3.3 \text{ V} \times 14 \text{ mA}) = 1246 \text{ mW}$$

So, for a junction temperature of 125°C and a maximum ambient temperature of 85°C, the required thermal resistance from junction to ambient is

$$\theta_{JA} = \frac{125^\circ\text{C} - 85^\circ\text{C}}{1.246 \text{ W}} = 32.1^\circ\text{C/W}$$

### PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The SOT-223's thermal resistance,  $\theta_{JA}$ , is determined by the sum of the junction-to-case and the case-to-ambient thermal resistances. The junction-to-case thermal resistance,  $\theta_{JC}$ , is determined by the package design and specified at 26.8°C/W. However, the case-to-ambient thermal resistance is determined by the printed circuit board design.

As shown in Figure 22, the amount of copper to which the ADP3339 is mounted affects thermal performance. When mounted to the minimal pads of 2 oz. copper (Figure 22a),  $\theta_{JA}$  is 126.6°C/W. Adding a small copper pad under the ADP3339 (Figure 22b) reduces the  $\theta_{JA}$  to 102.9°C/W. Increasing the copper pad to 1 square inch (Figure 22c) reduces the  $\theta_{JA}$  even further, to 52.8°C/W.

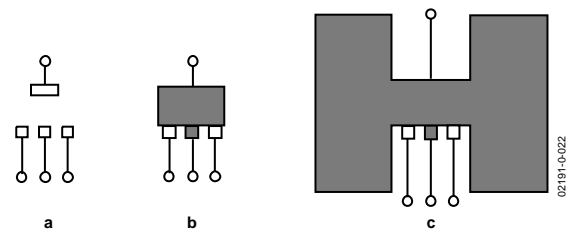


Figure 22. PCB Layouts

Use the following general guidelines when designing printed circuit boards:

1. Keep the output capacitor as close to the output and ground pins as possible.
2. Keep the input capacitor as close to the input and ground pins as possible.
3. PC board traces with larger cross sectional areas remove more heat from the ADP3339. For optimum heat transfer, specify thick copper and use wide traces.
4. The thermal resistance can be decreased by adding a copper pad under the ADP3339, as shown in Figure 22b.
5. If possible, utilize the adjacent area to add more copper around the ADP3339. Connecting the copper area to the output of the ADP3339, as shown in Figure 22c, is best, but thermal performance will be improved even if it is connected to other pins.
6. Use additional copper layers or planes to reduce the thermal resistance. Again, connecting the other layers to the output of the ADP3339 is best, but is not necessary. When connecting the output pad to other layers, use multiple vias.

OUTLINE DIMENSIONS

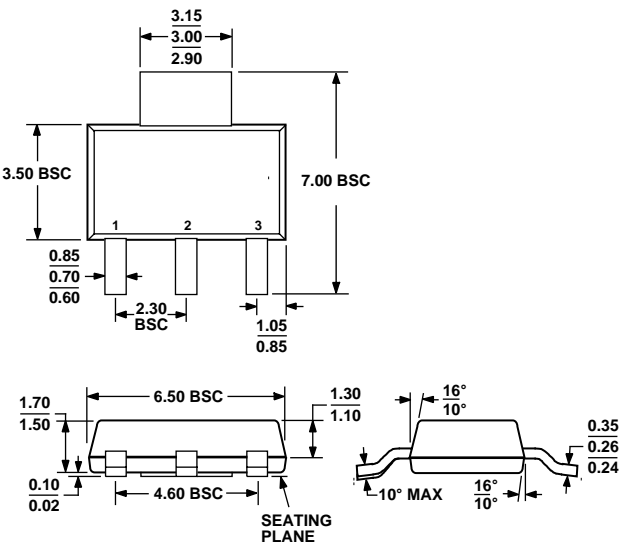


Figure 23. 3-Lead Small Outline Transistor Package [SOT-223]  
(KC-3)  
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage (V)	Package Option	Package Description
ADP3339AKC-1.5-RL	−40°C to +85°C	1.5	KC-3	3-Lead SOT-223
ADP3339AKC-1.5-RL7	−40°C to +85°C	1.5	KC-3	3-Lead SOT-223
ADP3339AKC-1.8-RL	−40°C to +85°C	1.8	KC-3	3-Lead SOT-223
ADP3339AKC-1.8-RL7	−40°C to +85°C	1.8	KC-3	3-Lead SOT-223
ADP3339AKC-2.5-RL	−40°C to +85°C	2.5	KC-3	3-Lead SOT-223
ADP3339AKC-2.5-RL7	−40°C to +85°C	2.5	KC-3	3-Lead SOT-223
ADP3339AKC-2.85-RL	−40°C to +85°C	2.85	KC-3	3-Lead SOT-223
ADP3339AKC-2.85-RL7	−40°C to +85°C	2.85	KC-3	3-Lead SOT-223
ADP3339AKC-3-RL	−40°C to +85°C	3.0	KC-3	3-Lead SOT-223
ADP3339AKC-3-RL7	−40°C to +85°C	3.0	KC-3	3-Lead SOT-223
ADP3339AKC-3.3-RL	−40°C to +85°C	3.3	KC-3	3-Lead SOT-223
ADP3339AKC-3.3-RL7	−40°C to +85°C	3.3	KC-3	3-Lead SOT-223
ADP3339AKC-5-RL	−40°C to +85°C	5	KC-3	3-Lead SOT-223
ADP3339AKC-5-RL7	−40°C to +85°C	5	KC-3	3-Lead SOT-223