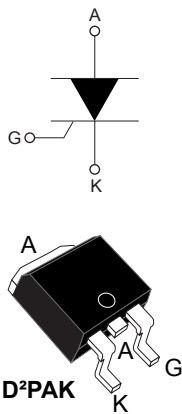


Standard SCR, D²PAK, 25 A, 1200 V



Features

- Max. blocking voltage = $V_{\text{DRM}}, V_{\text{RRM}} = 1200 \text{ V}$
- I_{GT} maximum = 40 mA
- High static and dynamic commutation at $T_j = 125^\circ\text{C}$
 - $di/dt = 50 \text{ A}/\mu\text{s}$
 - $dV/dt = 1500 \text{ V}/\mu\text{s}$
- ECOPACK[®]2 compliant (RoHS and HF compliance)

Applications

- Solar
- Wind renewable energy inverters
- Solid State Relay (SSR)
- Uninterruptible Power Supply (UPS)
- AC DC Inrush Current Limiter (ICL)
- Battery charger
- AC DC voltage controlled rectifier
- Industrial welding systems
- Off board automotive battery charger
- Soft starter
- General purpose motor control

Product status link

[TN2540-12G](#)

Product summary

$I_{\text{T(RMS)}}$	25 A
$V_{\text{DRM}}, V_{\text{RRM}}$	1200 V
I_{GT}	40 mA
T_j	125 °C

Description

Available in SMD D²PAK with anode in backside.

The [TN2540-12G](#) SCR is suitable in industrial applications where high immunity is required with a lower gate current.

1 Characteristics

Table 1. Absolute maximum ratings (limiting values), $T_j = 25\text{ °C}$ unless otherwise specified

Symbol	Parameter		Value	Unit
V _{DRM} /V _{RRM}	Repetitive peak off-state voltage (50-60 Hz)		T _J = 125 °C 1200	V
I _{T(RMS)}	On-state RMS current (180° conduction angle)		T _C = 102 °C 25	A
I _{T(AV)}	Average on-state current (180° conduction angle)			
I _{TSM}	Non repetitive surge peak on-state current		t _p = 8.3 ms 314	A
			t _p = 10 ms 300	
I ² t	I ² t value for fusing		t _p = 10 ms 450	A ² s
di/dt	I _G = 2 x I _{GT} , tr ≤ 100 ns Critical rate of rise of on-state current		f = 60 Hz 50	A/μs
I _{GM}	Peak gate current	t _p = 20 μs T _J = 125 °C	4	A
P _{G(AV)}	Average gate power dissipation		T _J = 125 °C 1	W
T _{stg}	Storage junction temperature range			-40 to +150 °C
T _J	Operating junction temperature range			-40 to +125 °C

Table 2. Electrical characteristics ($T_j = 25\text{ °C}$ unless otherwise specified)

Symbol	Test conditions		Value	Unit
I_{GT}	$V_D = 12\text{ V}$, $R_L = 33\text{ }\Omega$	Min.	4	mA
		Max.	40	
V_{GT}		Max.	1.3	V
V_{GD}	$V_D = V_{\text{DRM}}$, $R_L = 3.3\text{ k}\Omega$	$T_j = 125\text{ °C}$ Min.	0.2	V
I_{H}	$I_T = 500\text{ mA}$, gate open		Max. 80	mA
I_{L}	$I_G = 1.2 \times I_{\text{GT}}$		Max. 90	mA
dV/dt	$V_D = 67\text{ \% } V_{\text{DRM}}$, gate open	$T_j = 125\text{ °C}$ Min.	1500	V/ μ s

Table 3. Static electrical characteristics

Symbol	Test conditions		Value	Unit
V_{TM}	$I_{\text{TM}} = 50\text{ A}$, $t_p = 380\text{ }\mu\text{s}$	$T_j = 25\text{ °C}$ Max.	1.60	V
V_{TO}	Threshold voltage		$T_j = 125\text{ °C}$ Max.	
R_D	Dynamic resistance		$T_j = 125\text{ °C}$ Max.	m Ω
I_{DRM} , I_{RRM}	$V_{\text{OUT}} = 1200\text{ V}$	$T_j = 25\text{ °C}$ Max.	10	μ A
		$T_j = 125\text{ °C}$ Max.	6	mA

Table 4. Thermal resistance parameter

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance Junction to case (DC)	Max.	$^{\circ}\text{C/W}$

1.1 Characteristics (curves)

Figure 1. Maximum average power dissipation versus average on-state current

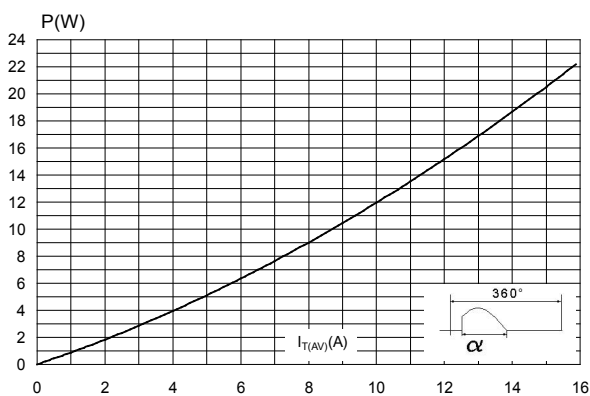


Figure 2. Average and DC on-state current versus case temperature

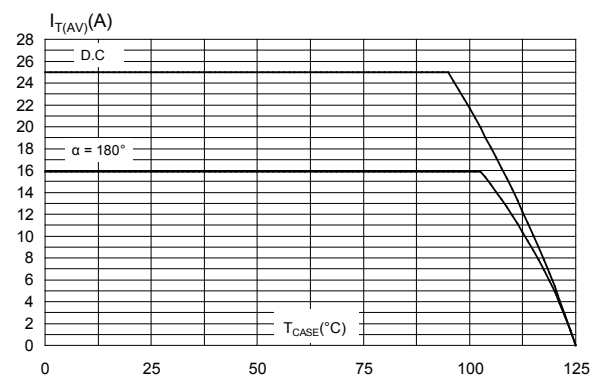


Figure 3. Average and D.C. on state current versus ambient temperature

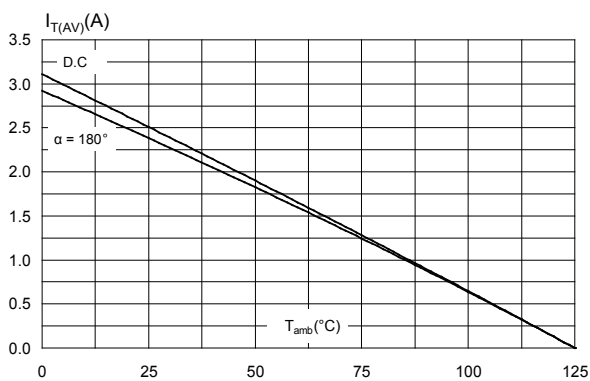


Figure 4. Relative variation of thermal impedance junction to case

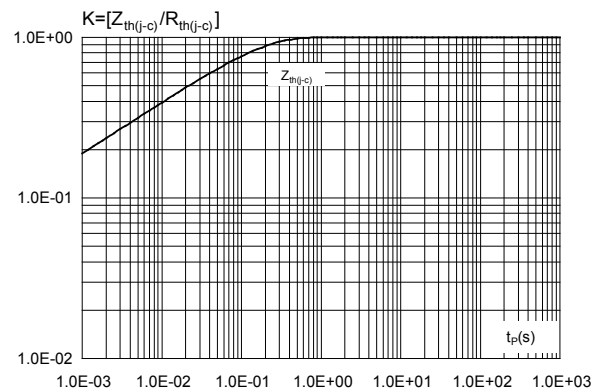


Figure 5. Relative variation of gate trigger and holding current versus junction temperature

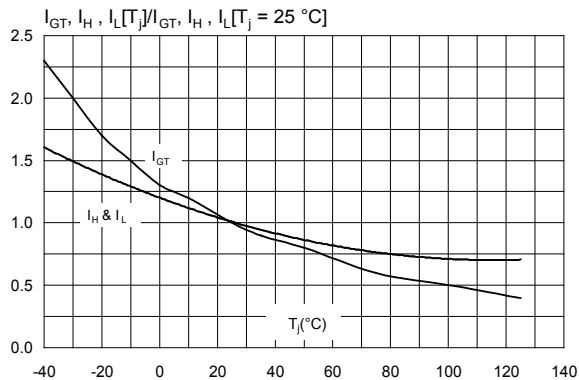


Figure 6. Surge peak on-state current versus number of cycles

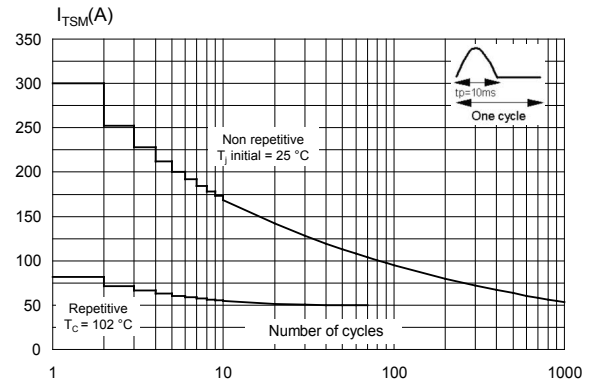


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ ms}$

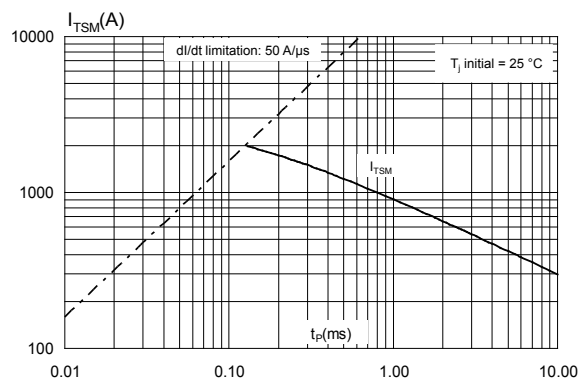
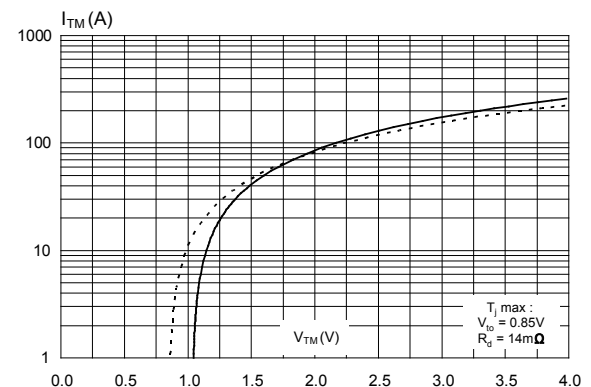


Figure 8. On-state characteristics (maximum values)



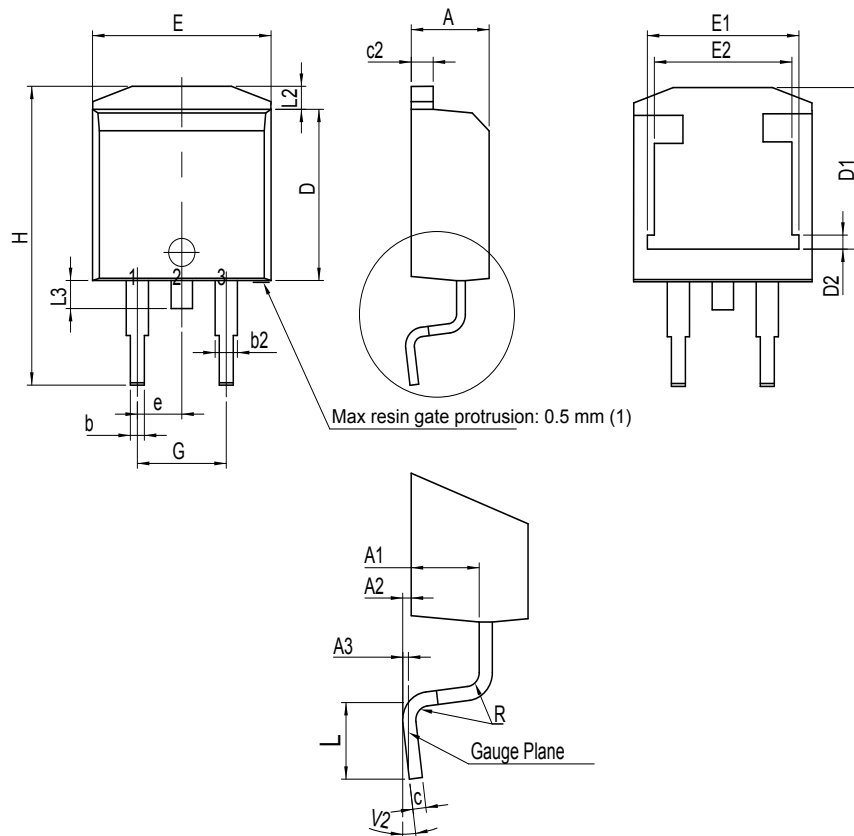
2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 D²PAK package information

- ECOPACK®2 compliant
- Lead-free package leads finishing
- Molding compound resin is halogen-free and meets UL standard level V0

Figure 9. D²PAK package outline



(1) Resin gate is accepted in each of position shown on the drawing, or their symmetrical.

Table 5. D²PAK package mechanical data

Ref.	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.30		4.60	0.1693		0.1811
A1	2.49		2.69	0.0980		0.1059
A2	0.03		0.23	0.0012		0.0091
A3		0.25			0.0098	
b	0.70		0.93	0.0276		0.0366
b2	1.25		1.7	0.0492		0.0669
c	0.45		0.60	0.0177		0.0236
c2	1.21		1.36	0.0476		0.0535
D	8.95		9.35	0.3524		0.3681
D1	7.50		8.00	0.2953		0.3150
D2	1.30		1.70	0.0512		0.0669
e	2.54			0.10000		
E	10.00		10.28	0.3937		0.4047
E1	8.30		8.70	0.3268		0.3425
E2	6.85		7.25	0.2697		0.2854
G	4.88		5.28	0.1921		0.2079
H	15		15.85	0.5906		0.6240
L	1.78		2.28	0.0701		0.0898
L2	1.27		1.40	0.0500		0.0551
L3	1.40		1.75	0.0551		0.0689
R		0.40			0.0157	
V2 ⁽²⁾	0°		8°	0°		8°

1. Dimensions in inches are given for reference only

2. Degrees

Technical drawing of a stepped profile with the following dimensions:

- Overall width: 16.90
- Overall height: 10.30
- Width of the leftmost section: 8.90
- Width of the middle section: 3.70
- Height of the middle section: 5.08
- Height of the rightmost section: 1.30

Technical drawing of a rectangular plate with a grid of holes. The drawing shows a top view and a side view.

Top View Dimensions:

- Overall width: 8,90
- Overall height: 10,30 (10,20)
- Grid of holes: 4 rows by 3 columns.
- Horizontal spacing between hole centers: 2,10
- Vertical spacing between hole centers: 2,60
- Hole diameter: 2,54
- Distance from left edge to first hole center: 0,05
- Distance from right edge to last hole center: 0,05
- Distance from top edge to first hole center: 0,05
- Distance from bottom edge to last hole center: 0,05
- Distance from left edge to first hole center: 0,05
- Distance from right edge to last hole center: 0,05
- Distance from top edge to first hole center: 0,05
- Distance from bottom edge to last hole center: 0,05

Side View Dimensions:

- Overall width: 8,90
- Overall height: 10,30 (10,20)
- Grid of holes: 4 rows by 3 columns.
- Horizontal spacing between hole centers: 2,10
- Vertical spacing between hole centers: 2,60
- Hole diameter: 2,54
- Distance from left edge to first hole center: 0,05
- Distance from right edge to last hole center: 0,05
- Distance from top edge to first hole center: 0,05
- Distance from bottom edge to last hole center: 0,05
- Distance from left edge to first hole center: 0,05
- Distance from right edge to last hole center: 0,05
- Distance from top edge to first hole center: 0,05
- Distance from bottom edge to last hole center: 0,05

3 Ordering information

Figure 12. Ordering information scheme

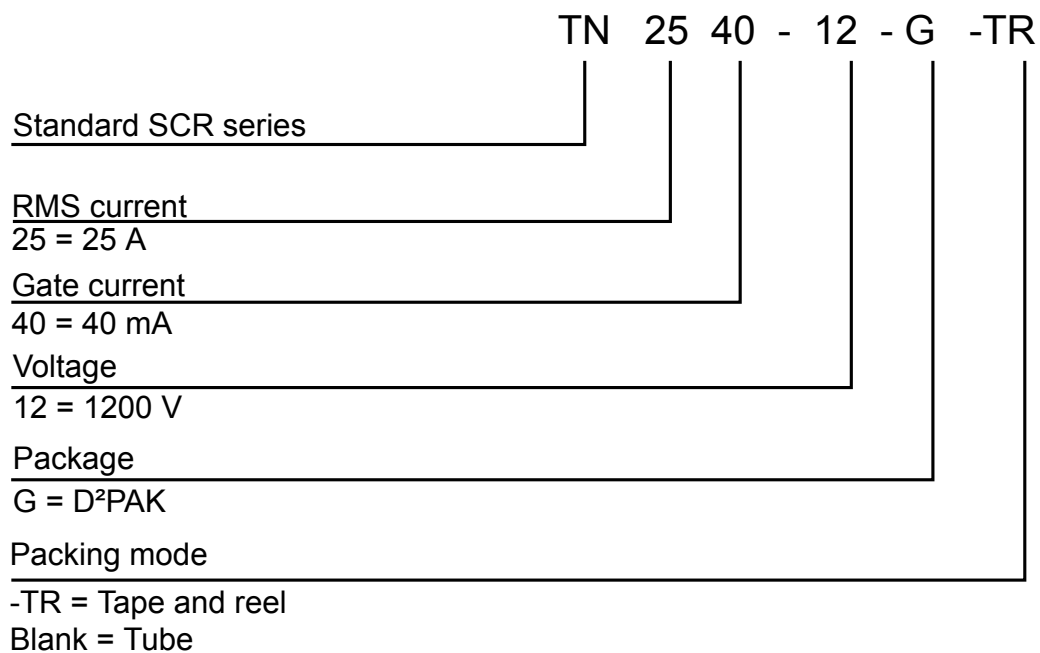


Table 6. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TN2540-12G-TR	TN2540-12G	D ² PAK	1.6 g	1000	Tape and Reel
TN2540-12G				50	Tube

Revision history

Table 7. Document revision history

Date	Version	Changes
18-Oct-2018	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved