IRFP9140

Vishay Siliconix

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PRODUCT SUMMARY

V_{DS} (V)

 $R_{DS(on)}(\Omega)$

Qq (max.) (nC)

Q_{gs} (nC)

Q_{gd} (nC)

Configuration

GO

 $V_{GS} = -10 V$

P-Channel MOSFET

0.20

-100

61

14

29

Single

TO-247AC

Power MOSFET

FEATURES

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- P-channel
- · Isolated central mounting hole
- 175 °C operating temperature
- · Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The **TO-247AC** package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220AB devices. The TO-247AC is similar but superior to the earlier TO-218 package because of its isolated mouting hole. It also provides greater creepage distance between pins to meet the requirements of most safety specifications.

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	IRFP9140PbF

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V _{DS}	-100	V
Gate-source voltage			V _{GS}	± 20	v
Continuous drain current V_{GS} at - 10 V $T_C = 25 \degree C$ $T_C = 100 \degree C$		I _D	-21		
Continuous drain current	V _{GS} at - 10 V	$T_C = 100 ^{\circ}C$	D	-15	А
Pulsed drain current ^a		I _{DM}	-84		
Linear derating factor				1.2	W/°C
Single pulse avalanche energy ^b			E _{AS}	960	mJ
Repetitive avalanche current ^a			I _{AR}	-21	А
Repetitive avalanche energy ^a			E _{AR}	18	mJ
Maximum power dissipation $T_{C} = 25 \text{ °C}$			PD	180	W
Peak diode recovery dV/dt ^c			dV/dt	-5.5	V/ns
Operating junction and storage temperature range		T _J , T _{stg}	-5 to +175	°C	
Soldering recommendations (peak temperature) for 10 s		S		300 ^d	U
Mounting Torque	6 22 or M2	corow		10	lbf · in
Mounting Torque	6-32 or M3 screw			1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11) b. V_{DD} = - 25 V, starting T_J = 25 °C, L = 3.3 mH, R_g = 25 Ω , I_{AS} = - 21 A (see fig. 12) c. I_{SD} ≤ - 21 A, dl/dt ≤ 200 A/µs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C d. 1.6 mm from case

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THERMAL RESISTANCE RAT	INGS						
PARAMETER	SYMBOL	TYP.	M	AX.		UNIT	
Maximum junction-to-ambient	R _{thJA}	-		40			
Case-to-sink, flat, greased surface	R _{thCS}	0.24 -		-		°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	0	.83			
SPECIFICATIONS (T _J = $25 \degree C$,	unless otherv	vise noted)					
PARAMETER	SYMBOL		CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						•	
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 V, I_D = 0$	-250 µA	-100	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25	5 °C, I _D = -1 mA	-	-0.087	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D =$	-250 µA	-2.0	-	-4.0	V
Gate-source leakage	I _{GSS}	$V_{GS} = \pm 20 V$		-	-	± 100	nA
Zara gata voltaga drain averant	L	V _{DS} = -100 V, V	_{GS} = 0 V	-	-	-100	
Zero gate voltage drain current	IDSS	$V_{DS} = -80 \text{ V}, \text{ V}_{G}$	_S = 0 V, T _J = 150 °C	-	-	-500	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = -10 V	I _D = - 13 A ^b	-	-	0.20	Ω
Forward transconductance	g _{fs}	$V_{DS} = -50 \text{ V}, \text{ I}_{D}$	= - 13 A ^b	6.2	-	-	S
Dynamic							
Input capacitance	C _{iss}	$V_{GS} = 0 V,$		-	1400	-	
Output capacitance	C _{oss}	$V_{DS} = -25 V,$		-	590	-	pF
Reverse transfer capacitance	C _{rss}	f = 1.0 MHz, se	e fig. 5	-	140	-	
Total gate charge	Qg			-	-	61	
Gate-source charge	Q _{gs}	$V_{GS} = -10 V$	$I_D = -19 \text{ A}, V_{DS} = -80 \text{ see fig. 6 and } 13^{\text{ b}}$	JV, -	-	14	nC
Gate-drain charge	Q _{gd}		obe ligi e alla re	-	-	29	
Turn-on delay time	t _{d(on)}		·	-	16	-	
Rise time	t _r	V _{DD} = -	50 V, I _D = -19 A,	-	73	-	
Turn-off delay time	t _{d(off)}	R _g = 9.1 Ω, R	$_{\rm D}$ = 2.4 Ω , see fig. 10 ^t) -	34	-	ns
Fall time	t _f			-	57	-	
Internal drain inductance	L _D	Between lead,	۵ لر	-	5.0	-	
Internal source inductance	Ls	6 mm (0.25") from package and center of die contact		-	13	-	nH
Drain-Source Body Diode Characterist	ics	<u> </u>			1	I	1
Continuous source-drain diode current	I _S	MOSFET symb		-	-	- 21	
Pulsed diode forward current ^a	I _{SM}	showing the integral reverse p - n junction d		-	-	- 84	A
Body diode voltage	V _{SD}	T _J = 25 °C, I _S =	- 21 A, V _{GS} = 0 V ^b	-	-	- 5.0	V
Body diode reverse recovery time	t _{rr}				130	260	ns
Body diode reverse recovery charge	Qrr	$I_{\rm J} = 25 {}^{\circ}{\rm C}, I_{\rm F} = 10$	- 19 A, dl/dt = 100 A/µ	-	0.35	0.70	uС

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

Q_{rr}

t_{on}

b. Pulse width \leq 300 µs; duty cycle \leq 2 %.

Body diode reverse recovery charge

Forward turn-on time

2

0.35

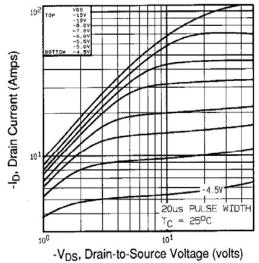
Intrinsic turn-on time is negligible (turn-on is dominated by L_{S} and $L_{D}\!)$

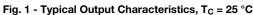
0.70

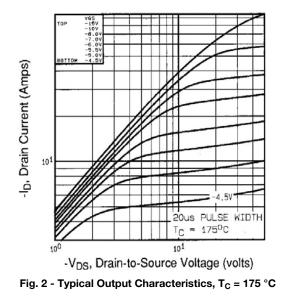
μC

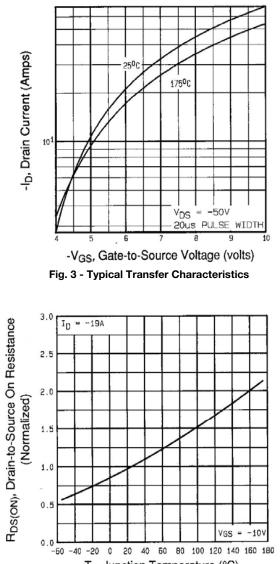


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)









T_J, Junction Temperature (°C)

Fig. 4 - Normalized On-Resistance vs. Temperature

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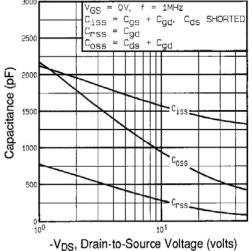


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

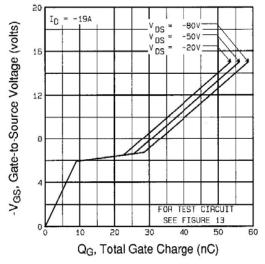


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

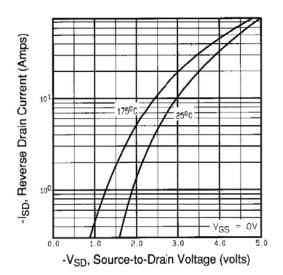
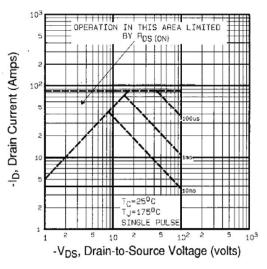


Fig. 7 - Typical Source-Drain Diode Forward Voltage





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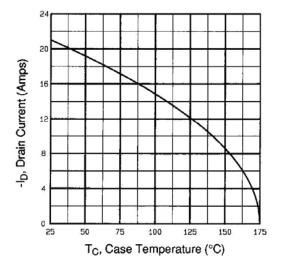


Fig. 9 - Maximum Drain Current vs. Case Temperature

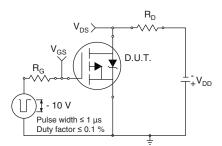


Fig. 10 - Switching Time Test Circuit

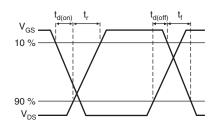


Fig. 11 - Switching Time Waveforms

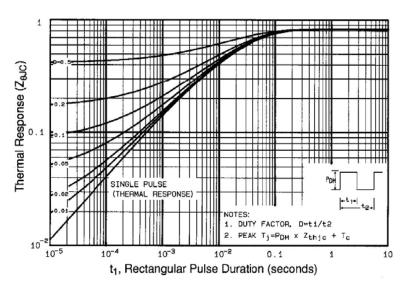


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

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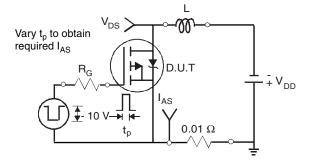


Fig. 13 - Unclamped Inductive Test Circuit

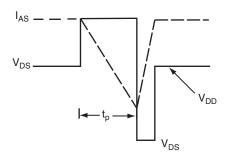


Fig. 14 - Unclamped Inductive Waveforms

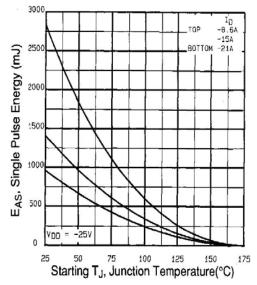
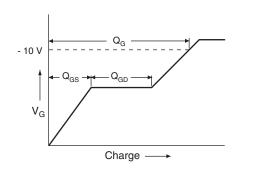


Fig. 15 - Maximum Avalanche Energy vs. Drain Current





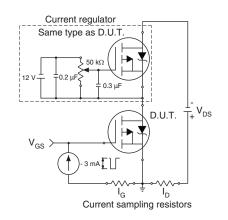


Fig. 17 - Gate Charge Test Circuit

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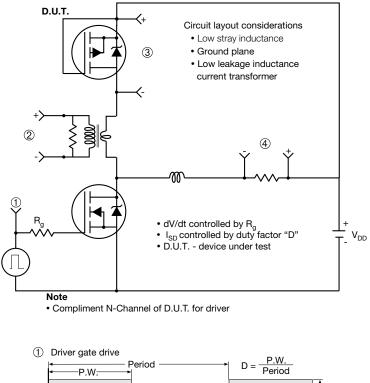
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Peak Diode Recovery dV/dt Test Circuit



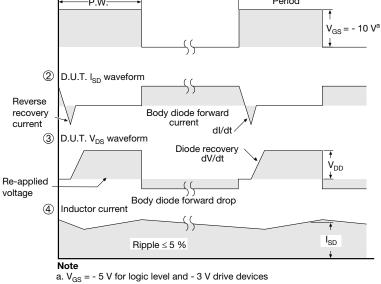


Fig. 18 - For P-Channel

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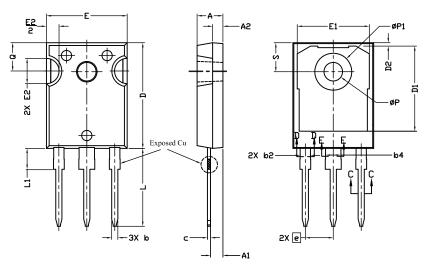
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TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9





Section C--C, D--D, E--E

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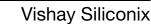
	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
А	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	5.44 BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØP	3.56	3.65	7
Ø P1	7.19	7.19 ref.	
Q	5.31	5.69	
S	5.54	5.74	

Notes

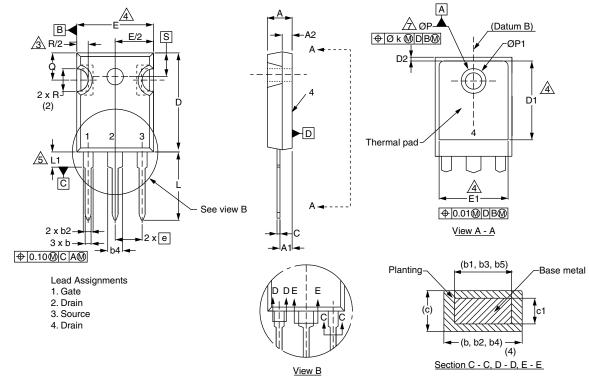
- ⁽¹⁾ Package reference: JEDEC[®] TO247, variation AC
- (2) All dimensions are in mm
- ⁽³⁾ Slot required, notch may be rounded
- ⁽⁴⁾ Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁵⁾ Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

Revision: 19-Oct-2020





VERSION 2: FACILITY CODE = Y



	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
А	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
с	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

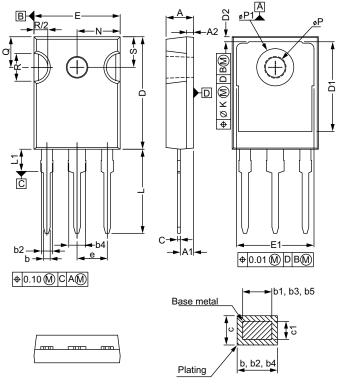
	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.2	254	
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51	BSC	

Notes

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- ⁽²⁾ Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- ⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1
- ⁽⁵⁾ Lead finish uncontrolled in L1
- ⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- ⁽⁷⁾ Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



	MILLIN	IETERS		MILLIN	IETERS
DIM.	MIN.	MAX.	DIM.	MIN.	MAX.
А	4.65	5.31	D2	0.51	1.35
A1	2.21	2.59	E	15.29	15.87
A2	1.17	1.37	E1	13.46	-
b	0.99	1.40	e	5.46	BSC
b1	0.99	1.35	k	0.2	254
b2	1.65	2.39	L	14.20	16.10
b3	1.65	2.34	L1	3.71	4.29
b4	2.59	3.43	N	7.62	BSC
b5	2.59	3.38	Р	3.56	3.66
С	0.38	0.89	P1	-	7.39
c1	0.38	0.84	Q	5.31	5.69
D	19.71	20.70	R	4.52	5.49
D1	13.08	-	S	5.51	BSC

Notes

⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994

⁽²⁾ Contour of slot optional

⁽³⁾ Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body

⁽⁴⁾ Thermal pad contour optional with dimensions D1 and E1

⁽⁵⁾ Lead finish uncontrolled in L1

⁽⁶⁾ Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")

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