DS64EV400 Programmable Quad Equalizer

Check for Samples: DS64EV400

FEATURES

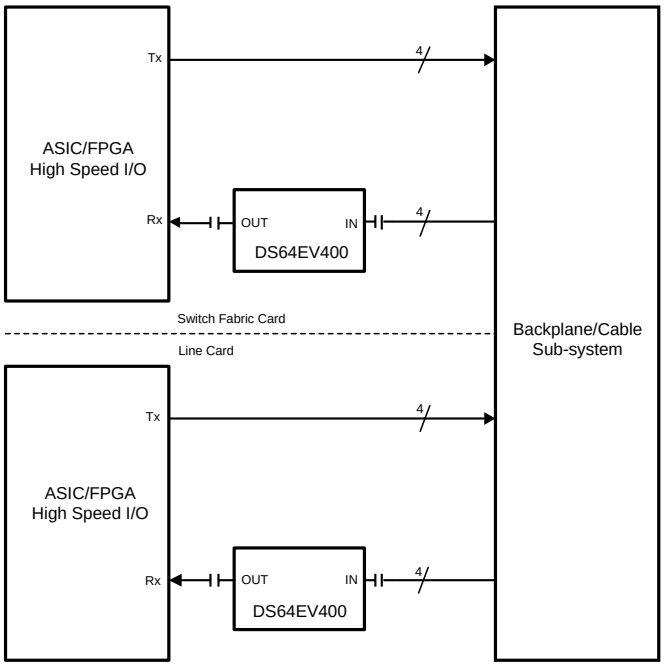
- **Equalizes up to 24 dB Loss at 10 Gbps**
- **Equalizes up to 22 dB Loss at 6.4 Gbps**
- **8 Levels of Programmable Equalization**
- **Settable through Control Pins or SMBus Tnterface**
- **Operates up to 10 Gbps with 30” FR4 Traces**
- **Operates up to 6.4 Gbps with 40” FR4 Traces**
- **0.175 UI Residual Deterministic Jitter at 6.4 Gbps with 40” FR4 Traces**
- **Single 2.5V or 3.3V Power Supply**
- **Signal Detect for Individual Channels**
- **Standby Mode for Individual Channels**
- **Supports AC or DC-Coupling with Wide Input Common-Mode**
- **Low Power Consumption: 375 mW Typ at 2.5V**
- **Small 7 mm x 7 mm 48-Pin WQFN Package**
- **9 kV HBM ESD Rating**
- **-40 to 85°C Operating Temperature Range**

DESCRIPTION

The DS64EV400 programmable quad equalizer provides compensation for transmission medium losses and reduces the medium-induced deterministic jitter for four NRZ data channels. The DS64EV400 is optimized for operation up to 10 Gbps for both cables and FR4 traces. Each equalizer channel has eight levels of input equalization that can be programmed by three control pins, or individually through a Serial Management Bus (SMBus) interface.

The equalizer supports both AC and DC-coupled data paths for long run length data patterns such as PRBS-31, and balanced codes such as 8b/10b. The device uses differential current-mode logic (CML) inputs and outputs. The DS64EV400 is available in a 7 mm x 7 mm 48-pin leadless WQFN package. Power is supplied from either a 2.5V or 3.3V supply.

Simplified Application Diagram



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Pin Descriptions

Pin Name	Pin No.	I/O, Type[1]	Description
HIGH SPEED DIFFERENTIAL I/O			
IN_0+ IN_0–	1 2	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_0+ and IN_0-. Refer to Figure 7.
IN_1+ IN_1–	4 5	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_1+ and IN_1-. Refer to Figure 7.
IN_2+ IN_2–	8 9	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_2+ and IN_2-. Refer to Figure 7.
IN_3+ IN_3–	11 12	I, CML	Inverting and non-inverting CML differential inputs to the equalizer. An on-chip 100Ω terminating resistor is connected between IN_3+ and IN_3-. Refer to Figure 7.
OUT_0+ OUT_0–	36 35	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_0+ to V_{DD} and OUT_0- to V_{DD}.
OUT_1+ OUT_1–	33 32	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_1+ to V_{DD} and OUT_1- to V_{DD}.
OUT_2+ OUT_2–	29 28	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_2+ to V_{DD} and OUT_2- to V_{DD}.
OUT_3+ OUT_3–	26 25	O, CML	Inverting and non-inverting CML differential outputs from the equalizer. An on-chip 50Ω terminating resistor connects OUT_3+ to V_{DD} and OUT_3- to V_{DD}.
EQUALIZATION CONTROL			
BST_2 BST_1 BST_0	37 14 23	I, LVCMOS	BST_2, BST_1, and BST_0 select the equalizer strength for all EQ channels. BST_2 is internally pulled high. BST_1 and BST_0 are internally pulled low.
DEVICE CONTROL			
EN0	44	I, LVCMOS	Enable Equalizer Channel 0 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
EN1	42	I, LVCMOS	Enable Equalizer Channel 1 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
EN2	40	I, LVCMOS	Enable Equalizer Channel 2 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
EN3	38	I, LVCMOS	Enable Equalizer Channel 3 input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High.
FEB	21	I, LVCMOS	Force External Boost. When held high, the equalizer boost setting is controlled by BST_[2:0] pins. When held low, the equalizer boost setting is controlled by SMBus (Table 1) register bits. FEB is internally pulled High.
SD0	45	O, LVCMOS	Equalizer Ch0 Signal Detect Output. Produces a High when signal is detected.
SD1	43	O, LVCMOS	Equalizer Ch1 Signal Detect Output. Produces a High when signal is detected.
SD2	41	O, LVCMOS	Equalizer Ch2 Signal Detect Output. Produces a High when signal is detected.
SD3	39	O, LVCMOS	Equalizer Ch3 Signal Detect Output. Produces a High when signal is detected.
POWER			
V_{DD}	3, 6, 7, 10, 13, 15, 46	Power	V_{DD} = 2.5V ± 5% or 3.3V ± 10%. V_{DD} pins should be tied to V_{DD} plane through low inductance path. A 0.01µF bypass capacitor should be connected between each V_{DD} pin to GND planes.
GND	22, 24, 27, 30, 31, 34	Power	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
DAP	PAD	Power	Ground reference. The exposed pad at the center of the package must be connected to ground plane of the board.
SERIAL MANAGEMENT BUS (SMBus) INTERFACE CONTROL PINS			
SDA SDC CS	18 17 16	I/O, LVCMOS I, LVCMOS I, LVCMOS	Data input/output (bi-directional). Internally pulled high. Clock input. Internally pulled high. Chip select. When pulled high, access to the equalizer SMBus registers are enabled. When pulled low, access to the equalizer SMBus registers are disabled. Please refer to " SMBus configuration Registers" section for detail information.
Other			
Reserv	19, 20 47,48		Reserved. Do not connect.

(1) **Note:** I = Input O = Output

Connection Diagram

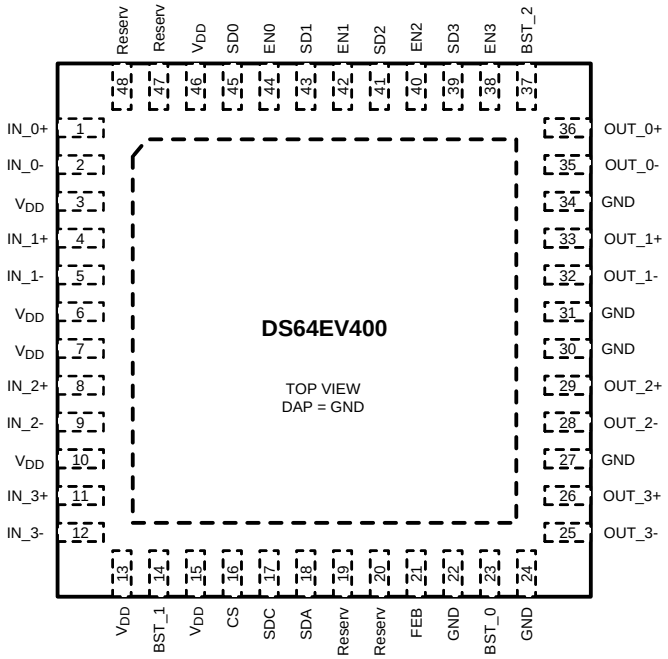

Figure 1. WQFN Package
See Package Number NJU0048D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage (V_{DD})	−0.5V to +4.0V
CMOS Input Voltage	−0.5V + 4.0V
CMOS Output Voltage	−0.5V to 4.0V
CML Input/Output Voltage	−0.5V to 4.0V
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 Seconds)	+260°C
ESD Rating	
HBM, 1.5 kΩ, 100 pF	> 9 kV
EIAJ, 0Ω, 200 pF	> 250V
Thermal Resistance θ_{JA}, No Airflow	30°C/W

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. Absolute Maximum Numbers are ensured for a junction temperature range of -40°C to +125°C. Models are validated to Maximum Operating Voltages only.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Recommended Operating Conditions

		Min	Typ	Max	Units
Supply Voltage	$V_{DD2.5}$ to GND	2.375	2.5	2.625	V
	$V_{DD3.3}$ to GND	3.0	3.3	3.6	V
Ambient Temperature		−40	25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges with default register settings unless other specified.

Parameter		Test Conditions	Min	Typ (1)	Max	Units
POWER						
P	Power Supply Consumption	Device Output Enabled (EN [0–3] = High), $V_{DD3.3}$ (2)		490	700	mW
		Device Output Disable (EN [0–3] = Low), $V_{DD3.3}$			100	mW
P	Power Supply Consumption	Device Output Enabled (EN [0–3] = High), $V_{DD2.5}$ (2)		360	490	mW
		Device Output Disable (EN [0–3] = Low), $V_{DD2.5}$ (2)		30		
N	Supply Noise Tolerance (3)	50 Hz — 100 Hz 100 Hz — 10 MHz 10 MHz — 1.6 GHz		100 40 10		mV_{P-P} mV_{P-P} mV_{P-P}
LVCMOS DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage	$V_{DD3.3}$	2.0		$V_{DD3.3}$	V
		$V_{DD2.5}$	1.6		$V_{DD2.5}$	V
V_{IL}	Low Level Input Voltage		-0.3		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -3mA, $V_{DD3.3}$	2.4			V
		I_{OH} = -3mA, $V_{DD2.5}$	2.0			
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA			0.4	V
I_{IN}	Input Leakage Current	$V_{IN} = V_{DD}$			+15	µA
		V_{IN} = GND	-15			µA
I_{IN-P}	Input Leakage Current with Internal Pull-Down/Up Resistors	$V_{IN} = V_{DD}$, with internal pull-down resistors			+120	µA
		V_{IN} = GND, with internal pull-up resistors	-20			µA
SIGNAL DETECT						
SDH	Signal Detect ON Threshold Level	Default input signal level to assert SD pin, 6.4 Gbps		70		mV_{p-p}
SDI	Signal Detect OFF Threshold Level	Default input signal level to de-assert SD, 6.4 Gbps		40		mV_{p-p}
CML RECEIVER INPUTS (IN_n+, IN_n-)						
V_{TX}	Source Transmit Launch Signal Level (IN diff)	AC-Coupled or DC-Coupled Requirement, Differential measurement at point A. Figure 2	400		1600	mV_{P-P}
V_{INTRE}	Input Threshold Voltage	Differential measurement at point B. Figure 2		120		mV_{P-P}
V_{DDTX}	Supply Voltage of Transmitter to EQ	DC-Coupled Requirement (4)	1.6		V_{DD}	V
V_{ICMDC}	Input Common Mode Voltage	DC-Coupled Requirement, Differential measurement at point A. Figure 2, (5)	V_{DDTX} – 0.8		V_{DDTX} – 0.2	V
R_{LI}	Differential Input Return Loss	100 MHz – 3.2 GHz, with fixture's effect de-embedded		10		dB

(1) Typical values represent most likely parametric norms at V_{DD} = 3.3V or 2.5V, T_A = 25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(2) The $V_{DD2.5}$ is V_{DD} = 2.5V ± 5% and $V_{DD3.3}$ is V_{DD} = 3.3V ± 10%.
(3) Allowed supply noise (mV_{P-P} sine wave) under typical conditions.
(4) Recommended value. Parameter not tested in production.
(5) Measured with clock-like {11111 00000} pattern.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges with default register settings unless other specified.

Parameter		Test Conditions	Min	Typ (1)	Max	Units
R_{IN}	Input Resistance	Differential across IN+ and IN-, Figure 7	85	100	115	Ω
CML OUTPUTS (OUT_n+, OUT_n-)						
V_{OD}	Output Differential Voltage Level (OUT diff)	Differential measurement with OUT+ and OUT- terminated by 50Ω to GND, AC-Coupled Figure 3	500	620	725	mV_{P-P}
V_{OCM}	Output Common Mode Voltage	Single-ended measurement DC-Coupled with 50Ω terminations(5)	V_{DD}– 0.2		V_{DD}– 0.1	V
t_R, t_F	Transition Time	20% to 80% of differential output voltage, measured within 1” from output pins. Figure 3,(5)	20		60	ps
R_O	Output Resistance	Single ended to V_{DD}	42	50	58	Ω
R_{LO}	Differential Output Return Loss	100 MHz – 1.6 GHz, with fixture’s effect de-embedded. IN+ = static high.		10		dB
t_{PLHD}	Differential Low to High Propagation Delay	Propagation delay measurement at 50% VO between input to output, 100 Mbps. Figure 4, (5)		240		ps
t_{PHLD}	Differential High to Low Propagation Delay			240		ps
t_{CCSK}	Inter Pair Channel to Channel Skew	Difference in 50% crossing between channels		7		ps
t_{PPSK}	Part to Part Output Skew	Difference in 50% crossing between outputs		20		ps
EQUALIZATION						
DJ1	Residual Deterministic Jitter at 10 Gbps	30” of 6 mil microstrip FR4, EQ Setting 0x06, PRBS-7 (2^7-1) pattern.(6)		0.20		UI_{P-P}
DJ2	Residual Deterministic Jitter at 6.4 Gbps	40” of 6 mil microstrip FR4, EQ Setting 0x06, PRBS-7 (2^7-1) pattern.(7)(6)		0.17	0.26	UI_{P-P}
DJ3	Residual Deterministic Jitter at 5 Gbps	40” of 6 mil microstrip FR4, EQ Setting 0x07, PRBS-7 (2^7-1) pattern.(7) (6)		0.12	0.20	UI_{P-P}
DJ4	Residual Deterministic Jitter at 2.5 Gbps	40” of 6 mil microstrip FR4, EQ Setting 0x07, PRBS-7 (2^7-1) pattern.(7)(6)		0.1	0.16	UI_{P-P}
RJ	Random Jitter	See (8)(9)		0.5		psrms
SIGNAL DETECT and ENABLE TIMING						
t_{ZISD}	Input OFF to ON detect — SD Output High Response Time	Response time measurement at V_{IN} to SD output, V_{IN} = 800 mV_{P-P}, 100 Mbps, 40” of 6 mil microstrip FR4 Figure 2 and Figure 5,(8)		35		ns
t_{IZSD}	Input ON to OFF detect — SD Output Low Response Time			400		ns
t_{OZOED}	EN High to Output ON Response Time	Response time measurement at EN input to V_O, V_{IN} = 800 mV_{P-P}, 100 Mbps, 40” of 6 mil microstrip FR4 Figure 2 and Figure 7, (8)		150		ns
t_{ZOED}	EN Low to Output OFF Response Time			5		ns

(6) Deterministic jitter is measured at the differential outputs (point C of Figure 2), minus the deterministic jitter before the test channel (point A of Figure 2). Random jitter is removed through the use of averaging or similar means.
(7) Specification is ensured by characterization at optimal boost setting and is not tested in production.
(8) Measured with clock-like {11111 00000} pattern.
(9) Random jitter contributed by the equalizer is defined as sqrt ($J_{OUT}^2 - J_{IN}^2$). J_{OUT} is the random jitter at equalizer outputs in ps-rms, see point C of Figure 2; J_{IN} is the random jitter at the input of the equalizer in ps-rms, see point B of Figure 2.

Electrical Characteristics — Serial Management Bus Interface

Over recommended operating supply and temperature ranges unless other specified.

Parameter		Test Conditions	Min	Typ	Max	Units
SERIAL BUS INTERFACE DC SPECIFICATIONS						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.1		V_{DD}	V
I_{PULLUP}	Current Through Pull-Up Resistor or Current Source	High Power Specification	4			mA
V_{DD}	Nominal Bus Voltage		2.375		3.6	V
$I_{LEAK-Bus}$	Input Leakage Per Bus Segment	See (1)	-200		+200	µA
$I_{LEAK-Pin}$	Input Leakage Per Device Pin			-15		µA
C_I	Capacitance for SDA and SDC	See (1)(2)			10	pF
R_{TERM}	External Termination Resistance pull to V_{DD} = 2.5V ± 5% OR 3.3V ± 10%	$V_{DD3.3}$, (1)(2)(3)		2000		Ω
		$V_{DD2.5}$, (1)(2)(3)		1000		Ω
SERIAL BUS INTERFACE TIMING SPECIFICATIONS (Figure 8)						
FSMB	Bus Operating Frequency	See (4)	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout	See (4)	25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period	See (4)	4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)	See (4)			2	ms
t_F	Clock/Data Fall Time	See (4)			300	ns
t_R	Clock/Data Rise Time	See (4)			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	See (4)			500	ms

(1) Recommended value. Parameter not tested in production.
(2) Recommended maximum capacitance load per bus segment is 400pF.
(3) Maximum termination voltage should be identical to the device supply voltage.
(4) Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SMBus 2.0 physical layer specification. The use of the Chip Select signal is **required**. Holding the CS pin High enables the SMBus port allowing access to the configuration registers. Holding the CS pin Low disables the device's SMBus allowing communication from the host to other slave devices on the bus. In the STANDBY state, the System Management Bus remains active. When communication to other devices on the SMBus is active, the CS signal for the DS32EV400s must be driven Low.

The address byte for all DS64EV400s is AC'h. Based on the SMBus 2.0 specification, the DS64EV400 has a 7-bit slave address of 1010110'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 1100'b or AC'h.

The SDC and SDA pins are 3.3V LVCMOS signaling and include high-Z internal pull up resistors. External low impedance pull up resistors maybe required depending upon SMBus loading and speed. Note, these pins are not 5V tolerant.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SDC is High.

There are three unique states for the SMBus:

START A High-to-Low transition on SDA while SDC is High indicates a message START condition.

STOP A Low-to-High transition on SDA while SDC is High indicates a message STOP condition.

IDLE If SDC and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus Transactions

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drive the 8-bit data byte.
7. The Device drives an ACK bit (“0”).
8. The Host drives a STOP condition.
9. The Host de-selects the device by driving its SMBus CS signal Low.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
3. The Device (Slave) drives the ACK bit (“0”).
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit (“0”).
6. The Host drives a START condition.
7. The Host drives the 7-bit SMBus Address, and a “1” indicating a READ.
8. The Device drives an ACK bit “0”.

9. The Device drives the 8-bit data value (register contents).
10. The Host drives a NACK bit “1”indicating end of the READ transfer.
11. The Host drives a STOP condition.
12. The Host de-selects the device by driving its SMBus CS signal Low.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

See Table 1 for more information.

Table 1. SMBus Register Address

Name	Address	Default	Type (1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	0x00	0x00	RO	ID Revision				SD3	SD2	SD1	SD0
Status	0x01	0x00	RO	EN1	Boost 1			EN0	Boost 0		
Status	0x02	0x00	RO	EN3	Boost 3			EN2	Boost 2		
Enable/Boost (CH 0, 1)	0x03	0x44	RW	EN1 Output 0:Enable 1:Disable	Boost Control for CH1 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)			EN0 Output 0:Enable 1:Disable	Boost Control for CH0 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)		
Enable/Boost (CH 2, 3)	0x04	0x44	RW	EN3 Output 0:Enable 1:Disable	Boost Control for CH3 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)			EN2 Output 0:Enable 1:Disable	Boost Control for CH2 000 (Min Boost) 001 010 011 100 (Default) 101 110 111 (Max Boost)		
Signal Detect	0x05	0x00	RW	SD3 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV		SD2 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV		SD1 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV		SD0 ON Threshold Select 00: 70 mV (Default) 01: 55 mV 10: 90 mV 11: 75 mV	
Signal Detect	0x06	0x00	RW	SD3 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV		SD2 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV		SD1 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV		SD0 OFF Threshold Select 00: 40 mV (Default) 01: 30 mV 10: 55 mV 11: 45 mV	
SMBus Control	0x07	0x00	RW	Reserved							SMBus Enable Control 0: Disable 1: Enable
Output Level	0x08	0x78	RW	Reserved				Output Level: 00: 400 mV_{P-P} 01: 540 mV_{P-P} 10: 620 mV_{P-P}(Default) 11: 760 mV_{P-P}		Reserved	

(1) **Note: RO = Read Only, RW = Read/Write**

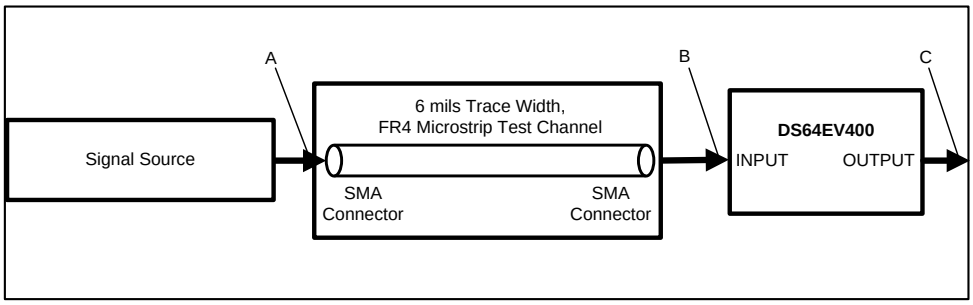

Figure 2. Test Setup Diagram

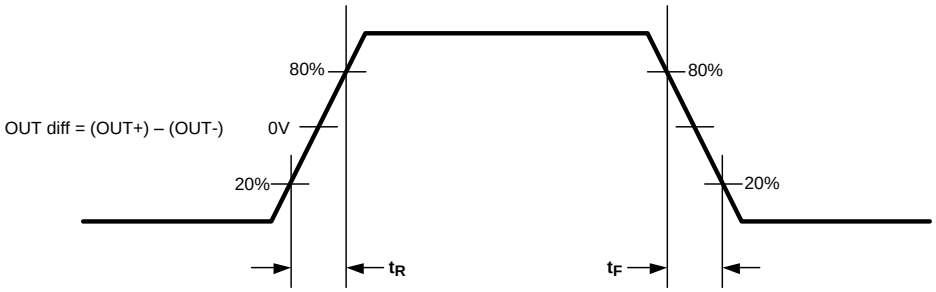

Figure 3. CML Output Transition Times

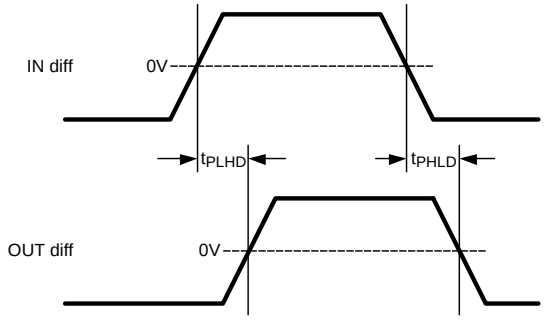

Figure 4. Propagation Delay Timing Diagram

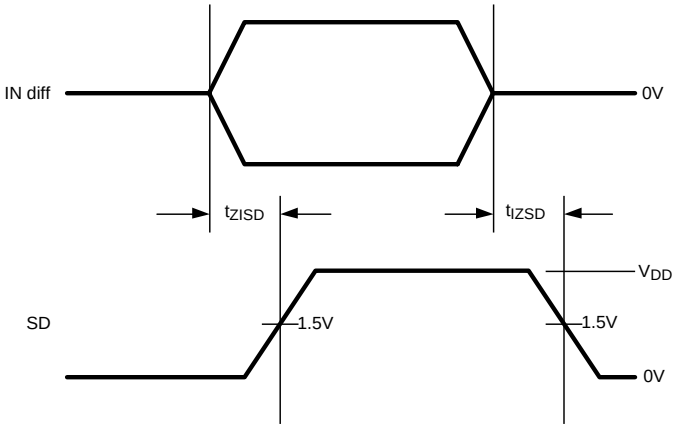

Figure 5. Signal Detect (SD) Delay Timing Diagram

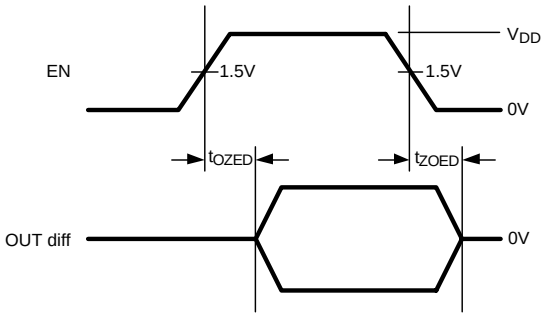

Figure 6. Enable (EN) Delay Timing Diagram

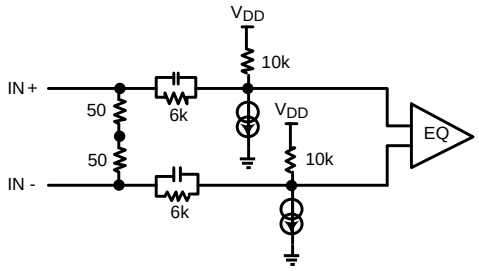

Figure 7. Simplified Receiver Input Termination Circuit

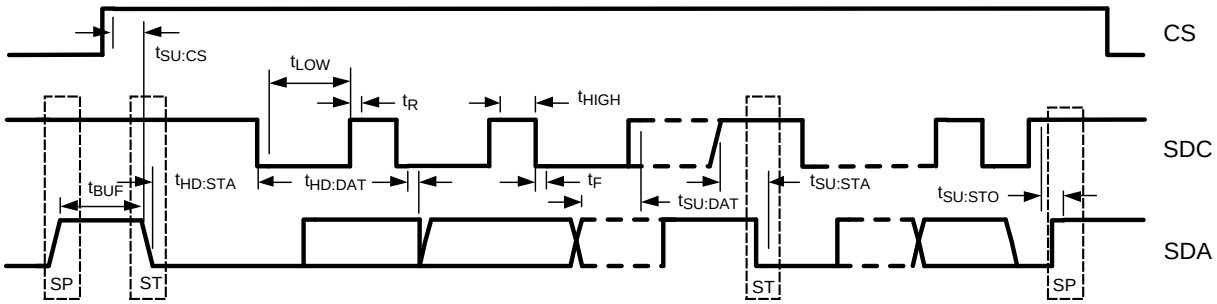

Figure 8. SMBus Timing Parameters

DS64EV400 FUNCTIONAL DESCRIPTIONS

The DS64EV400 is a programmable quad equalizer optimized for operation up to 10 Gbps for backplane and cable applications.

DATA CHANNELS

The DS64EV400 provides four data channels. Each data channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a CML driver as shown in Figure 9.

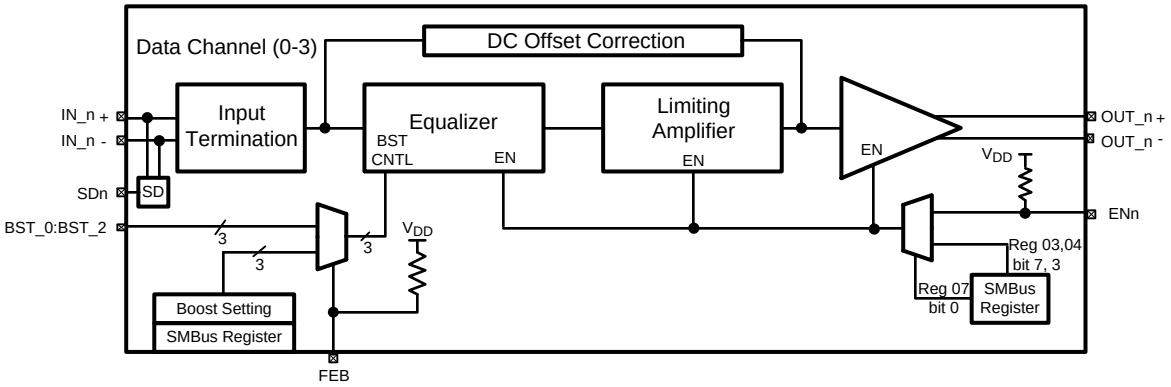

Figure 9. Simplified Block Diagram

EQUALIZER BOOST CONTROL

Each data channel support eight programmable levels of equalization boost. The state of the FEB pin determines how the boost settings are controlled. If the FEB pin is held High, then the equalizer boost setting is controlled by the Boost Set pins (BST_[2:0]) in accordance with Table 2. If this programming method is chosen, then the boost setting selected on the Boost Set pins is applied to all channels. When the FEB pin is held Low, the equalizer boost level is controlled through the SMBus. This programming method is accessed via the appropriate SMBus registers (see Table 1). Using this approach, equalizer boost settings can be programmed for each channel individually. FEB is internally pulled High (default setting); therefore if left unconnected, the boost settings are controlled by the Boost Set pins (BST_[0:2]). The eight levels of boost settings enables the DS64EV400 to address a wide range of media loss and data rates.

Table 2. EQ Boost Control Table

6 mil Microstrip FR4 Trace Length (m)	24 AWG Twin-AX cable length (m)	Channel Loss at 3.2 GHz (dB)	Channel Loss at 5 GHz (dB)	BST_N [2, 1, 0]
0	0	0	0	0 0 0
5	2	5	6	0 0 1
10	3	7.5	10	0 1 0
15	4	10	14	0 1 1
20	5	12.5	18	1 0 0 (Default)
25	6	15	21	1 0 1
30	7	17	24	1 1 0
40	10	22	30	1 1 1

DEVICE STATE AND ENABLE CONTROL

The DS64EV400 has an enable feature on each data channel which provides the ability to control device power consumption. This feature can be controlled either an Enable Pin (EN_n) with Reg 07 = 00'h (default value), or by the Enable Control Bit register which can be configured through the SMBus port (see Table 1 and Table 3 for detail register information), which require setting Reg 07 = 01'h and changing register value of Reg 03, 04. If the Enable is activated using either the external EN_n pin or SMBUS register, the corresponding data channel is placed in the ACTIVE state and all device blocks function as described. The DS64EV400 can also be placed in STANDBY mode to save power. In the STANDBY mode only the control interface including the SMBus port, as well as the signal detection circuit remain active.

Table 3. Controlling Device State

Register 07[0] (SMBus)	ENn Pin (CMOS)	CH 0: Reg. 03 bit 3 CH 1: Reg. 03 bit 7 CH 2: Reg. 04 bit 3 CH 3: Reg. 04 bit 7 (EN Control)	Device State
0 : Disable	1	X	ACTIVE
0 : Disable	0	X	STANDBY
1 : Enable	X	0	ACTIVE
1 : Enable	X	1	STANDBY

SIGNAL DETECT

The DS64EV400 features a signal detect circuit on each data channel. The status of the signal of each channel can be determined by either reading the Signal Detect bit (SDn) in the SMBus registers (see Table 1) or by the state of each SDn pin. An output logic high indicates the presence of a signal that has exceeded the ON threshold value (called SD_ON). An output logic Low means that the input signal has fallen below the OFF threshold value (called SD_OFF). These values are programmed via the SMBus (Table 1). If not programmed via the SMBus, the thresholds take on the default values as shown in Table 4. The Signal Detect threshold values can be changed through the SMBus. All threshold values specified are DC peak-to-peak differential signals (positive signal minus negative signal) at the input of the device.

Table 4. Signal Detect Threshold Values

Channel 0: Bit 1 Channel 1: Bit 3 Channel 2: Bit 5 Channel 3: Bit 7	Channel 0: Bit 0 Channel 1: Bit 2 Channel 2: Bit 4 Channel 3: Bit 6	SD_OFF Threshold Register 06 (mV)	SD_ON Threshold Register 05 (mV)
0	0	40 (Default)	70 (Default)
0	1	30	55
1	0	55	90
1	1	45	75

OUTPUT LEVEL CONTROL

The output amplitude of the CML drivers for each channel can be controlled via the SMBus (see Table 1). The default output level is 620 mV_{p-p}. The following Table presents the output level values supported:

Table 5. Output Level Control Settings

All Channels : Bit 3	All Channels : Bit 2	Output Level Register 08 (mV_{P-P})
0	0	400
0	1	540
1	0	620 (Default)
1	1	760

AUTOMATIC ENABLE FEATURE

It may be desirable to place unused channels in power-saving Standby mode. This can be accomplished by connecting the Signal detect (SDn) pin to the Enable (ENn) pin for each channel (See Figure 10). In order for this option to function properly, the register value for Reg. 07 should be 00'h (default value). If an input signal swing applied to a data channel is above the voltage level threshold as shown in Table 4, then the SDn output pin is asserted High. If the SDn pin is connected to the ENn pin, this will enable the equalizer, limiting amplifier, and output buffer on the data channels; thus the DS64EV400 will automatically enter the ACTIVE state. If the input signal swing falls below the SD_OFF threshold level, then the SDn output will be asserted Low, causing the channel to be placed in the STANDBY state.

DS64EV400 Applications Information

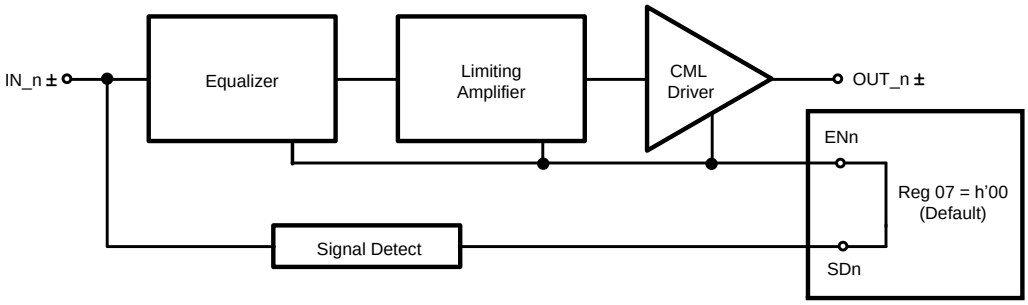

Figure 10. Automatic Enable Configuration

UNUSED EQUALIZER CHANNELS

It is recommended to put all unused channels into standby mode.

GENERAL RECOMMENDATIONS

The DS64EV400 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The CML inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route CML lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the CML signals away from other signals and noise sources on the printed circuit board. See AN-1187(SNOA401) for additional information on WQFN packages.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS64EV400 is provided with an adequate power supply. First, the supply (V_{DD}) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the V_{DD} and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.01µF bypass capacitor should be connected to each V_{DD} pin such that the capacitor is placed as close as possible to the DS64EV400. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS64EV400.

DC COUPLING

The DS64EV400 supports both AC coupling with external ac coupling capacitor, and DC coupling to its upstream driver, or downstream receiver. With DC coupling, users must ensure the input signal common mode is within the range of the electrical specification V_{ICMDC} and the device output is terminated with 50 Ω to V_{DD}. When power-up and power-down the device, both the DS64EV400 and the downstream receiver should be power-up and power-down together. This is to avoid the internal ESD structures at the output of the DS64EV400 at power-down from being turned on by the downstream receiver.

Typical Performance Eye Diagrams and Curves

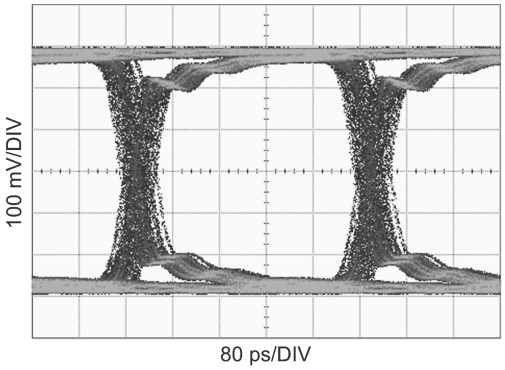

Figure 11. Equalized Signal (40 In FR4, 2.5Gbps, PRBS7, 0x07 Setting)

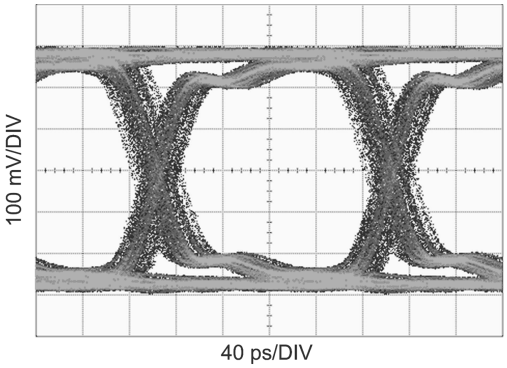

Figure 12. Equalized Signal (40 In FR4, 5Gbps, PRBS7, 0x07 Setting)

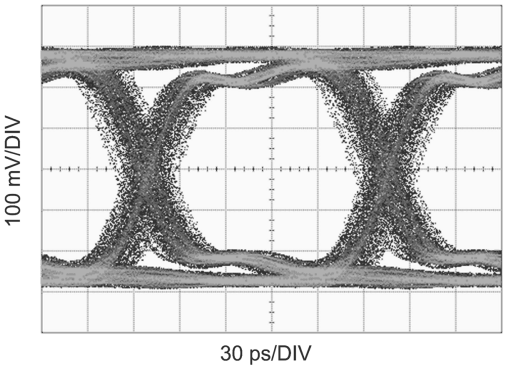

Figure 13. Equalized Signal (40 In FR4, 6.4 Gbps, PRBS7, 0x06 Setting)

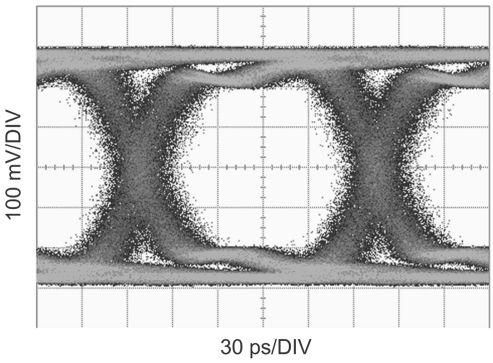

Figure 14. Equalized Signal (40 In FR4, 6.4 Gbps, PRBS31, 0x06 Setting)

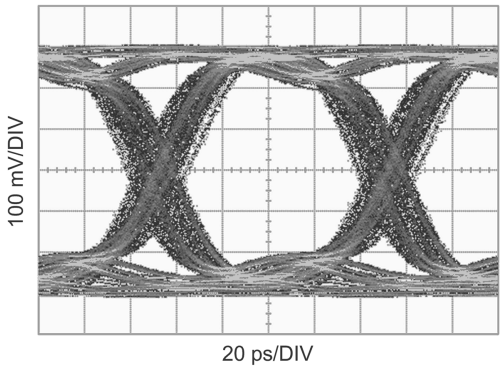

Figure 15. Equalized Signal (30 In FR4, 10 Gbps, PRBS7, 0x06 Setting)

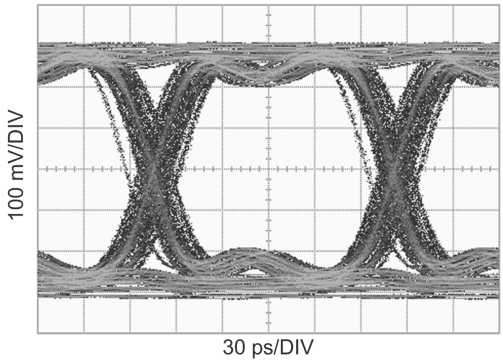

Figure 16. Equalized Signal (10m 24 AWG Twin-Ax Cable, 6.4 Gbps, PRBS7, 0x07 Setting)

Typical Performance Eye Diagrams and Curves (continued)

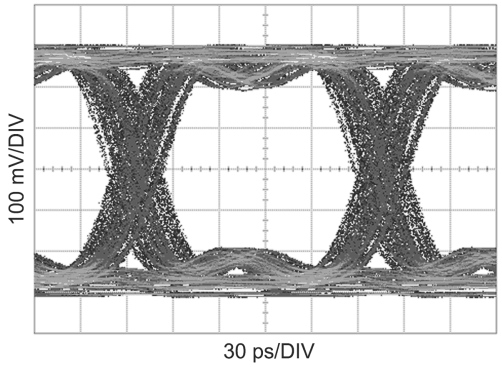

Figure 17. Equalized Signal (32 In Tyco XAUI Backplane, 6.25 Gbps, PRBS7, 0x06 Setting)

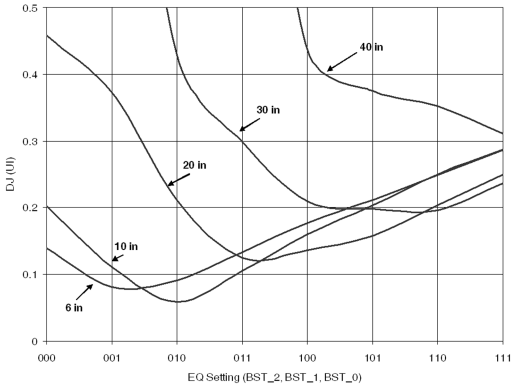

Figure 18. DJ vs. EQ Setting (10 Gbps)

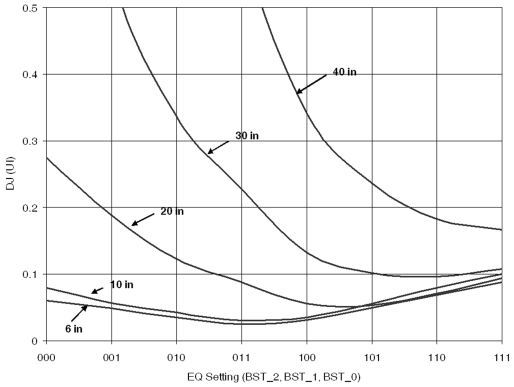

Figure 19. DJ vs EQ Setting (6.4 Gbps)

REVISION HISTORY

Changes from Revision G (April 2013) to Revision H	Page
• Changed layout of National Data Sheet to TI format	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS64EV400SQ/NOPB	ACTIVE	WQFN	NJU	48	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	DS64EV400	Samples
DS64EV400SQX/NOPB	ACTIVE	WQFN	NJU	48		TBD	Call TI	Call TI	-40 to 85	DS64EV400	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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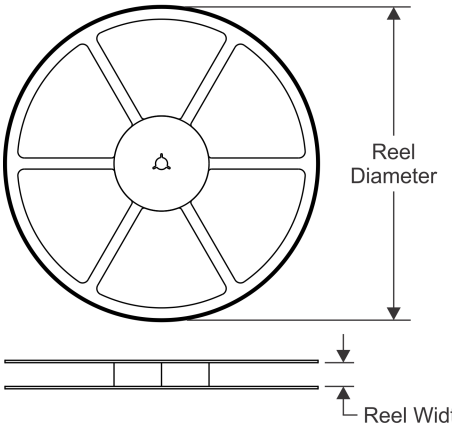
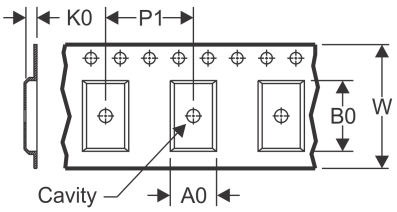
TAPE AND REEL INFORMATION

REEL DIMENSIONS

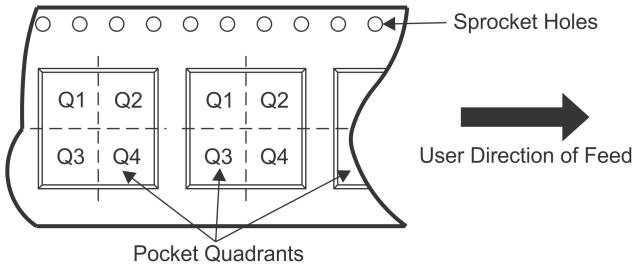


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

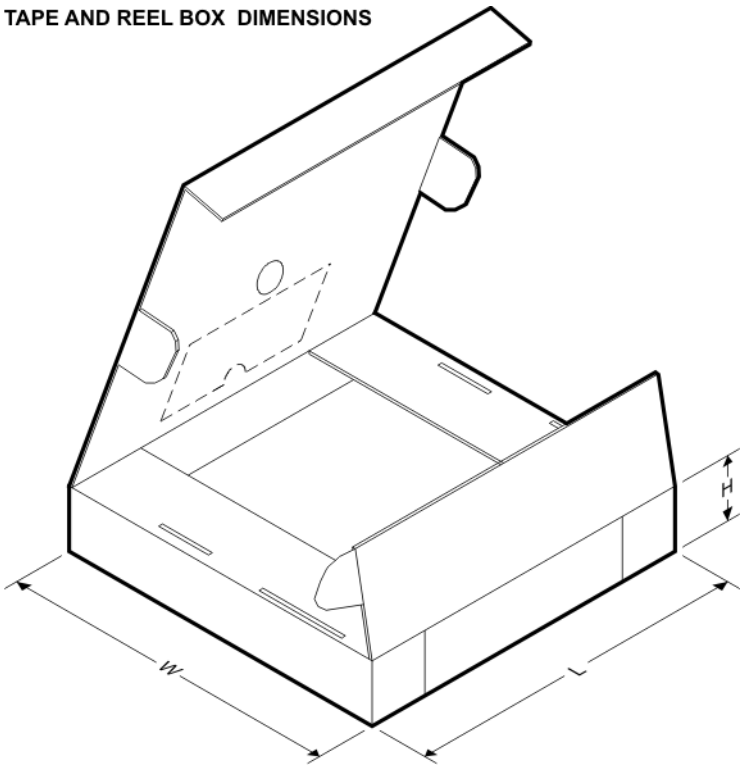
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

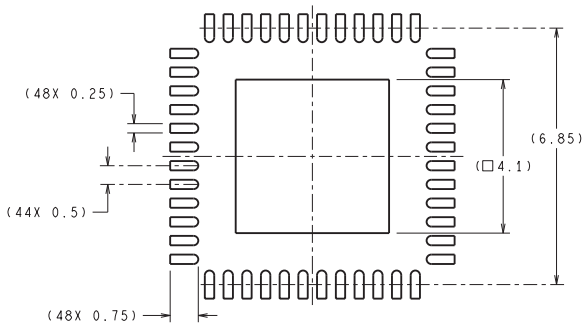
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS64EV400SQ/NOPB	WQFN	NJU	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS64EV400SQ/NOPB	WQFN	NJU	48	250	213.0	191.0	55.0



RECOMMENDED LAND PATTERN

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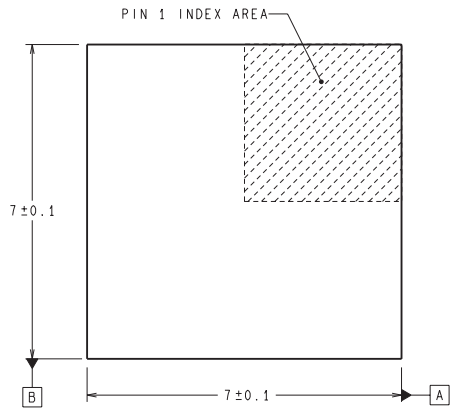
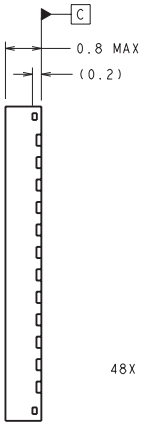
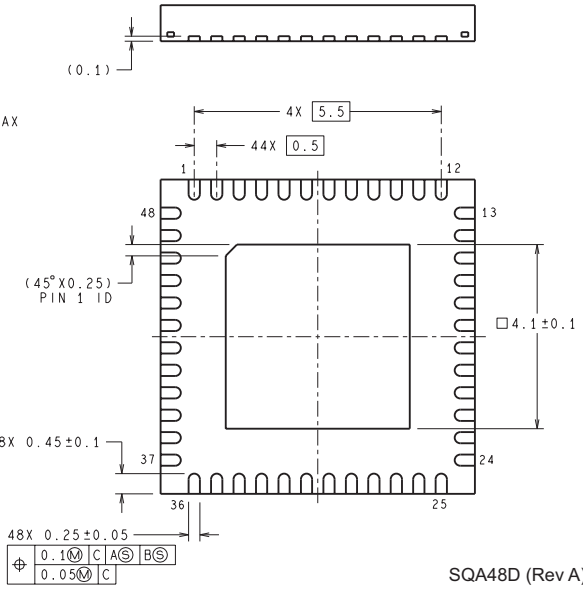
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SQA48D (Rev A)

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