

NCP1249A/B + NCP4355B

Very Low No-load Power Consumption Flyback Converter with Peak Power Excursion Evaluation Board User's Manual



ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Overview

The presented design demonstrates a switching mode AC/DC adapter with an extraordinary stand-by consumption (<10 mW) and high-efficiency operation. The design utilizes a primary flyback controller NCP1249A/B and the secondary side controller NCP4355B. The NCP1249 is a fixed frequency current mode controller featuring a peak power excursion. More over the NCP1249 supports a high-voltage start-up, OFF mode and an integrated X2 cap discharging feature that significantly reduces the input power at very light load or no load conditions.

The NCP1249 architecture is arranged to authorize a transient peak power excursion when the peak current hits the nominal current limit. At the point where the current reaches the current limit the switching frequency is increased from 65 kHz to 130 kHz until the peak power requirement disappears.

The NCP1249 controller also includes frequency fold-back and skip mode feature to provide high efficiency in light load. The secondary side controller, NCP4355B, provides output voltage regulation, very light-load condition detection, OFF mode control and indication LED driver. The NCP4355 communicates with a primary controller featuring OFF mode detection at the REM pin.

Key Features

- Constant voltage regulation
- Very low input power at light and no load
- High-voltage start-up
- Peak power excursion
- Overpower protection
- Universal mains operation

Circuit Description

The primary side uses a flyback topology, providing the advantage of a cost effective power stage design. The design operates in both CCM (continuous conduction mode) and DCM (discontinuous conduction mode), allowing it to accept a wide universal input voltage range. The CCM operation provides desired full load performance with a good efficiency and low ripple of the primary current. The DCM operation permits an increased efficiency under light load conditions by decreasing the switching losses.

The device switches at 65 kHz which represents a good trade-off between switching losses and flyback transformer size. The adapter consists of several important sections. The first is an input EMI filter to reduce the conducted EMI to the ac line at the input of the adapter. The EMI filter is formed by common-mode inductor L4 and capacitors C22, C12, C13 and C11 with differential mode inductor L2. The varistor R33 is used protect the adapter against the line overvoltage peaks. When the power supply is disconnected from the AC mains, X capacitors C22, C11 and Y capacitors C12 and C13 are discharged through HV pin via the following path: rectifying diodes D1, D4, surge protection resistive network R1, R2. This feature replaces commonly used discharging resistors and saves approximately 25 mW of input power consumption at 230 V(AC) line.

A following block is the rectifier with a bulk capacitor. The main power stage of the flyback converter utilizes the low $R_{DS(on)}$ MOSFET SPP11N60C3 along with a custom designed transformer TR1 KA5038-BL, from the Coilcraft company. The detailed design procedure of flyback adapter can be found in the application notes AND8461/D and AN9115/D at ON Semiconductor website: <http://www.onsemi.com>.

The secondary side rectification is done by a low forward voltage drop Schottky diode NTST30100SG from ON Semiconductor. A simple RC snubber (R12 and C5) across the secondary rectifier damps any high frequency ringing caused the unclamped leakage inductance of the transformer secondary side. The secondary-side controller NCP4355B provides the output voltage regulation. Output voltage is set by voltage divider R26, R32, R37 and R41. Regulation output is coupled via the optocoupler (OK1) to the primary side controller NCP1249. The secondary controller also detects a very light load via D19, R42, C27, R43 and R44 via OFFDET pin. When light load condition is detected, primary controller is switched into the OFF mode operation via optocoupler OK2 through the ONOFF pin. The NCP4355 controls the primary controller with an "Active ON" signal, meaning that it only drives optocoupler current during the ON mode to minimize consumption during the OFF mode operation. The built-in LED driver of the NCP4355 indicates primary side operation (when SMPS is not in OFF mode). The LED driver switches with a 1 kHz frequency and 12% duty cycle in order to optimize LED efficiency.

NCP1249A/B + NCP4355B

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	85 – 265	V_{AC}
Input Frequency	f_{IN}	30 – 80	Hz
Output Voltage	V_{OUT}	19.0	V
Nominal Output Current	I_{OUTNOM}	3.4	A
Efficiency $I_{OUT} > 3\% I_{OUTMAX}$	η	>84	%
Efficiency $I_{OUT} > 25\% I_{OUTMAX}$	η	>89	%
No-Load Power Consumption $V_{IN} = 115\text{ V} / 60\text{ Hz}$	P_{IN}	6.1	mW
No-Load Power Consumption $V_{IN} = 230\text{ V} / 50\text{ Hz}$	P_{IN}	9.1	mW
Output Voltage Ripple $I_{OUT} = 3.5\text{ A}$	V_{OUT_PK-PK}	45	mV
Load Regulation $I_{OUT} = 50\text{ mA}$ to 3.5 A	$LOAD_{REG}$	18.7	mV/A
Maximal Load Resistance to Stay in On-Mode	R_{OUTON}	4.4	k Ω
Minimal Load Resistance to Activate Off-Mode	R_{OUTOFF}	5.5	k Ω
Board Dimension		156x59x27	mm

NCP1249A/B + NCP4355B

Schematic

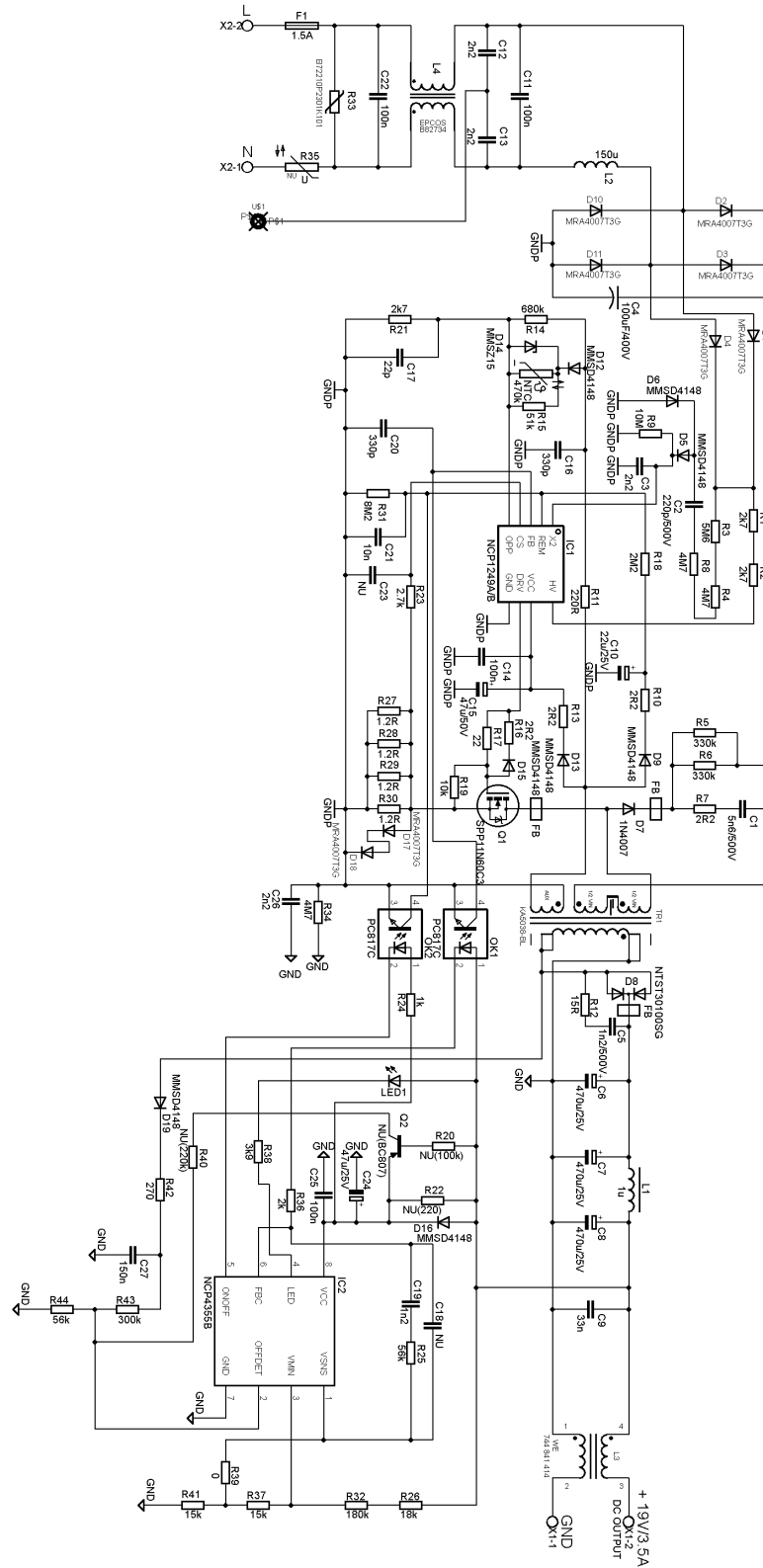


Figure 1. Demo Board Schematic

NCP1249A/B + NCP4355B

No Load Power Consumption

Power consumption was measured by a Yokogawa WT210. The input power was integrated for 60 minutes and averaged from 3 measurements.

Input voltage [V; Hz]	Input power [mW]
85 V; 60 Hz	2.9
115 V; 60 Hz	6.1
230 V; 50 Hz	9.1
265 V; 50 Hz	11.5

Load Regulation

The output voltage regulation is affected by a voltage drop on an output common mode inductor. Therefore output voltage is measured in front of that inductor.

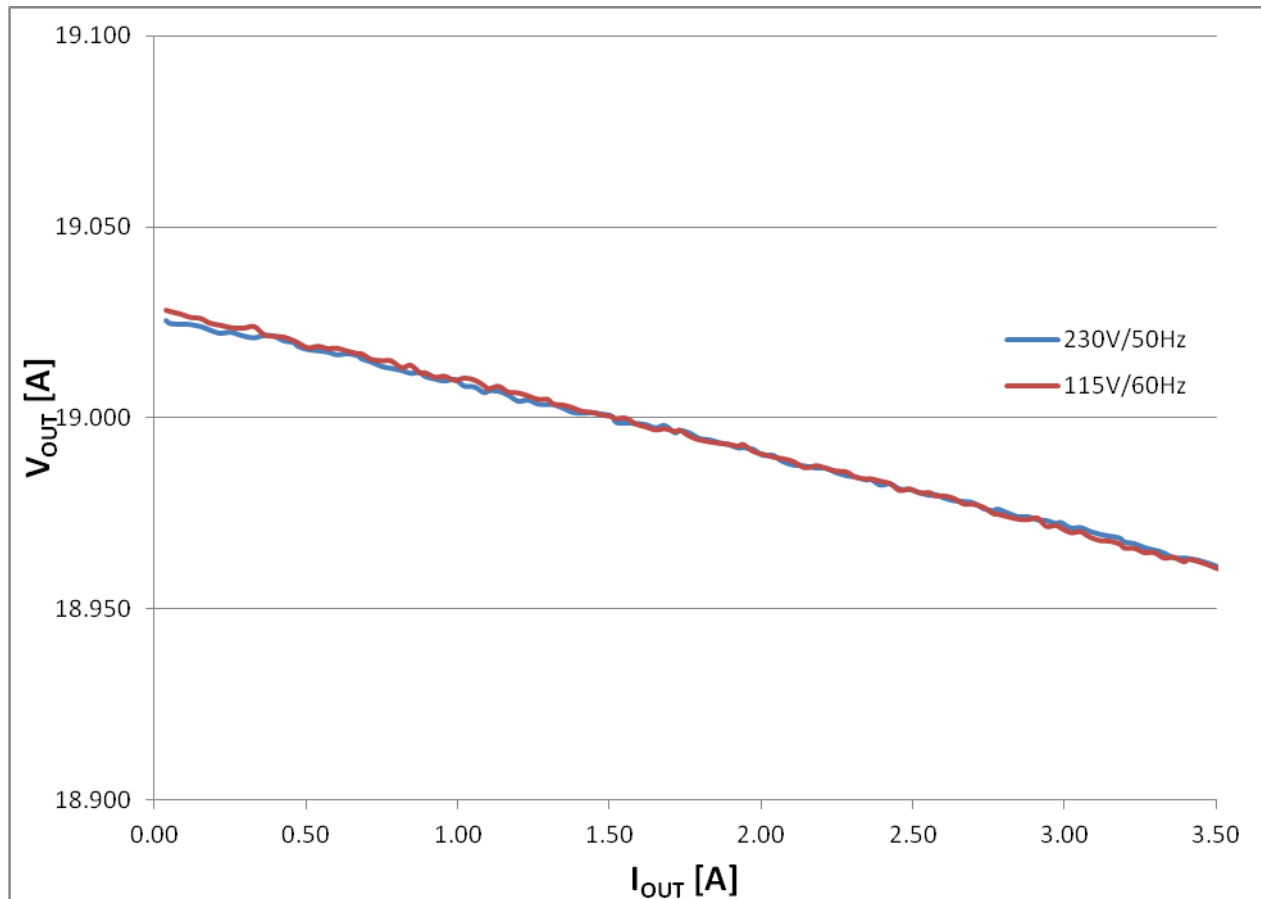


Figure 2. Load Regulation is 18.7 mV/A

NCP1249A/B + NCP4355B

Efficiency vs. Load

NCP1249A/B + NCP4355 Adapter Efficiency

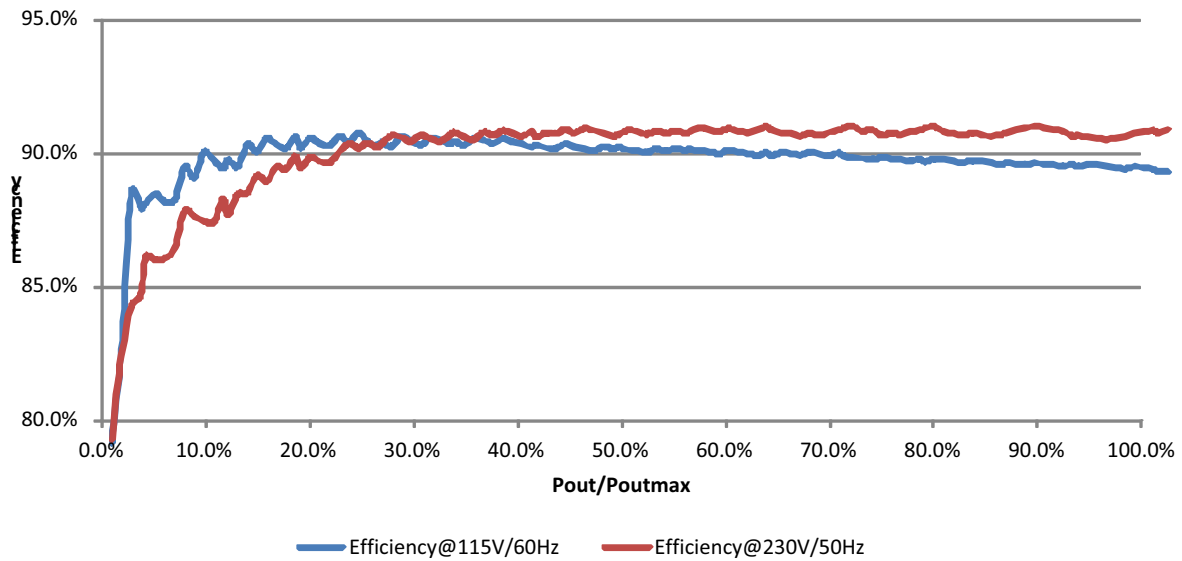


Figure 3. Converter Efficiency for Low and High Line

NCP1249A/B + NCP4355B

Output Voltage Ripple

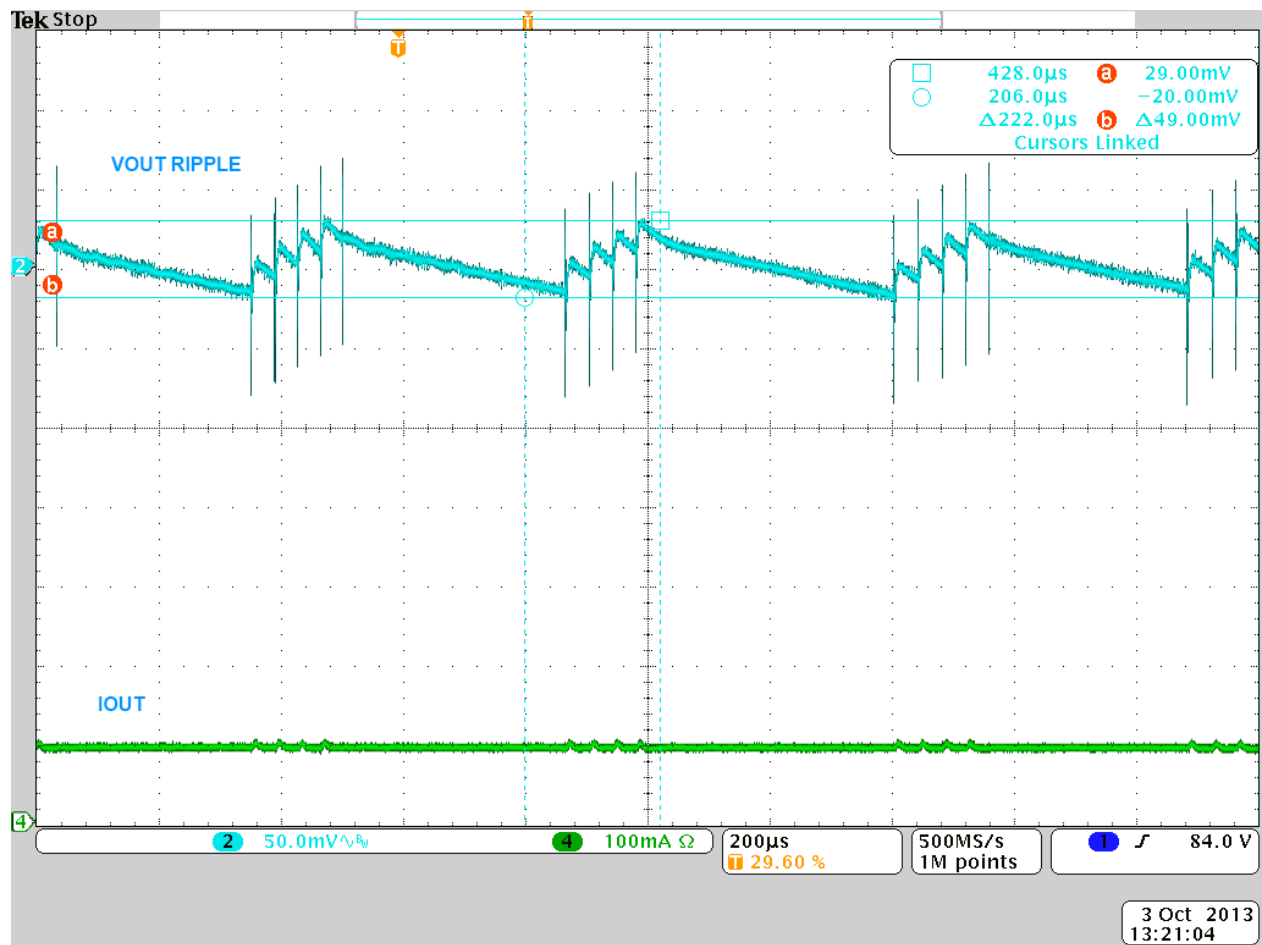


Figure 4. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 100 \text{ mA}$, primary controller is in skip mode, $\Delta V_{OUTPK-PK} = 55 \text{ mV}$

NCP1249A/B + NCP4355B

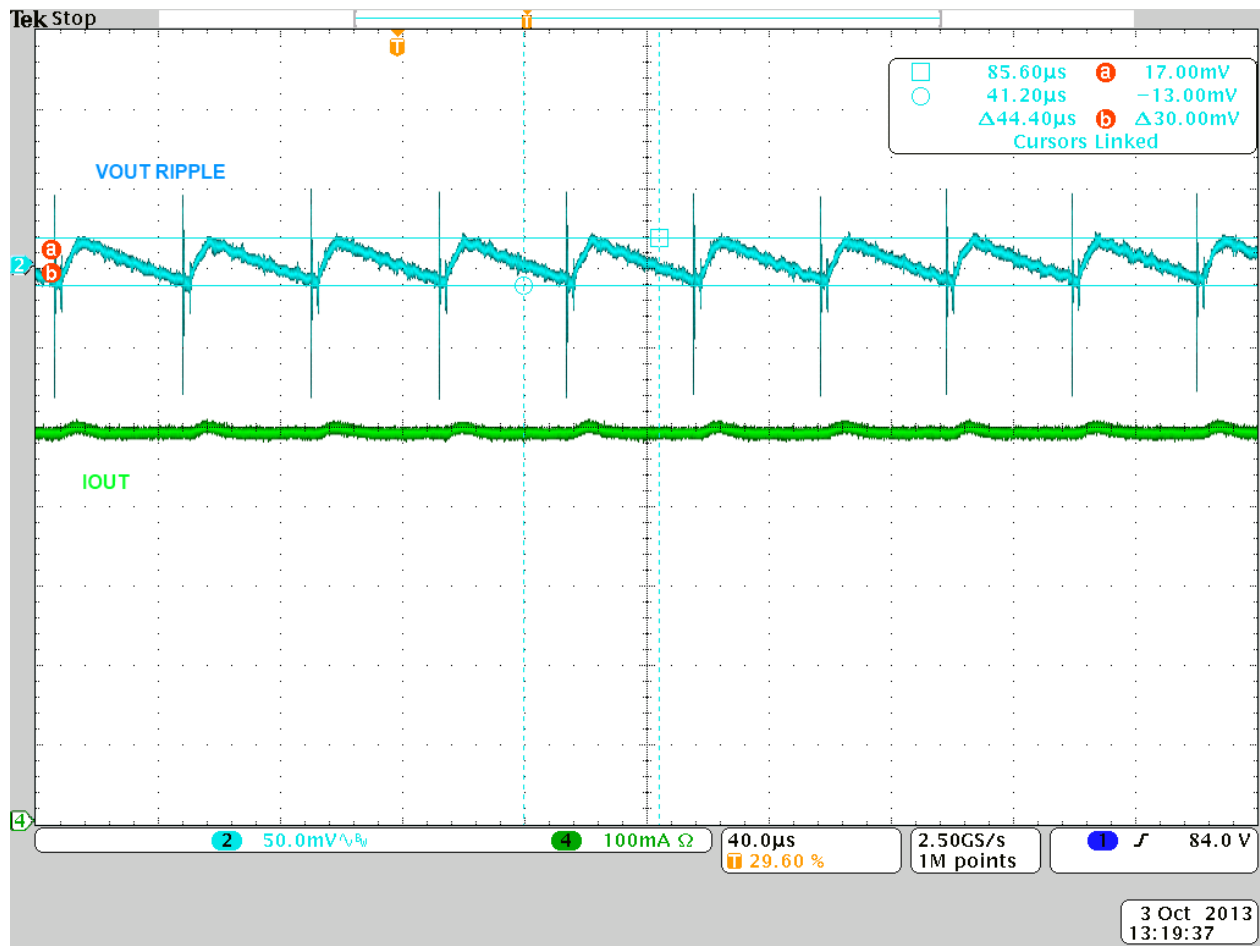


Figure 5. $V_{IN} = 230\text{ V}_{AC}$, $I_{OUT} = 500\text{ mA}$, $\Delta V_{OUTPK-PK} = 45\text{ mV}$

NCP1249A/B + NCP4355B

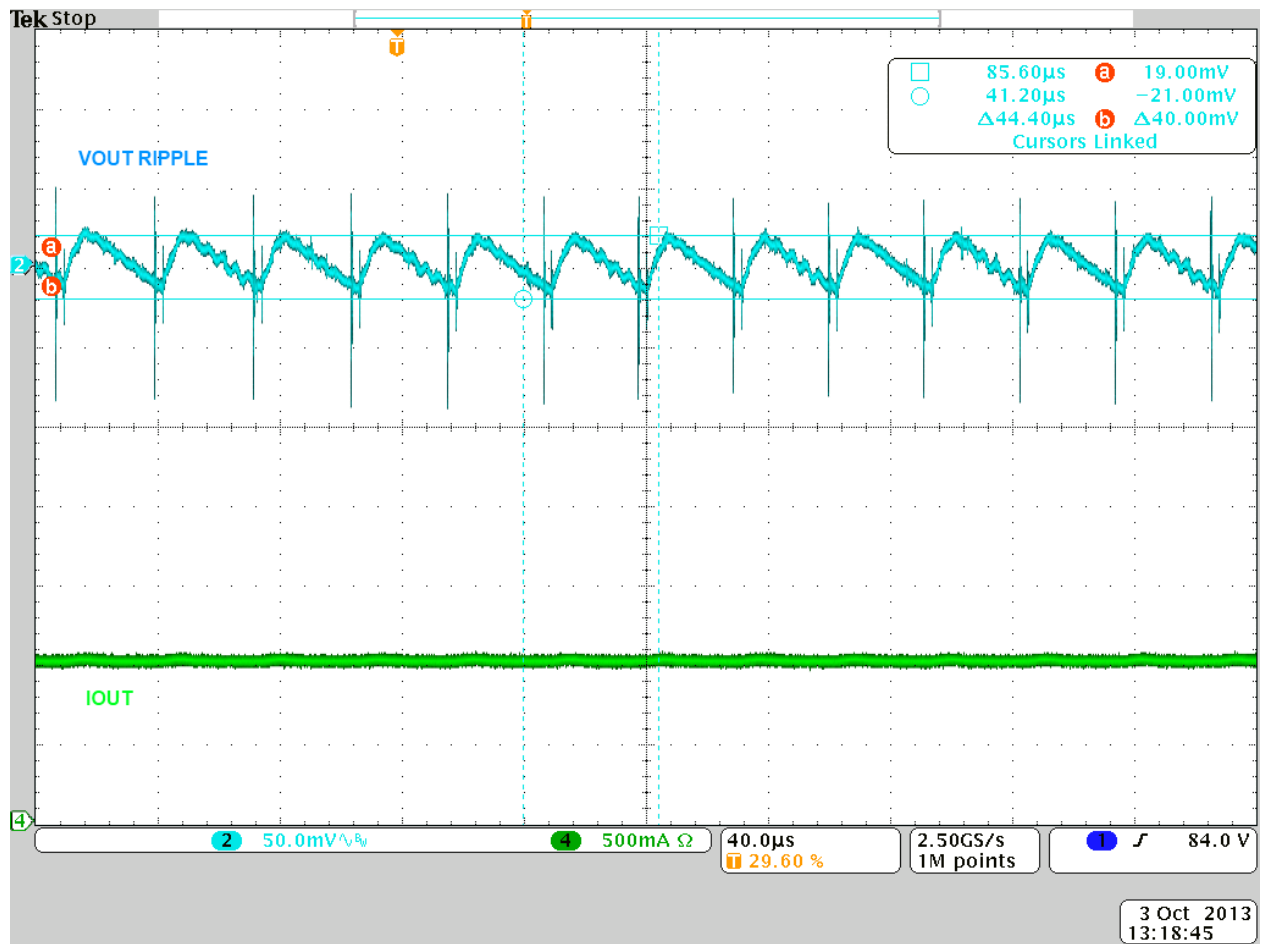


Figure 6. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 1.0 A$, $\Delta V_{OUTPK-PK} = 48 mV$

NCP1249A/B + NCP4355B

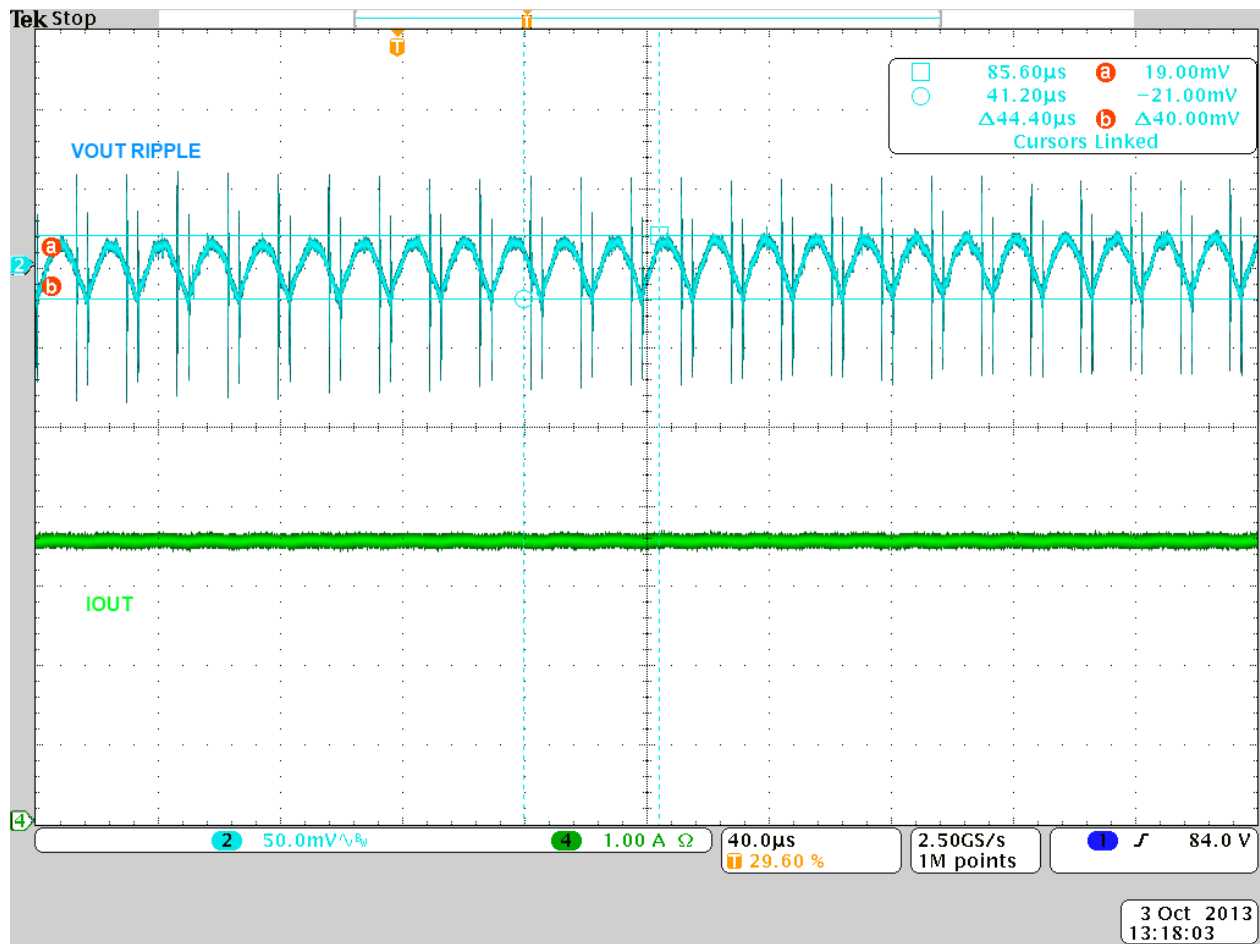


Figure 7. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 3.5 A$, $\Delta V_{OUTPK-PK} = 45 mV$

NCP1249A/B + NCP4355B

Full-load Operation at High-line and Low Line

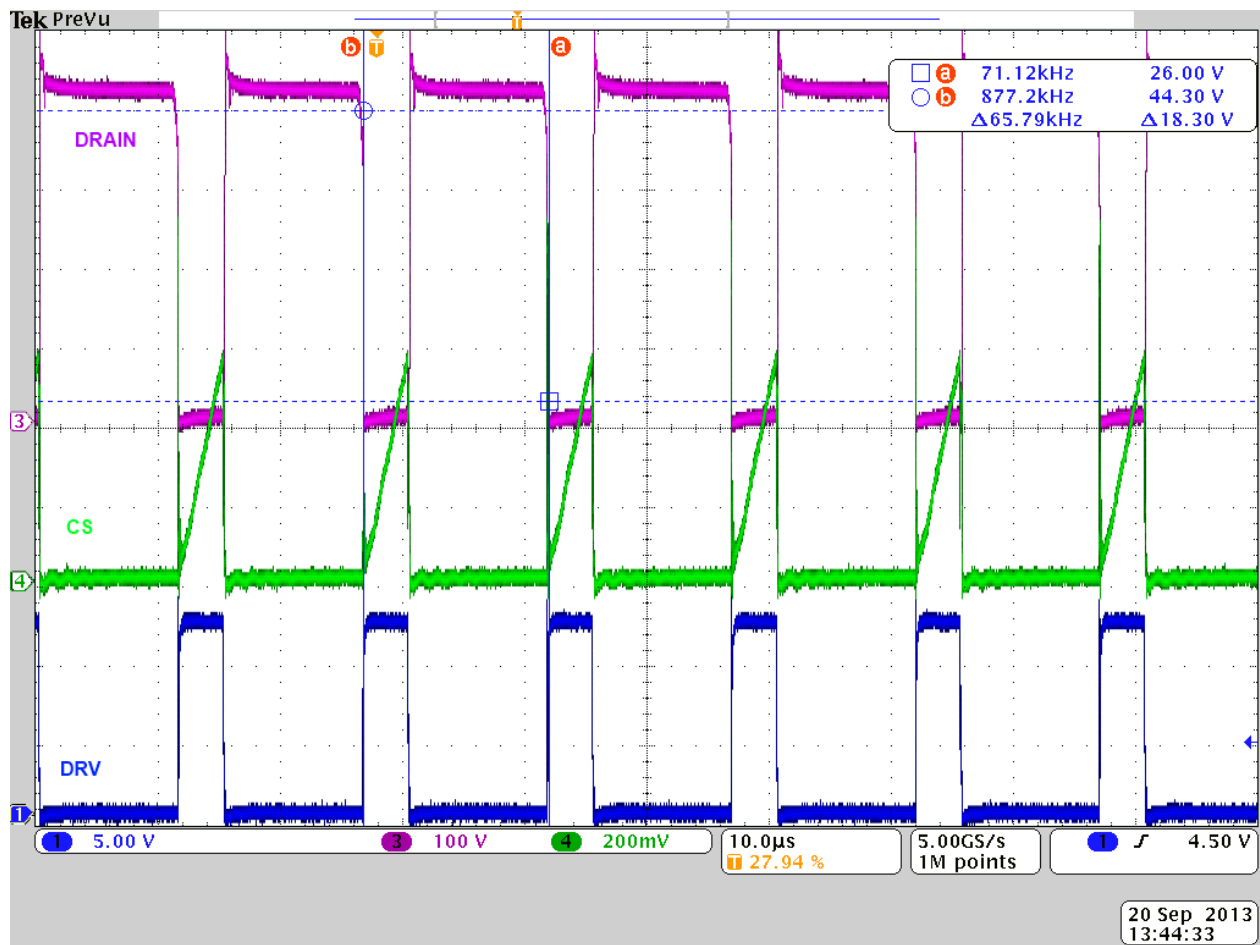


Figure 8. Full Load Operation at High-line, DCM Operation, $V_{IN} = 230 V_{AC}$, $I_{OUT} = 3.5 A$

NCP1249A/B + NCP4355B

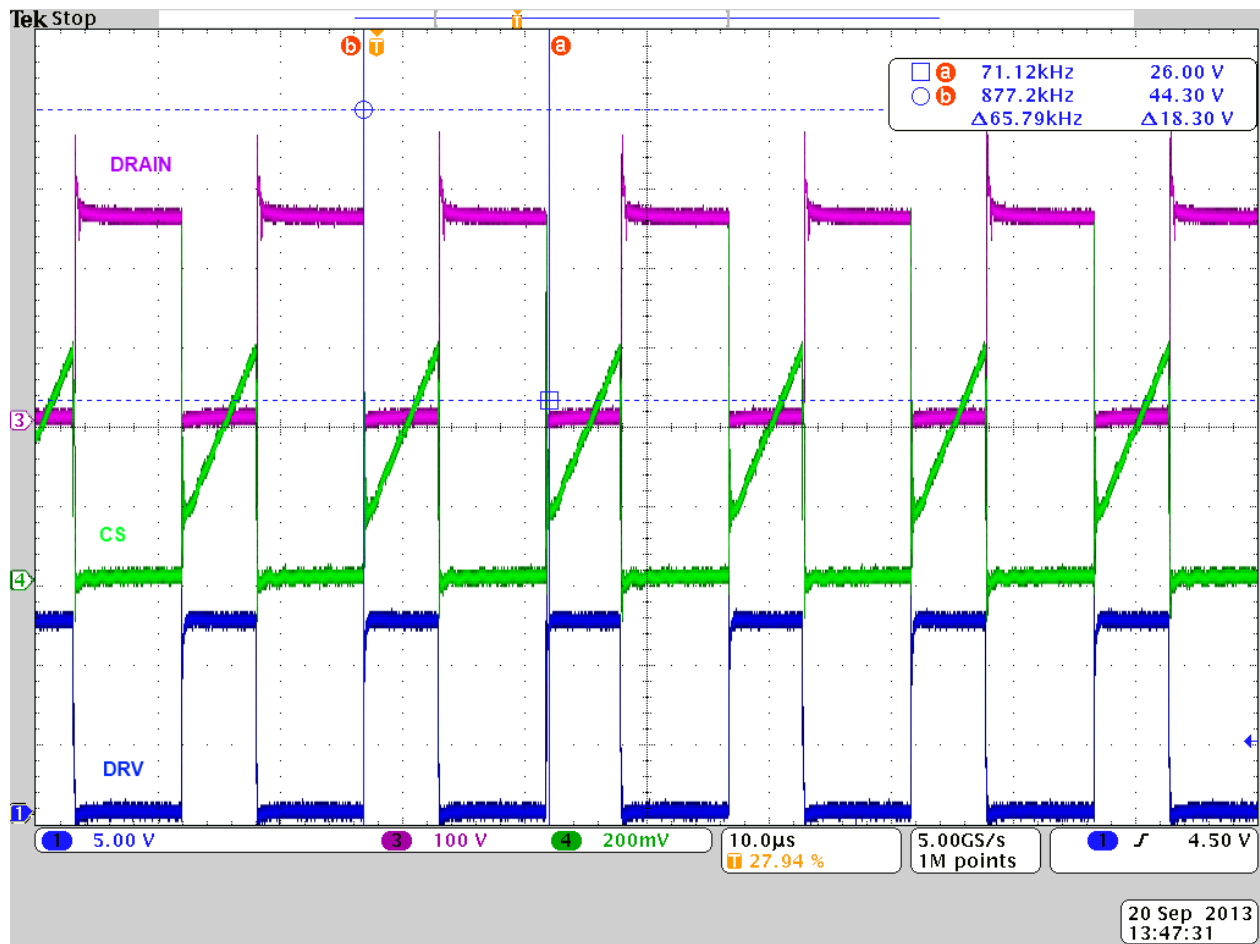


Figure 9. Full Load Operation at Low-line, CCM Operation, $V_{IN} = 115 V_{AC}$, $I_{OUT} = 3.5 A$

Tek Stop
 a 71.12kHz 26.00 V
 b 877.2kHz 44.30 V
 Δ65.79kHz Δ18.30 V

DRAIN
 CS
 DRV

1 5.00 V 3 100 V 4 200mV 10.0μs 27.94 % 5.00GS/s 1M points 1 4.50 V

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High Voltage Start-up

As previously mentioned, the HV startup/X2 discharge of the NCP1249 allows for very low stand-by power consumption levels that cannot be obtained with a classical resistive start-up network. During start up the primary controller NCP1249A/B features a high-voltage current source, which charges the V_{CC} capacitors (C15, C14) at the device start-up. The HV-pin is wired to a full-wave rectified ac input through diodes (D1, D4) and surge protection resistive network R1, R2. Once the device is

plugged into mains the HV pin detects if the input voltage is in a brown-out condition. If the input voltage is higher than V_{BO_on} then the start-up current source is enabled. The V_{CC} capacitors are charged in two steps. To protect HV current source from a short circuit at VCC pin the V_{CC} capacitor is charged with a reduced current I_{start1} until the voltage on the V_{CC} capacitors reach $V_{CC_inhibit}$. Then the source toggles to a full charging current I_{start2} . Once the V_{CC_ON} level is reached the primary controller is turned on and the soft-start sequence is performed.

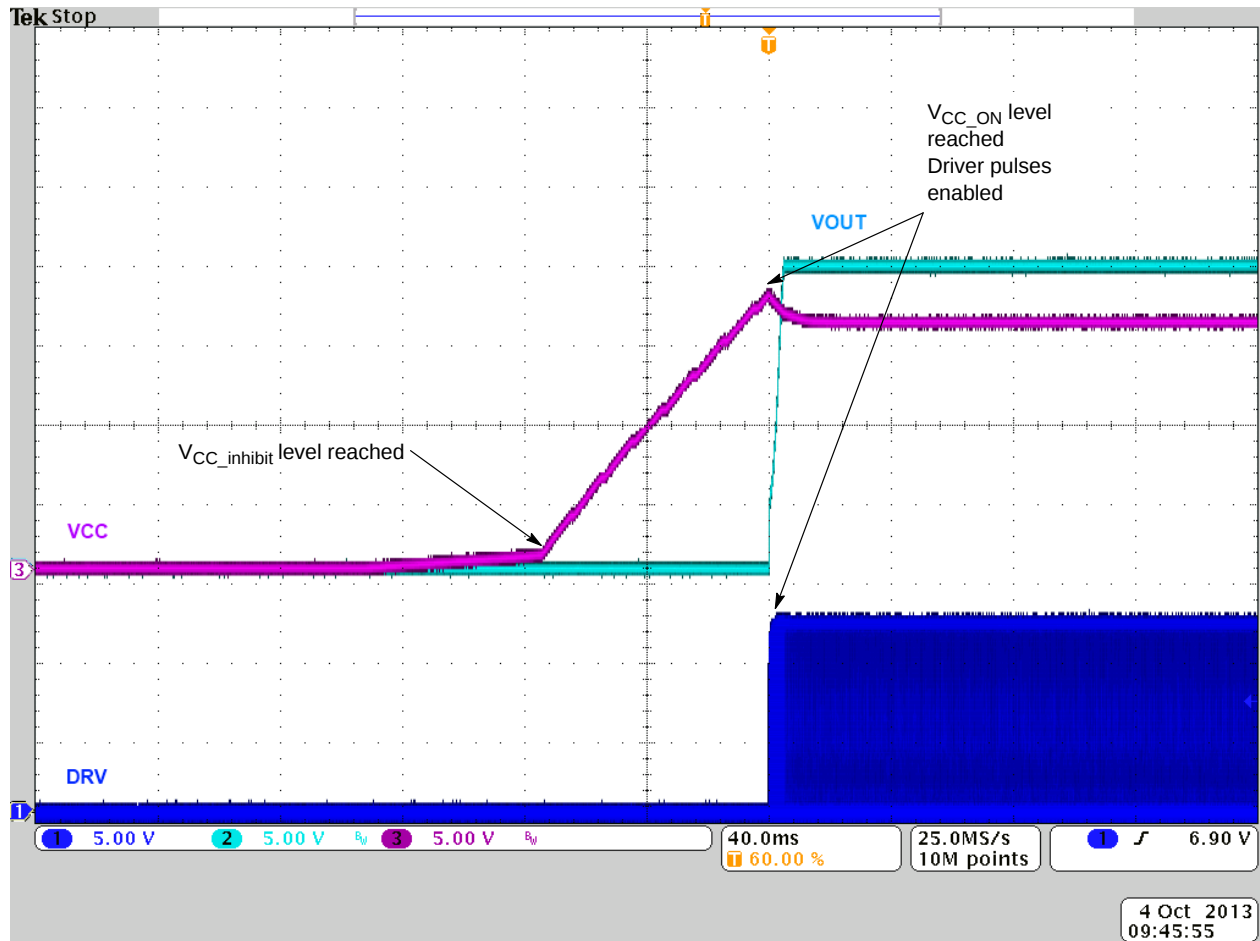


Figure 11. High-Voltage Start-up Source

Peak Power Excursion

The NCP1249 controller family excels in applications that require peak power delivery for a short period of time. In order to handle these peak power requirements the NCP1249 features frequency excursion. In the case that the application requires more power the feedback pin voltage (V_{FB}) increases. When the over-power limit is reached, the feedback pin will have $V_{FB} = V_{OVL} = 3.2$ V, and the current peak is limited to $0.8/R_{sense}$. In order to deliver more power to the output the switching frequency has to be increased.

The switching frequency continues to linearly increase from 65 kHz up to 130 kHz if feedback pin voltage is in an overload region $V_{FB} = 3.2$ V to 4.1 V. The maximum current peak continues to be limited to $0.8/R_{sense}$ which prevents the fly-back transformer core from saturating. This peak-power operation is limited by an over-load timer (Timer1 = 200 ms). Figure 12 shows a response of the controller to a short-term power demand. The output current is increased from 3 A to 6.4 A for a period of 200 ms.

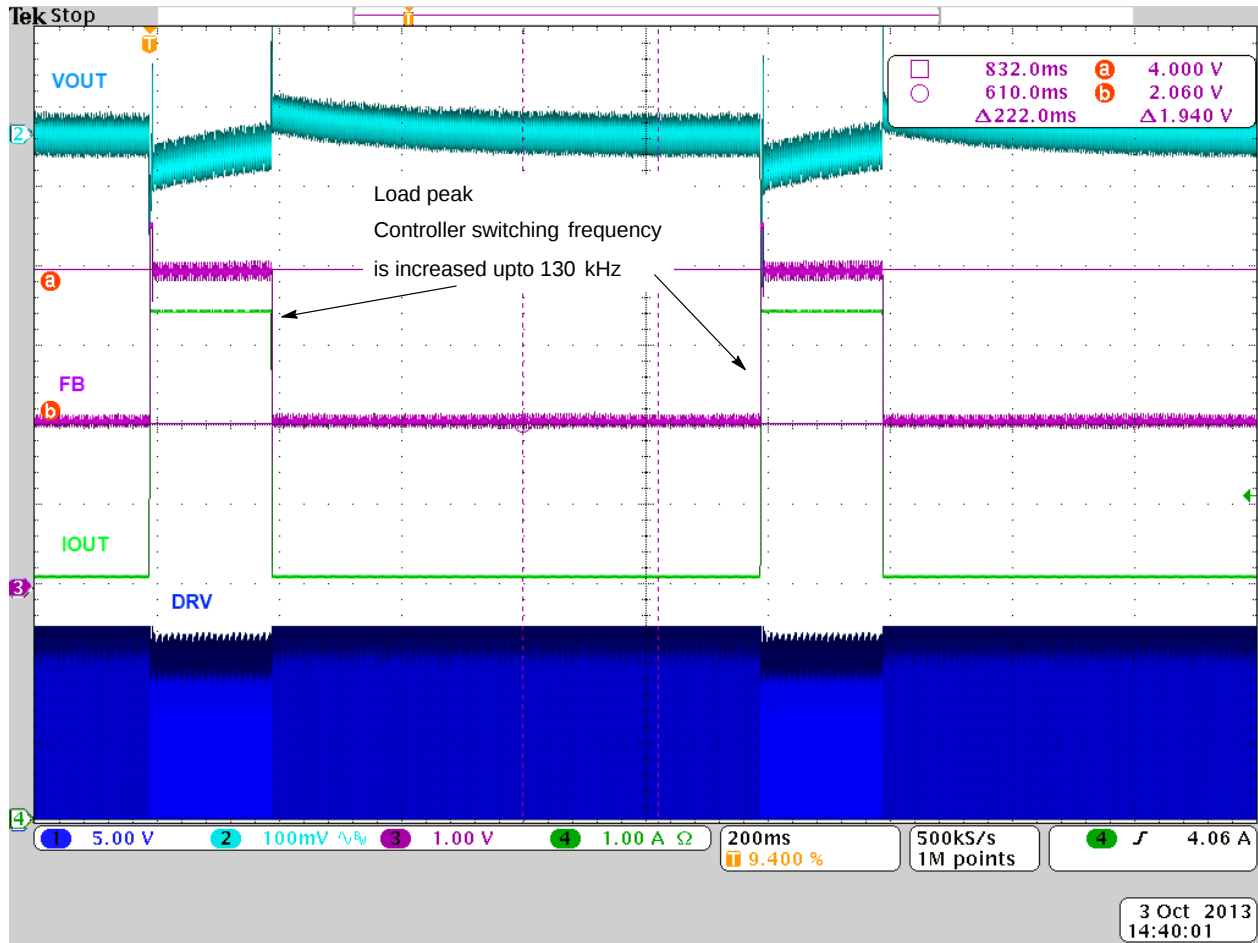


Figure 12. Peak Power Excursion, I_{OUT} Step from 3 A to 6.4 A for 200 ms

NCP1249A/B + NCP4355B

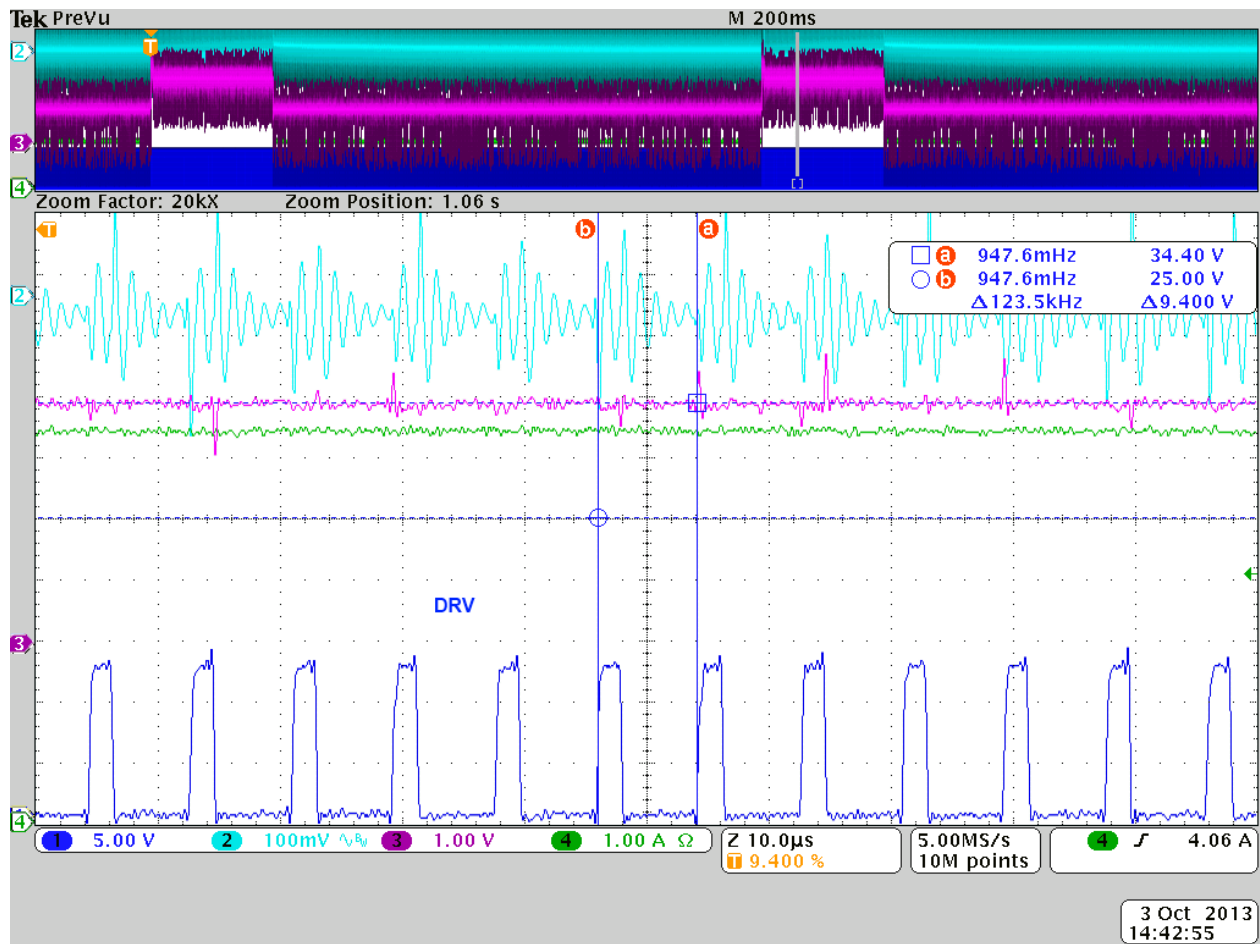


Figure 13. Peak Power Excursion, Detail View, $f_{sw}=123\text{ kHz}$

OFF Mode

The OFF Mode of the NCP4355 is advantageous for systems that require very low no-load power consumption. The OFF mode detection is based on the comparison of the output voltage (on VCC) and the voltage loaded on with fixed resistors (D19, R42, C27, R43 and R44). When the output voltage is loaded with very low current the primary controller goes into skip mode and it stops switching for some time. While the output capacitors are discharged very slowly a fixed load R43 and R44 discharge C27 faster than the load current discharges the output voltage on the output capacitors. The OFF-mode operation is activated in the case that the output current is below a predetermined set level. In this design, the off mode threshold is set to approximately 3.5 mA. This condition is detected by OFFDET comparator built-in NCP4355B secondary side controller. The OFFDET

pin is between the voltage divider created by R43 and R44. The capacitor C27 charging current is limited by R42 to avoid fully recharge by short and sporadic pulses in deep skip mode. When very light load is detected, ON/OFF pin stops sinking the current. The primary controller's REM pin voltage increases and the primary IC goes in to OFF mode.

The OFF mode is interrupted when V_{OUT} is below V_{MIN} level that is detected by VMIN comparator or NCP4355B V_{CC} falls below ULO threshold (3.5 V). ONOFF current starts to flow causing the primary controller's REM voltage decreases via the optocoupler (OK2). When primary REM is below V_{REM_on} level, the primary controller regains operation. The output capacitor is then recharged to the nominal output voltage.

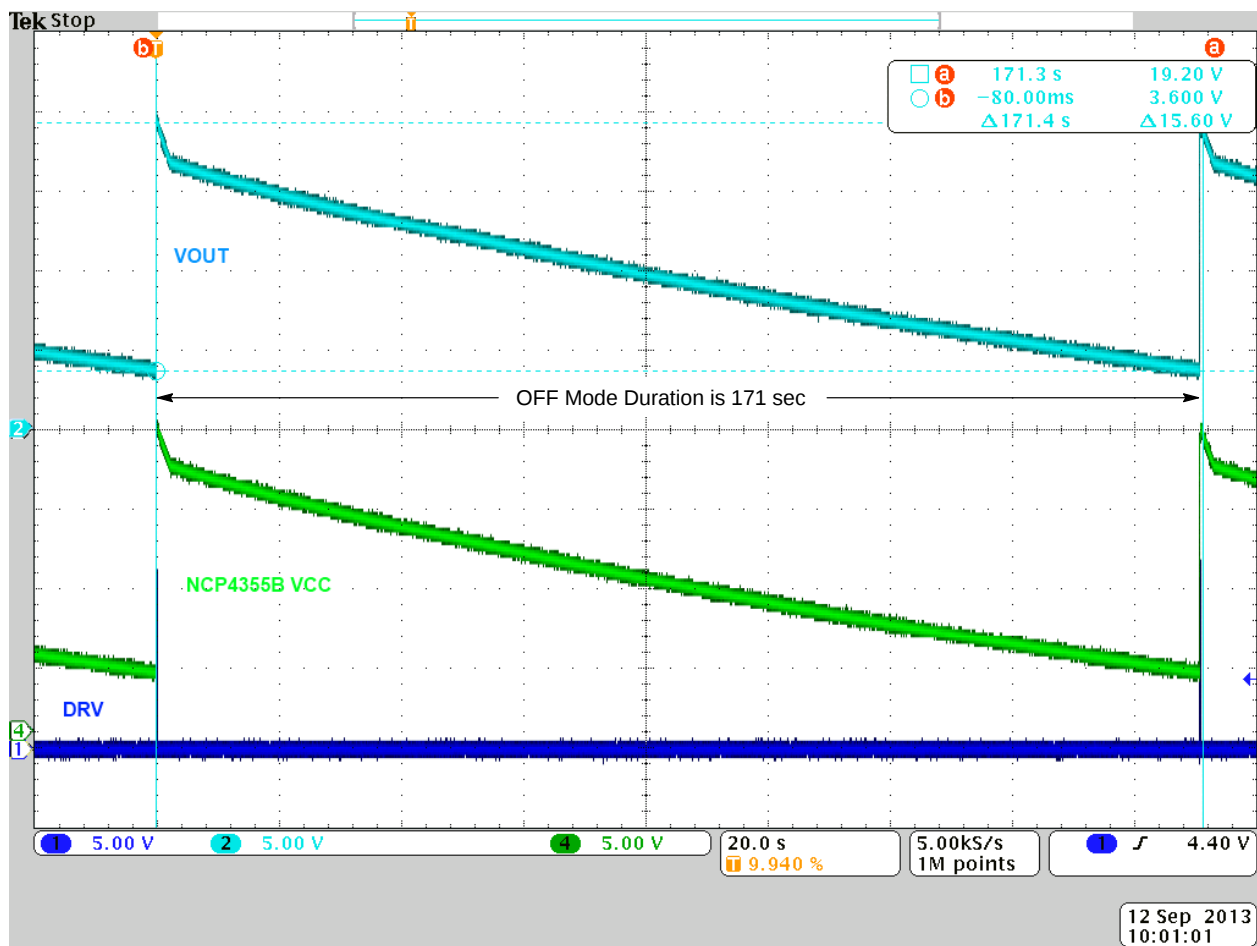


Figure 14. Off Mode Hicup with $I_{out} = 0$ A

Load Detection Speed Up Circuit

When there is no additional speed up circuit, shown in Figure 15, and the SMPS is in OFF mode and a load is connected to its output, the converter output voltage drops to VMIN level then the primary side is switched on and the output voltage is recharged to its nominal level. The output capacitor discharging may take some time that can be, in some applications, unwanted. Alternatively the OFF mode can be easily ended by an OFFDET comparator feature. When OFFDET voltage goes above 10% of VCC voltage it breaks the OFF mode before VMIN voltage is reached. The load detection circuit consists of D16, R20, R40, C24, Q2 and no

R22. When there is no load output capacitors C6, C7, C8 and C9 are discharged slower than the VCC capacitors C24 and C25. These VCC capacitors get recharged from the output capacitors to a voltage $V_{OUT} - V_{D16}$. In the no load condition transistor Q2 is doesn't conduct. When the SMPS is loaded, the output capacitors are discharged by the load faster than VCC capacitors by the I_{CC} current. This will create a reverse voltage drop on diode D16. The voltage on D16 biases Q2 so that it will start to conduct through resistor R40 and change the OFFDET divider. OFFDET voltage increases, then once it crosses 10% of V_{CC} the OFF mode is ended.

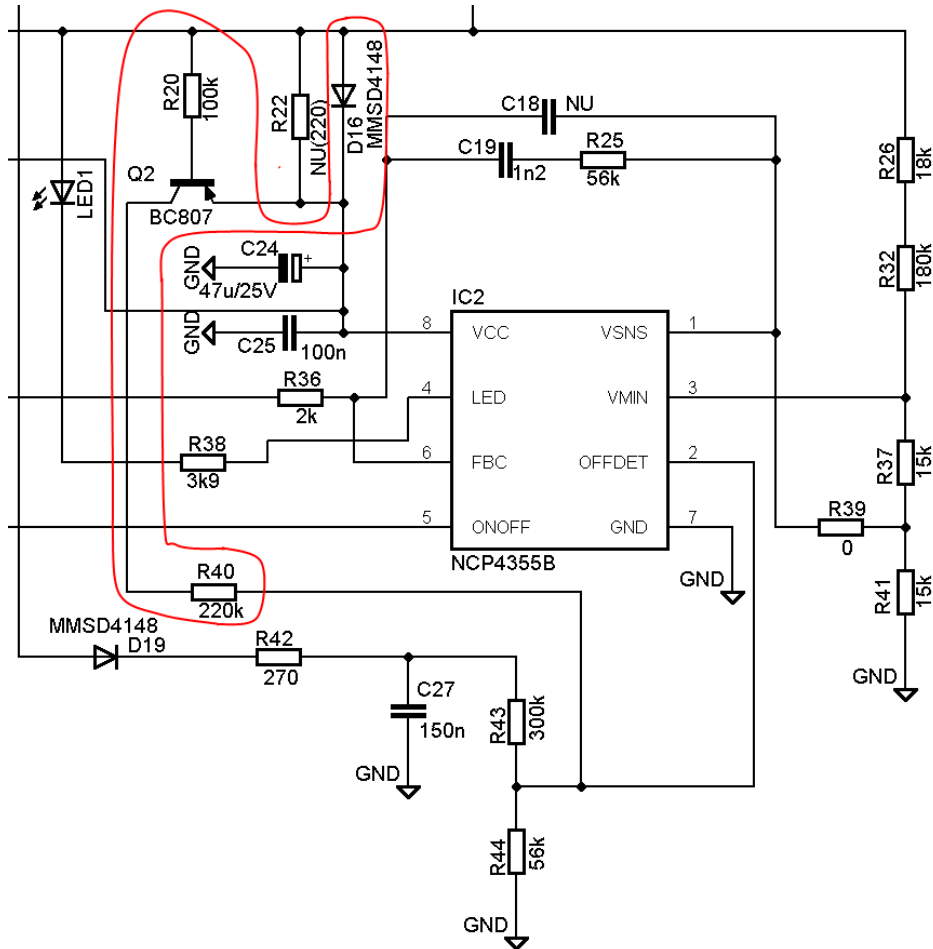


Figure 15. Speed Up Circuit Schematic

NCP1249A/B + NCP4355B

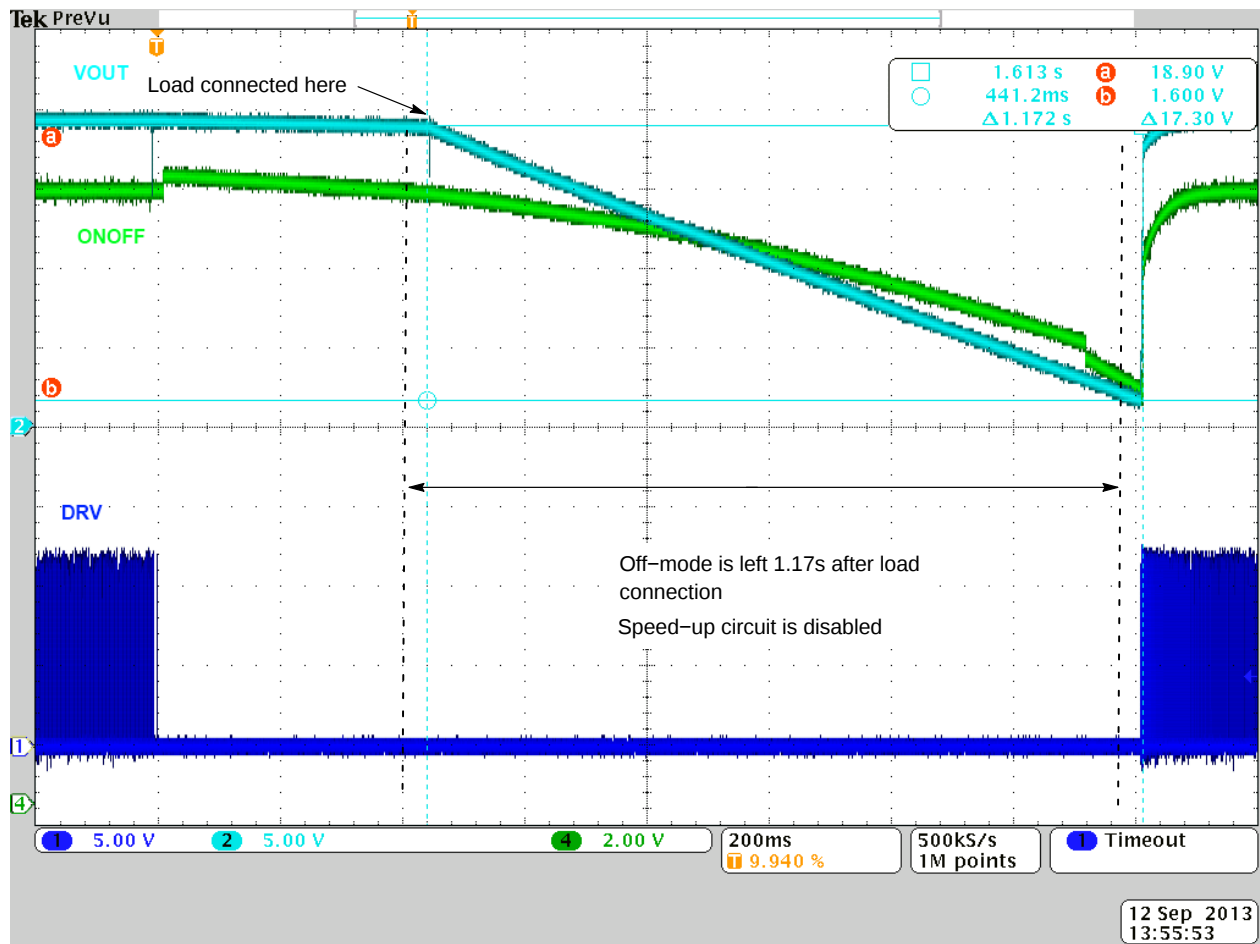


Figure 16. $V_{IN} = 230 \text{ VAC}$, $I_{OUT} = 0 \text{ A} \rightarrow 10 \text{ mA}$, load is connected to the output in off mode, speed-up circuit is disabled

NCP1249A/B + NCP4355B

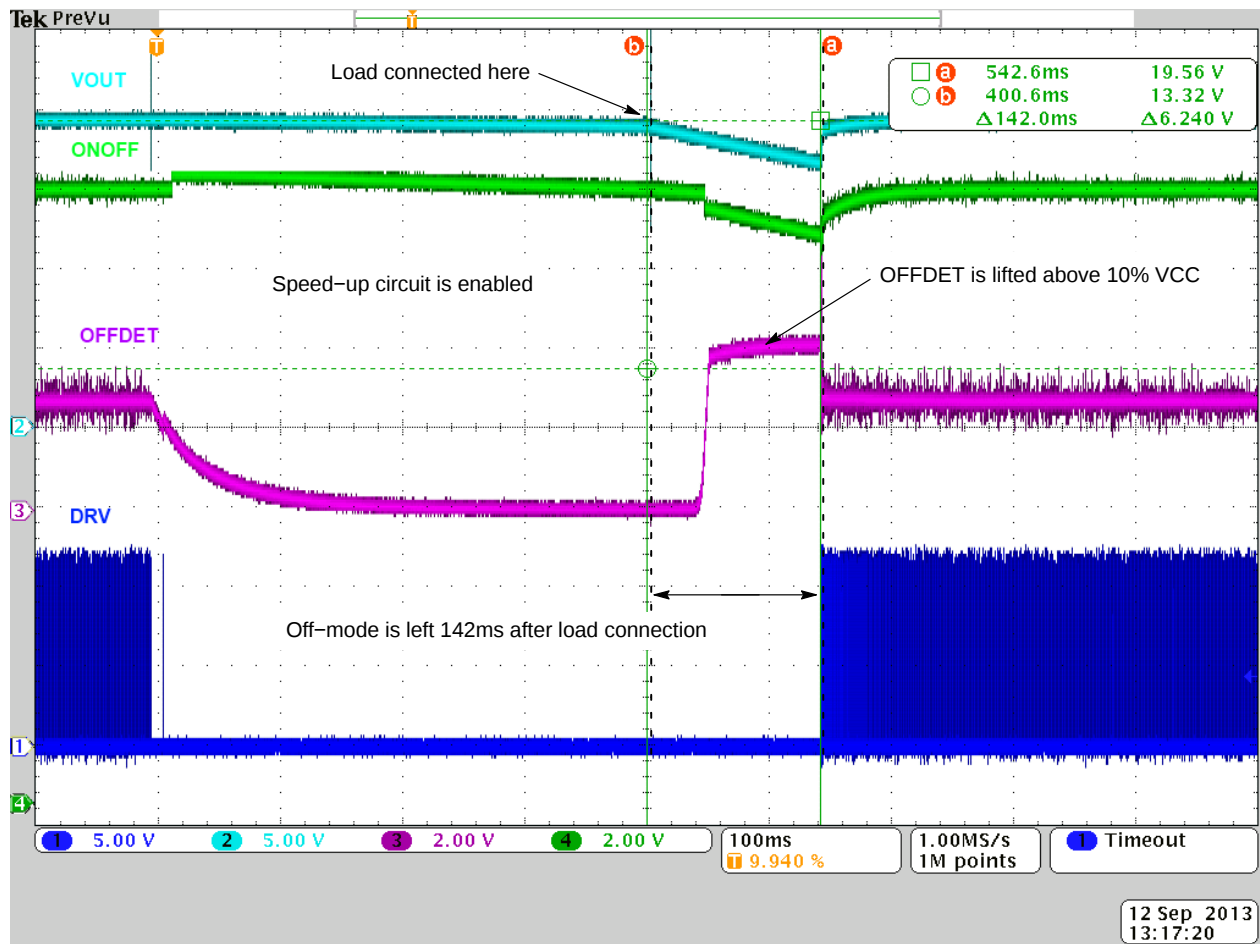


Figure 17. $V_{IN} = 230 \text{ VAC}$, $I_{OUT} = 0 \text{ A} \rightarrow 10 \text{ mA}$, load is connected to the output in off mode, speed-up circuit is enabled

X2 Discharger

The NCP1249 X2 discharge circuitry uses a dedicated pin (X2) together with an external charge pump sensing network to detect whether the application is plugged into the mains or not. The charge pump circuitry consist of resistors R3, R4, R8, R9, capacitors C2, C3 and diodes D5, and D6. If there is an AC voltage present at input terminals the capacitor C3

is being charged via the charge pump circuitry. Once the AC voltage disappears C3 is discharged via R9. Voltage on X2 pin falls below a threshold V_{th_X2} and X2_Timer is enabled. Once the X2_Timer elapses the HV start-up current source is enabled, thus the discharge paths for X2 capacitor is created.

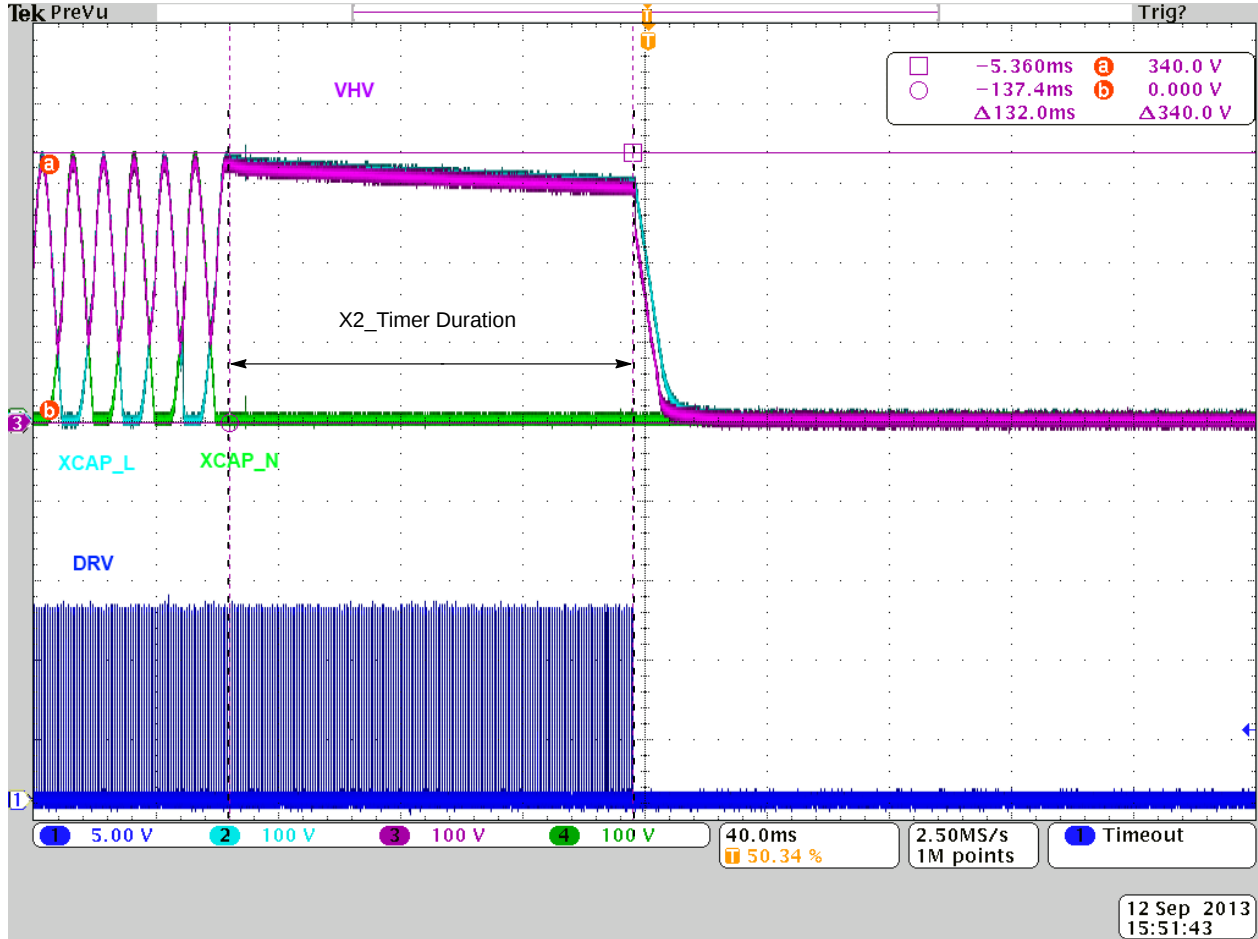


Figure 18. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 1.0 A$, when main is disconnected 132 ms hold-off time is started, after this time X2 cap is discharged. Discharging time is much shorter than is needed by norm ($\sim 150 ms \ll 1 s$)

NCP1249A/B + NCP4355B

Load Transient Response

Current slew rate is 125 mA/1 μ s for all transients.

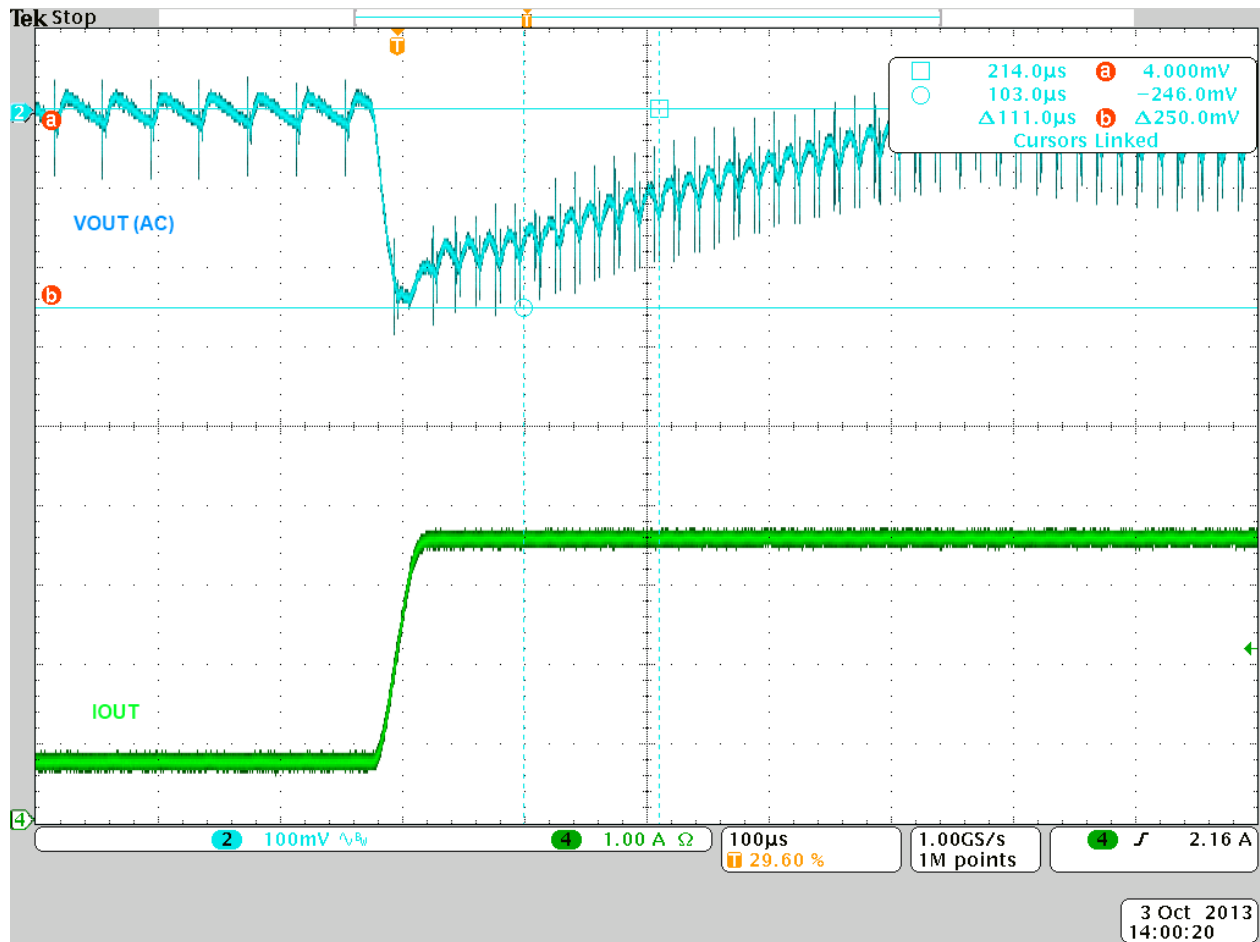


Figure 19. Load step-up from 20% to 100% I_{OUT} , $V_{IN} = 230 V_{AC}$, $V_{OUT_DROP} = 250 mV$

NCP1249A/B + NCP4355B

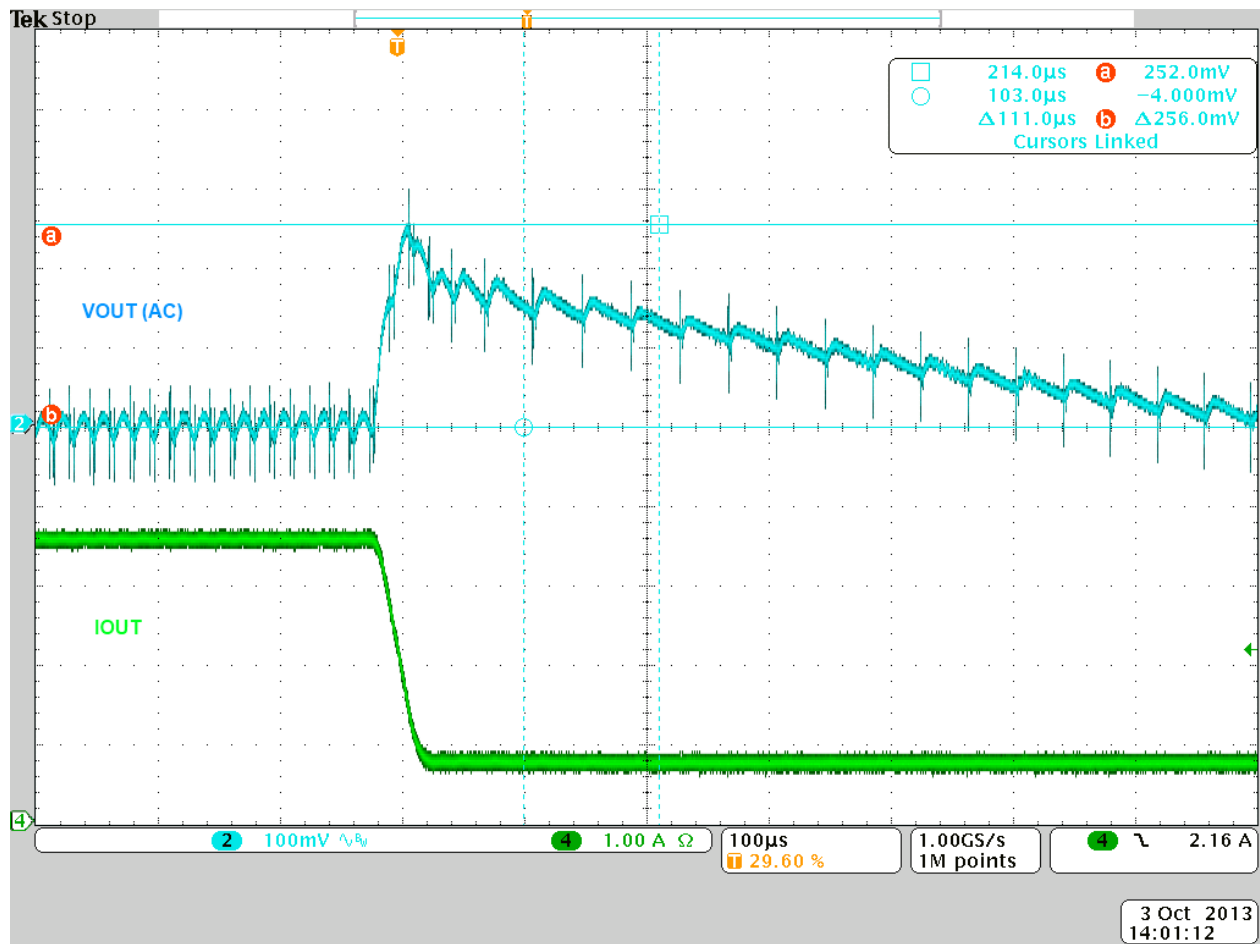


Figure 20. Load step-down from 100% to 20% I_{OUT} , $V_{\text{IN}} = 230 \text{ V}_{\text{AC}}$, $V_{\text{OUT_OVERSHOOT}} = 256 \text{ mV}$

NCP1249A/B + NCP4355B

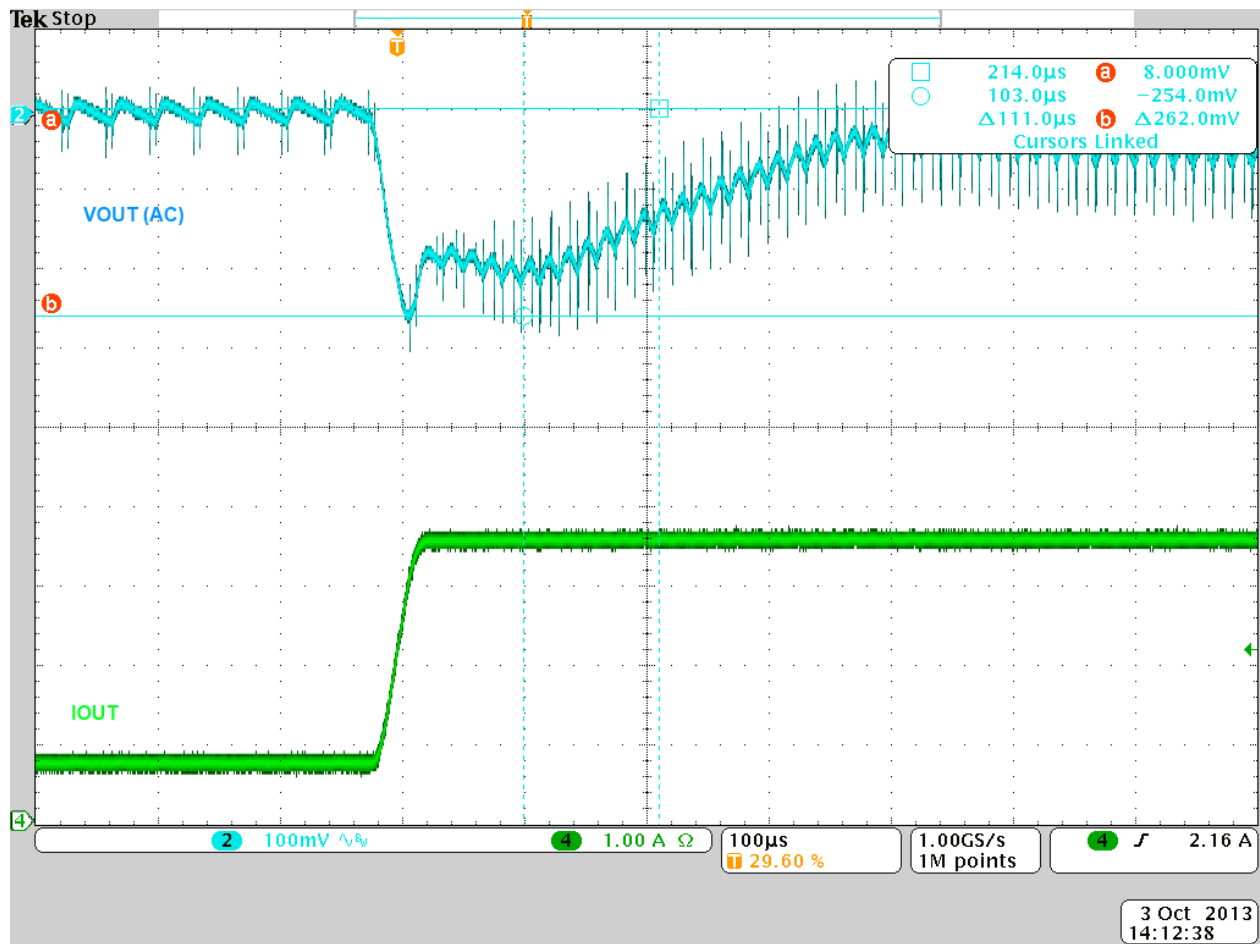


Figure 21. Load step-up from 20% to 100% I_{OUT} , $V_{IN} = 115 V_{AC}$, $V_{OUT_DROP} = 256 mV$

NCP1249A/B + NCP4355B

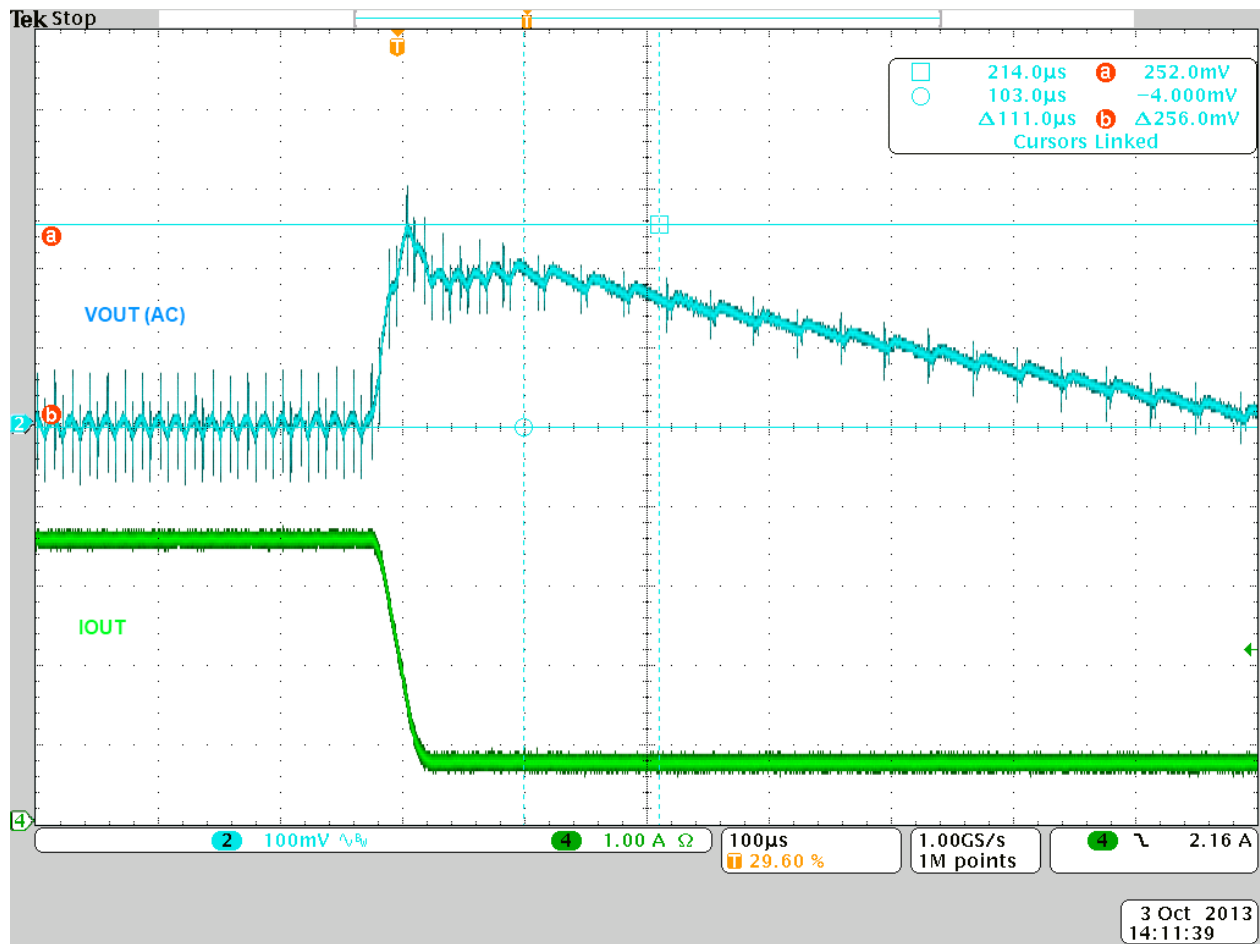


Figure 22. Load step-down from 100% to 20% I_{OUT} , $V_{IN} = 115$ V_{AC}, $V_{OUT_OVERSHOOT} = 256$ mV

NCP1249A/B + NCP4355B

Gain Phase Characteristics

Voltage Control Loop

- Phase margin is never lower than 50°
- Gain margin is never lower than 13 dB
- Crossover frequency is between 0.6 – 0.75 kHz
- The phase-gain charts for various load conditions can be seen in figures below.

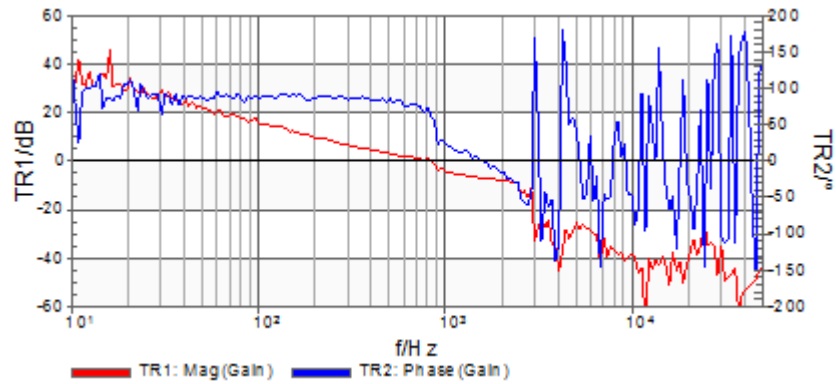


Figure 23. $V_{IN} = 115 V_{AC}$, $I_{OUT} = 100 \text{ mA}$

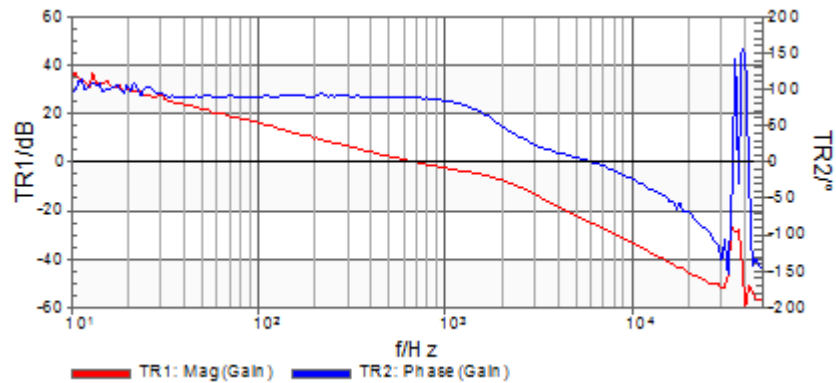


Figure 24. $V_{IN} = 115 V_{AC}$, $I_{OUT} = 1.0 \text{ A}$

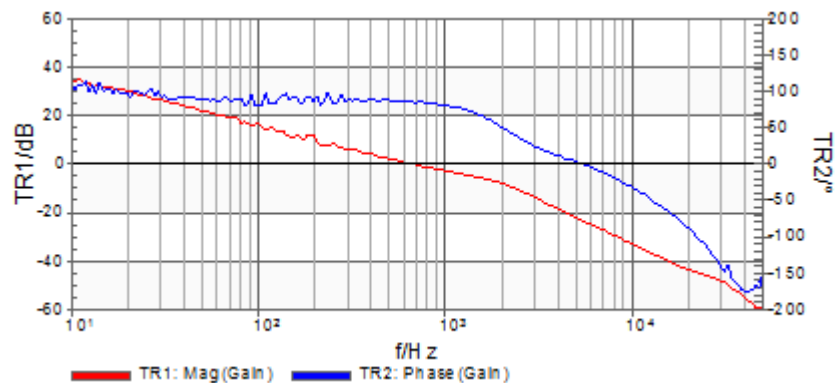


Figure 25. $V_{IN} = 115 V_{AC}$, $I_{OUT} = 3.5 \text{ A}$

NCP1249A/B + NCP4355B

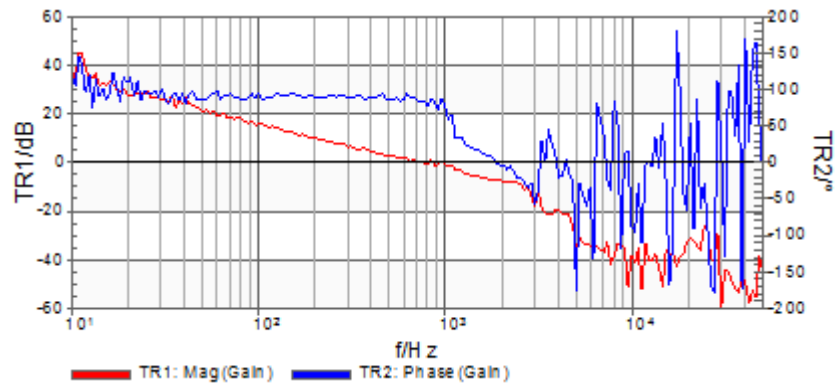


Figure 26. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 100 \text{ mA}$

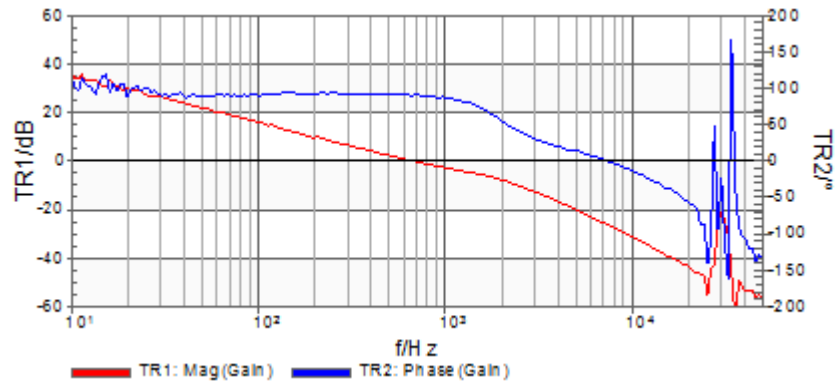


Figure 27. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 1.0 \text{ A}$

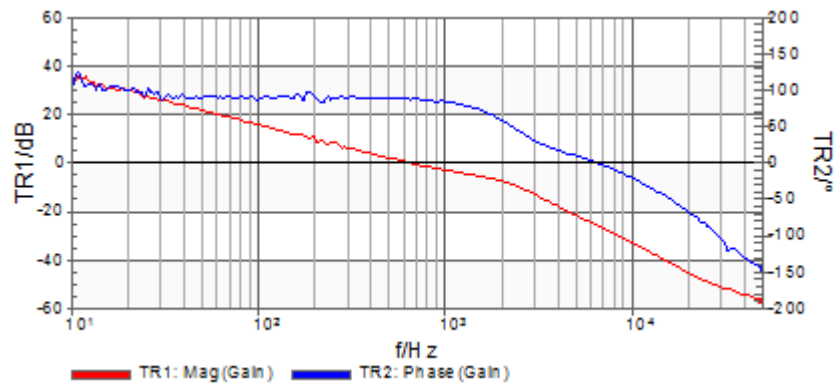


Figure 28. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 3.5 \text{ A}$

Conducted Emission Quasi-peak

The design meets conducted electromagnetic interference international standards for domestic use.

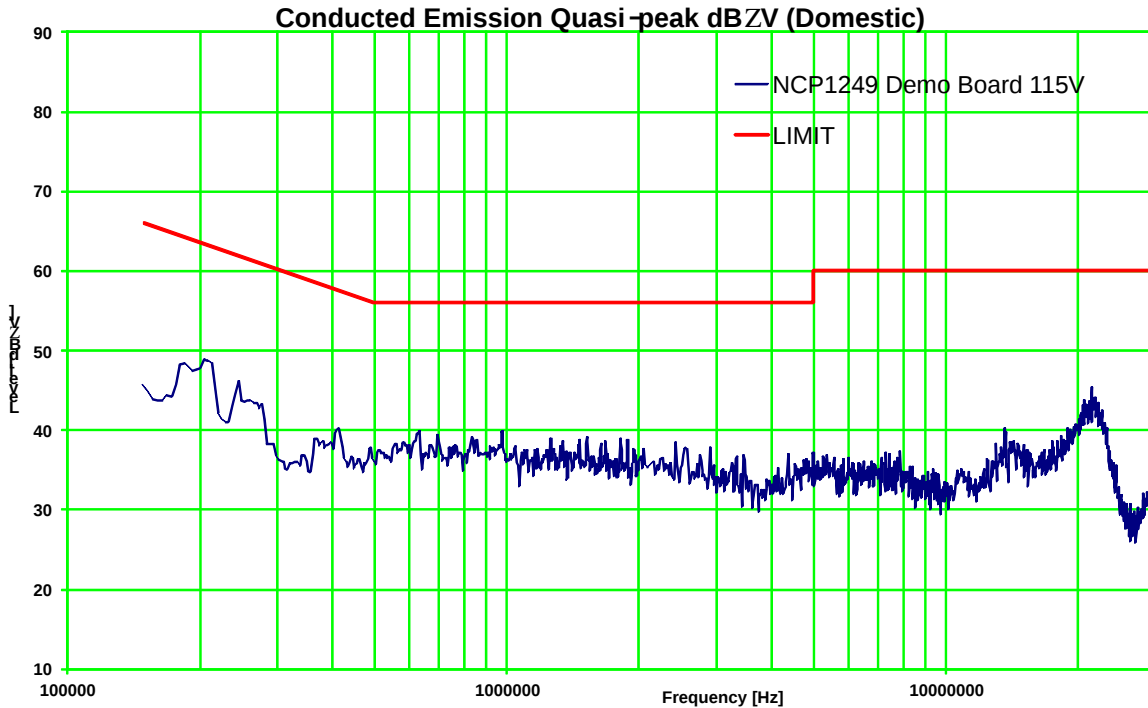


Figure 29. $V_{IN} = 115 V_{AC}$, $I_{OUT} = 3.5 A$

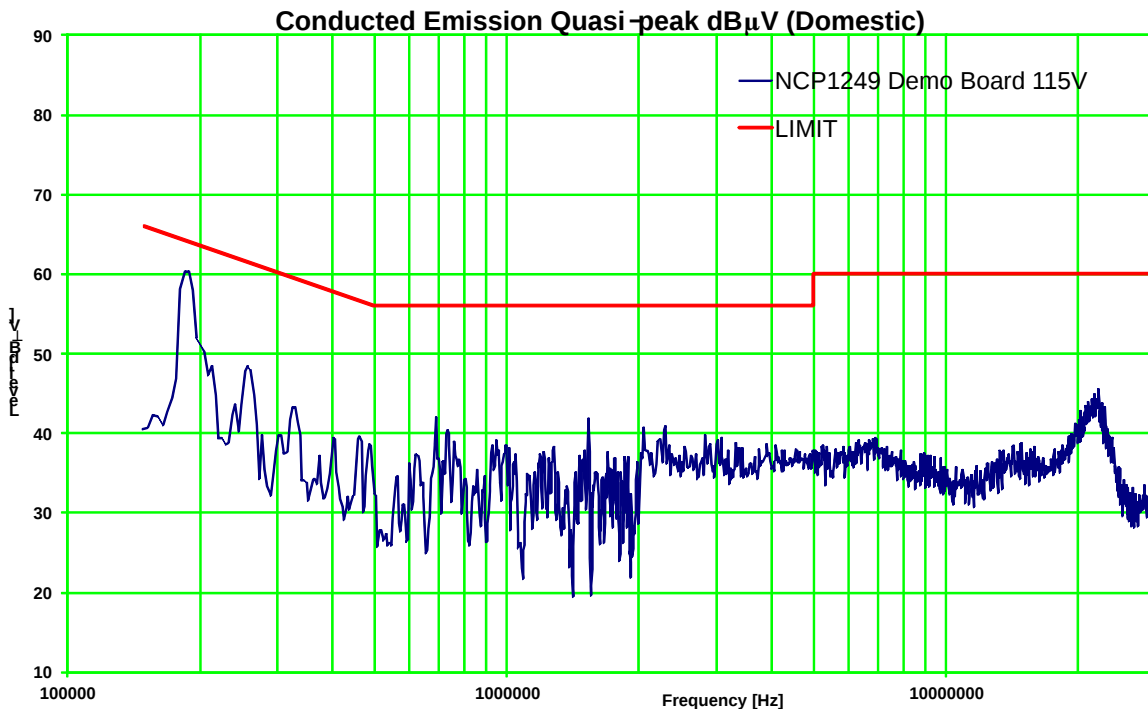


Figure 30. $V_{IN} = 230 V_{AC}$, $I_{OUT} = 3.5 A$

Result Summary

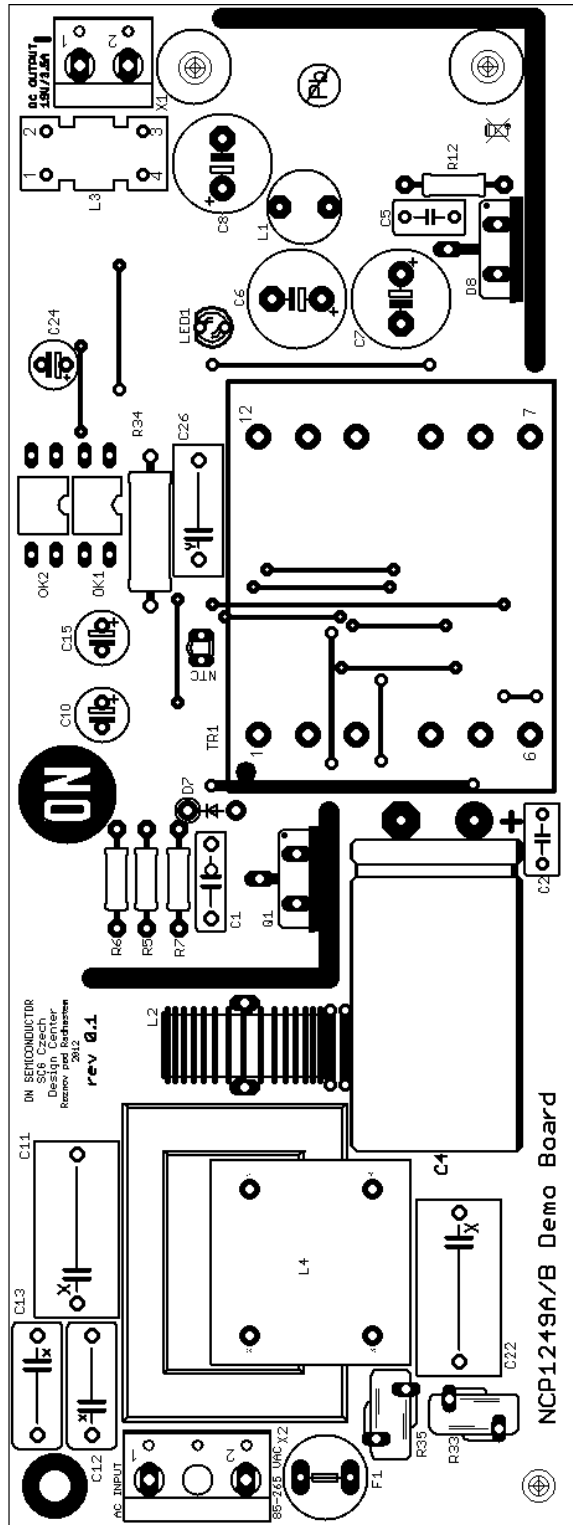
NCP1249A/B and NCP4355B controllers allow building cost effective, easy to design, high efficiency power supplies with very low no load input consumption. The presented demo board offers both an extraordinary no-load consumption and superb efficiency. The frequency

excursion feature perfectly fits applications where it is necessary to cover short peak power demand like printers, game stations, and others.

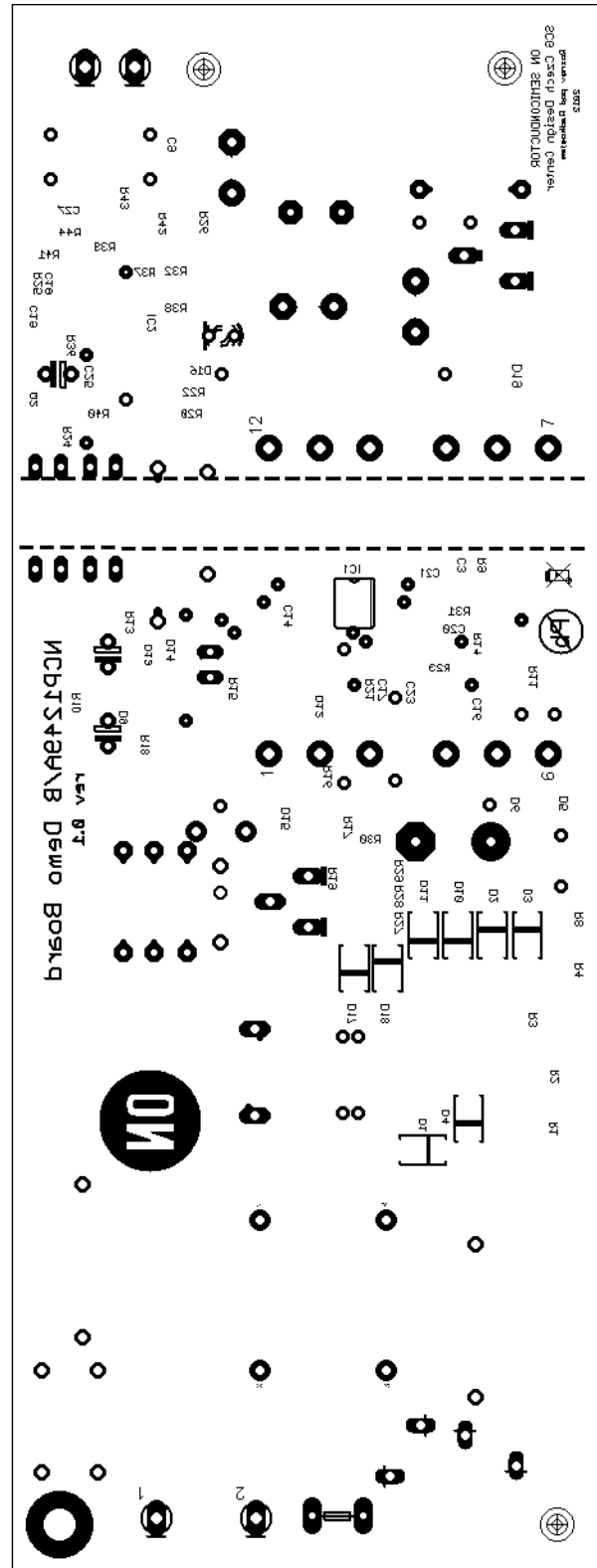
Special thanks go to companies Coilcraft, Epcos and Würth that provided samples of their components for this demoboard.

NCP1249A/B + NCP4355B

Top Side Assembly



Bottom Side Assembly



NCP1249A/B + NCP4355B

Demo Board Photo



NCP1249A/B + NCP4355B

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