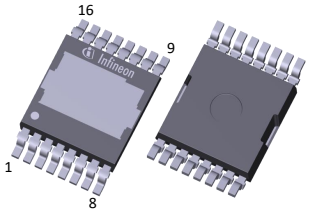
CoolGaN™ G5

CoolGaN™ Transistor 650 V G5

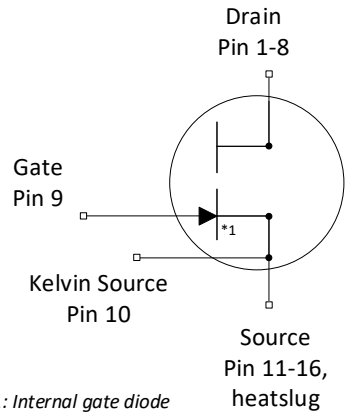
Infineon's CoolGaN™ is a highly efficient gallium nitride (GaN) transistor designed for power conversion at 650 V. It enables higher power density, supports reduced system BOM cost, and facilitates miniaturized form factors. Produced using 200 mm (8 inch) wafer technology and fully automated production lines, it features narrow production tolerances and the highest product quality. This makes it suitable for a wide range of applications, from consumer electronics to industrial applications.

TOLT



Features

- Enhancement mode transistor
- Ultra-fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate and output charge
- Superior commutation ruggedness
- 2 kV HBM ESD standards



**1: Internal gate diode*

Benefits

- Normally OFF transistor technology ensures safe operation
- Enables rapid and precise power delivery control
- Improves system efficiency and reliability
- Ensures robust performance under challenging conditions

These features collectively make CoolGaN™ a game-changer in the realm of power conversion, offering a compelling combination of efficiency, compactness, and reliability.

Potential applications

Industrial, telecom, datacenter SMPS based on half-bridge hard and soft switching topologies such as totem pole PFC and high frequency LLC, as well as charger and adapter.

Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS,max}$	650	V
$V_{DS,trans-max}$	900	V
$R_{DS(on),max}$	140	mΩ
$Q_{g,typ}$	2.4	nC
$I_{D,pulse}$	30	A
Q_{oss} @ 400 V	18	nC
Q_{rr}	0	nC

Part number	Package	Marking	Related links
IGLT65R110D2	PG-HDSOP-16	65R110D2	see Appendix A

Table of contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80% of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain source voltage, continuous	$V_{DS,max}$	-	-	650	V	V_{GS} = 0 V; derating recommendation according JEDEC JEP198
Leakage current at drain source transient voltage	$I_{DS,trans}$	-	-	6.2	mA	V_{GS} = 0 V; $V_{DS,trans}$ = 900 V
Drain source voltage transient	$V_{DS,trans}$	-	-	900	V	<1% duty cycle; <1 µs; 1 million pulses
Drain source voltage, pulsed	$V_{DS,pulsed}$	-	-	750	V	T_j = 25°C; V_{GS} ≤ 0 V; cumulated stress time ≤ 10 h
						T_j = 125°C; V_{GS} ≤ 0 V; cumulated stress time ≤ 1 h
Switching surge voltage, pulsed	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse}$ = 750 V; turn on $I_{D,pulse}$ =13 A; f ≤ 100 kHz; T_j = 105°C; t ≤100 s (10 million pulses)
Continuous current, drain source [1]	I_D	-	-	15	A	T_C=25°C; T_j = $T_{j,max}$
Pulsed current, drain source [2]	$I_{D,pulse}$	-30	-	30	A	T_j=25°C; I_G=13 mA; See Diagram 3, 5
		-18		18		T_j=125°C; I_G=13 mA; See Diagram 4, 6
Gate current, continuous [3]	$I_{G,avg}$	-	6.0	10	mA	T_j=-55°C to T_j=150°C; See Table 9
Gate current, pulsed [3]	$I_{G,pulsed}$	-1	-	1	A	T_j=-55°C to T_j=150°C; t_{pulse}= 50 ns; f = 100 kHz; See Table 9
Gate source voltage, continuous [3]	V_{GS}	-10	-	-	V	T_j=-55°C to T_j=150°C; See Diagram 12
Gate source voltage, pulsed [3]	$V_{GS,pulse}$	-25	-	-	V	T_j=-55°C to T_j=150°C; t_{pulse}= 50 ns; f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	55	W	T_C=25°C
Operating junction temperature	T_j	-55	-	150	°C	-
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions
Drain-source voltage slew-rate	dv/dt	-	-	200	V/ns	-

1) Limited by $T_{j,max}$. Maximum duty cycle D = 0.75

2) Defined by design. Not subject to production test.

3) Consider the influence of the gate current (I_G) on the drain current (I_D). For further details, see Table 10 (related links) and refer to the Gate Drive Application Note and the Reliability White Paper, or contact your local Infineon sales office.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.3	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	94	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	68	°C/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thickness) copper area. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless specified otherwise

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9	1.2	1.6	V	I_{DS}=1.3 mA; V_{DS}=10 V; T_j=25°C
		-	1	-		I_{DS}=1.3 mA; V_{DS}=10 V; T_j=150°C
Gate-Source reverse clamping voltage	$V_{GS,\ clamp}$	-	-	-8	V	I_{GS}=-1 mA
Drain-Source leakage current	I_{DSS}	-	0.51	51	µA	V_{DS}=650 V; V_{GS}=0 V; T_j=25°C
			10	-		V_{DS}=650 V; V_{GS}=0 V; T_j=150°C
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.110	0.140	Ω	I_G=13 mA; I_D=4.0 A; T_j=25°C
			0.240	-		I_G=13 mA; I_D=4.0 A; T_j=150°C
Gate resistance [4]	$R_{G,int}$	-	0.96	-	Ω	LCR impedance measurement; f=f_{res}, open drain

[4] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Defined by design. Not subject to production test.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	170	-	pF	V_{GS}=0 V; V_{DS}=400 V; f=1 MHz
Output capacitance	C_{oss}		29			
Reverse transfer capacitance	C_{rss}		0.39			
Effective output capacitance, time related [5]	$C_{o(tr)}$	-	45	-	pF	V_{GS}=0 V; V_{DS}=0 to 400 V; I_D=const
Effective output capacitance, energy related [6]	$C_{o(er)}$	-	33	-	pF	V_{DS}=0 to 400 V
Output charge	Q_{oss}		18	-	nC	
Coss stored energy	E_{oss}		2.6	.	µJ	
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	I_D= 4 A; R_{ON}=10 Ω; R_{OFF}=10 Ω; R_{SS}=680 Ω; C_C=1.5 nF; V_{DRV}=12 V; see Table 8
Turn-off delay time	$t_{d(off)}$		10			
Rise time	t_r		7			
Fall time	t_f		20			

[5] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

[6] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate charge [7]	Q_G	-	2.4	-	nC	V_{GS}=0 to 3 V; V_{DS}=400 V; I_D=4.0 A

[7] Defined by design. Not subject to production test.

Table 7 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.0	2.4	V	V_{GS}=0 V; I_{SD}=4 A
Pulsed current, reverse	$I_{SD,pulse}$	-	-	30	A	I_G=13 mA
Reverse recovery charge [8]	Q_{rr}	-	0	-	nC	I_{SD}=4 A; V_{DS}=400 V

[8] Defined by design. Not subject to production test. Excluding Qoss.

4 Electrical characteristics diagrams

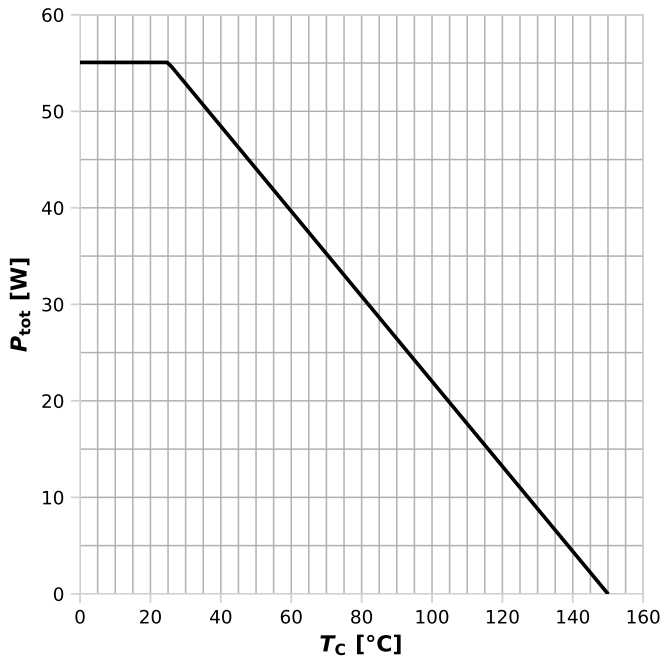
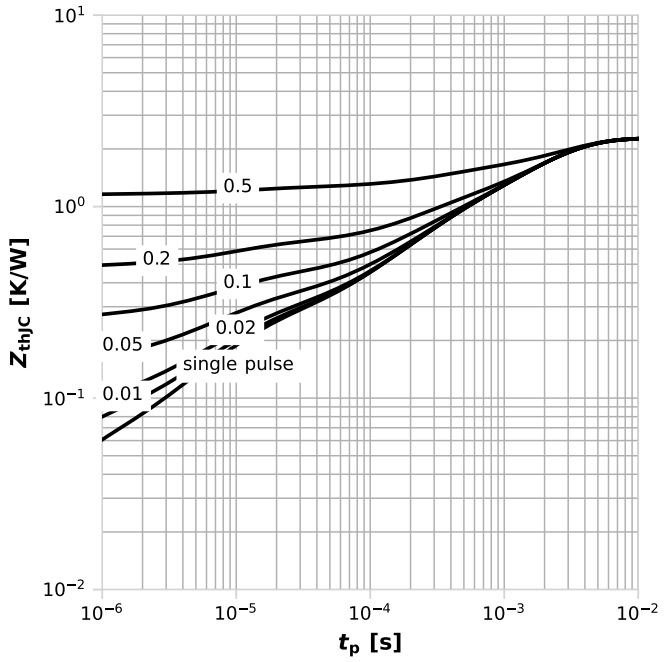
Diagram 1: Power dissipation	Diagram 2: Max. transient thermal impedance
	
P_{tot}=f(T_C)	Z_{thJC} =f(t_P); parameter: D=t_p/T

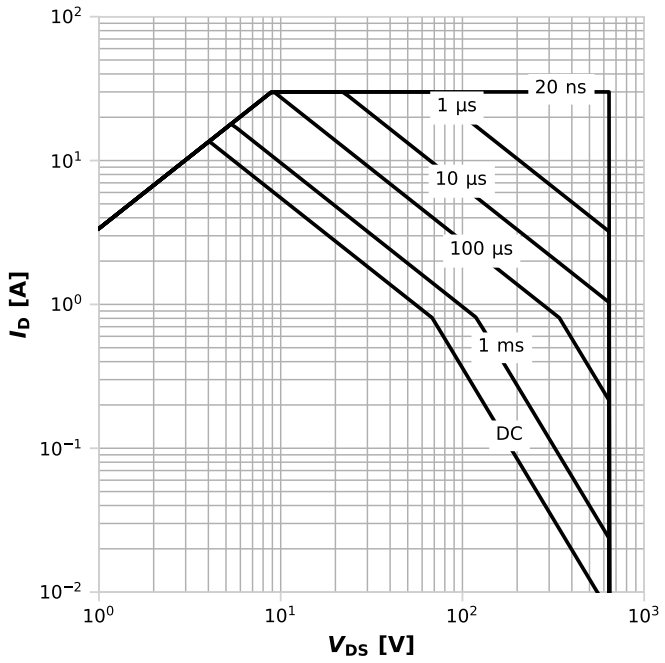
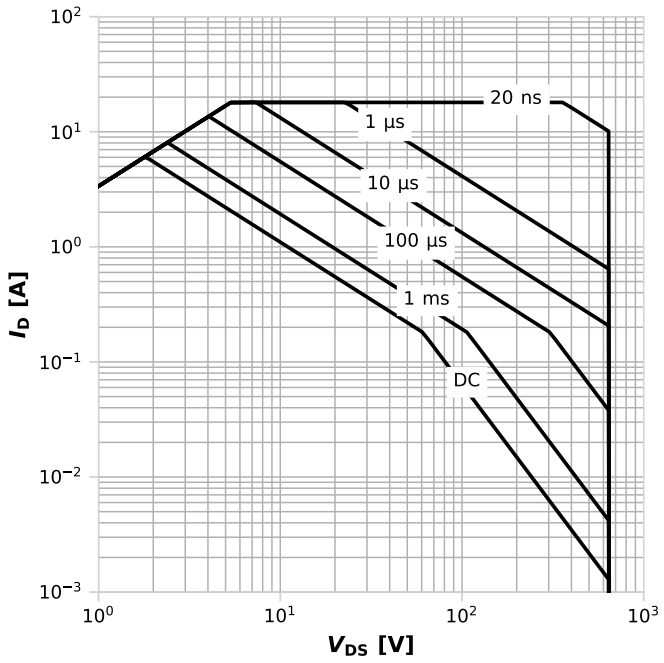
Diagram 3: Safe operating area	Diagram 4: Safe operating area
	
I_D=f(V_{DS}); T_C=25°C; D=0; parameter: t_p	I_D=f(V_{DS}); T_C=125°C; D=0; parameter: t_p

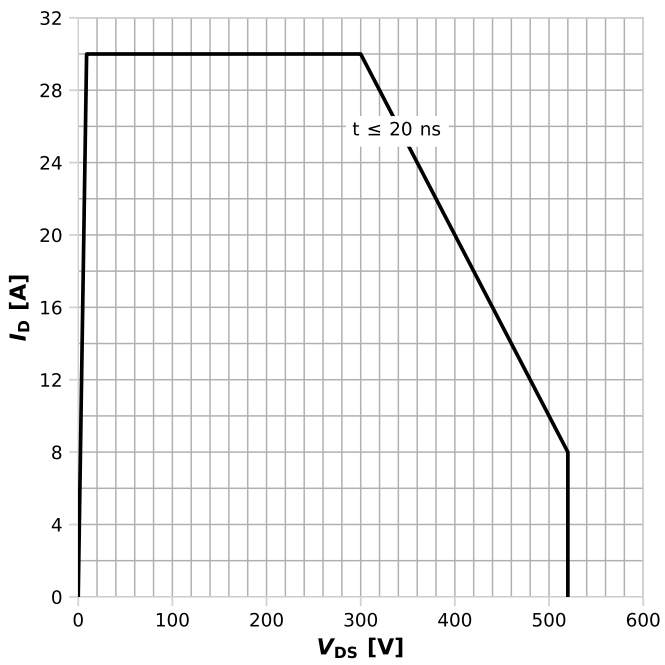
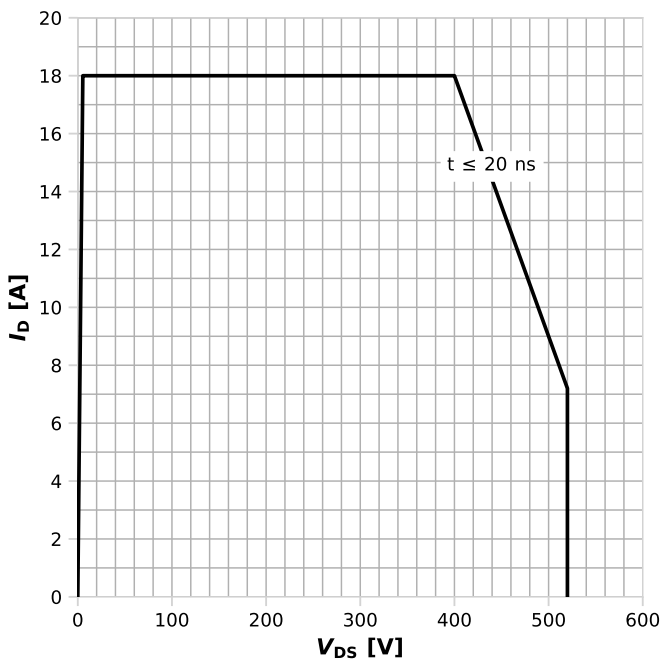
Diagram 5: Repetitive safe operating area	Diagram 6: Repetitive safe operating area
	
I_D=f(V_{DS}); T_C=25°C; T_j≤150°C; parameter: t_p	I_D=f(V_{DS}); T_C=125°C; T_j≤150°C; parameter: t_p

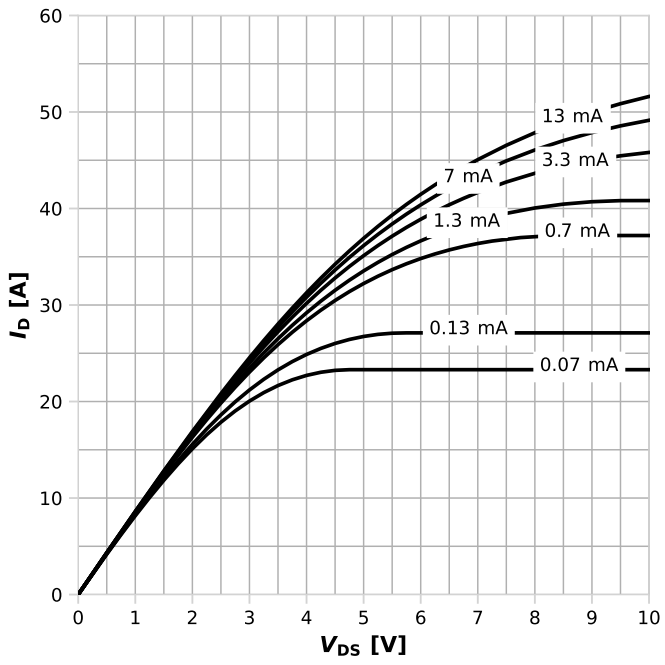
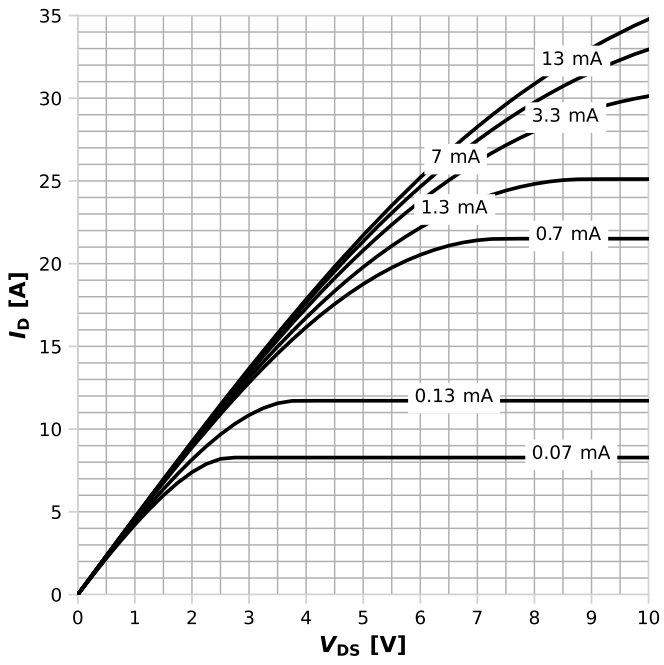
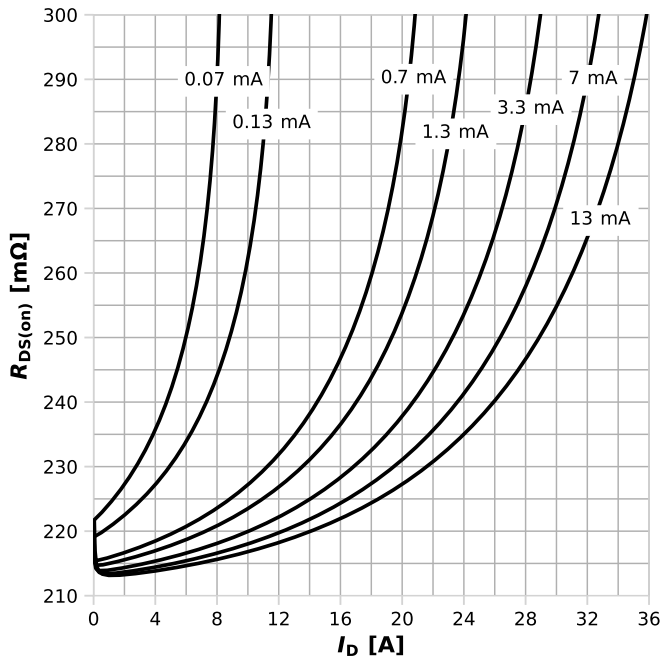
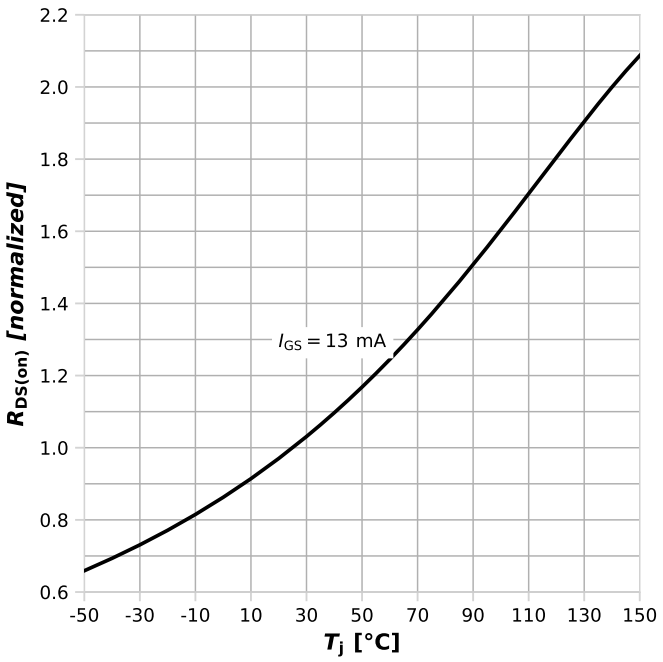
Diagram 7: Typ. static* output characteristics	Diagram 8: Typ. static* output characteristics
	
I_D=f(V_{DS}); T_j=25°C; parameter: I_{GS}; * Refer to gate drive application note	I_D=f(V_{DS}); T_j=125°C; parameter: I_{GS}; * Refer to gate drive application note

Diagram 9: Typ. Drain-source on-state resistance



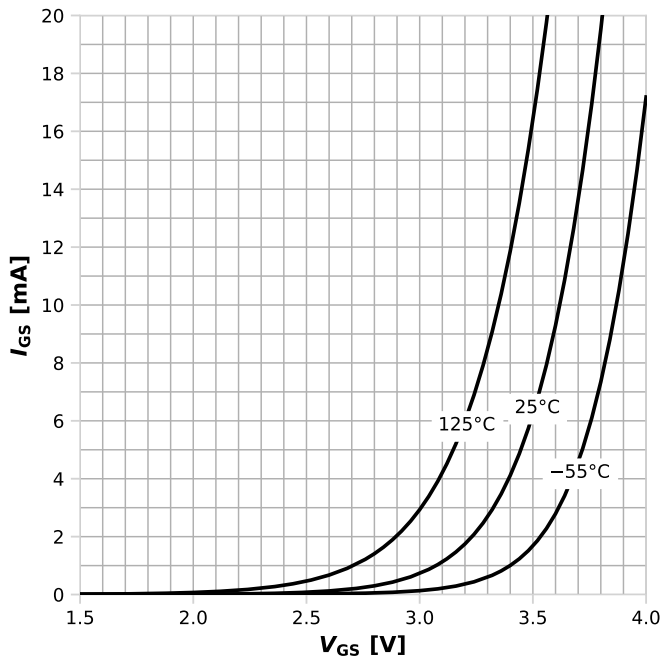
$R_{DS(on)}$=f(I_D); T_j=125°C; parameter: I_{GS}

Diagram 10: Drain-source on-state resistance



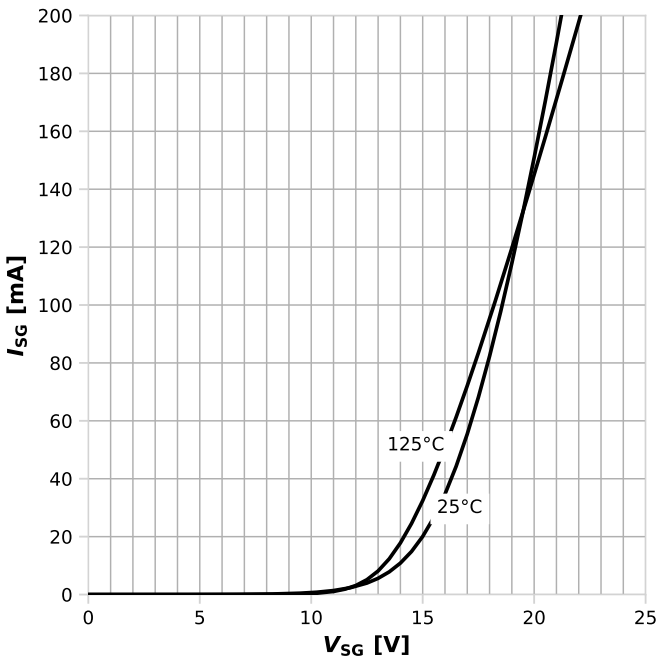
$R_{DS(on)}$=f(T_j); I_D=4.0 A

Diagram 11: Typ. gate characteristics forward



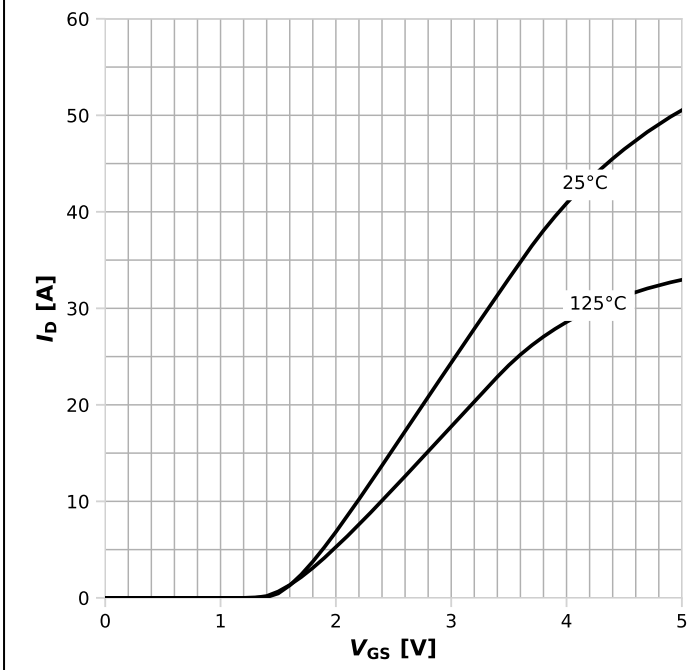
I_{GS}=f(V_{GS}); open drain; parameter: T_j

Diagram 12: Typ. gate characteristics reverse



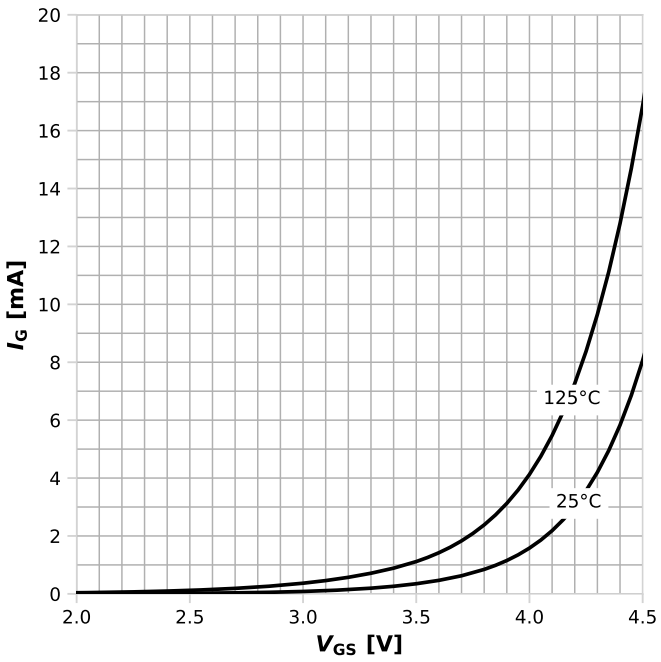
I_{SG}=f(V_{SG}); parameter: T_j

Diagram 13: Typ. transfer characteristics



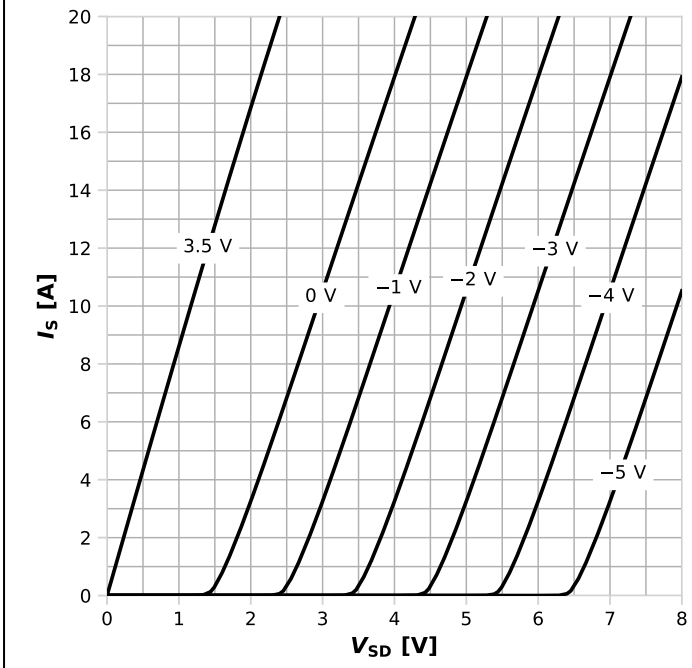
I_D=f(I_{GS}); V_{DS}=8V; parameter: T_j

Diagram 14: Typ. transfer gate current characteristic



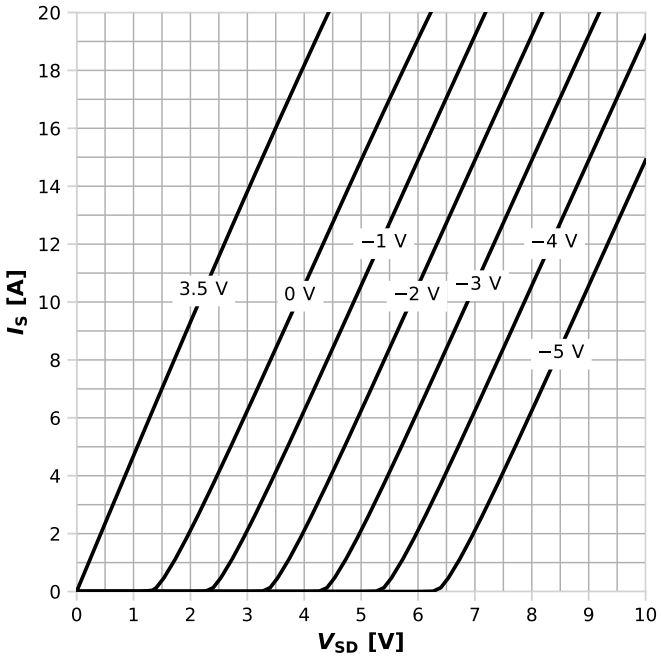
I_G=f(V_{GS}); V_{DS}=8V; parameter: T_j

Diagram 15: Typ. channel reverse characteristics



I_S=f(V_{SD}); T_j=25°C; parameter: V_{GS}

Diagram 16: Typ. channel reverse characteristics



I_S=f(V_{SD}); T_j=125°C; parameter: V_{GS}

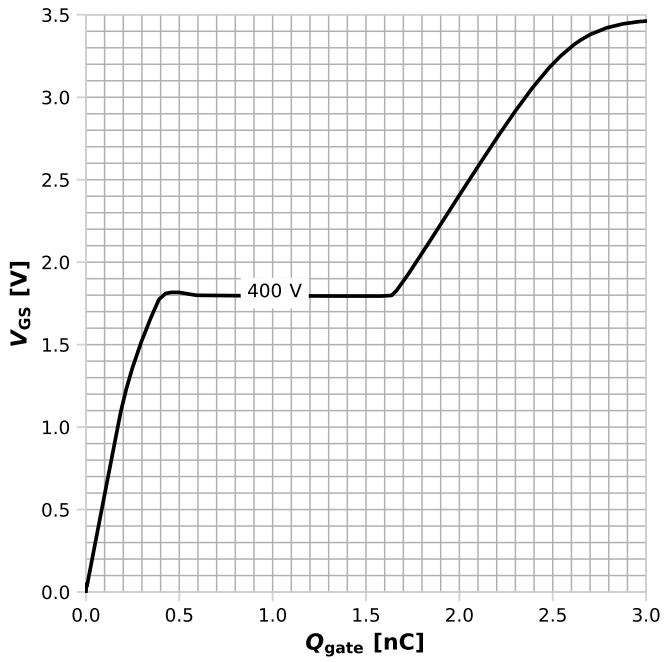
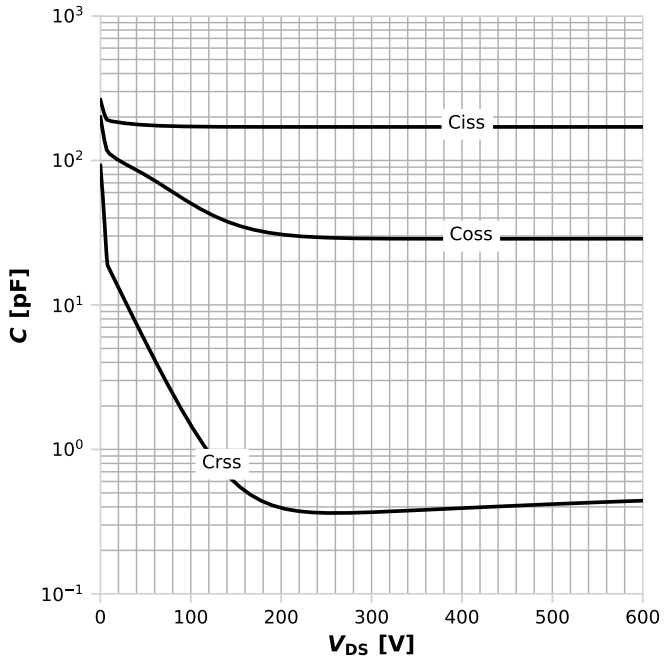
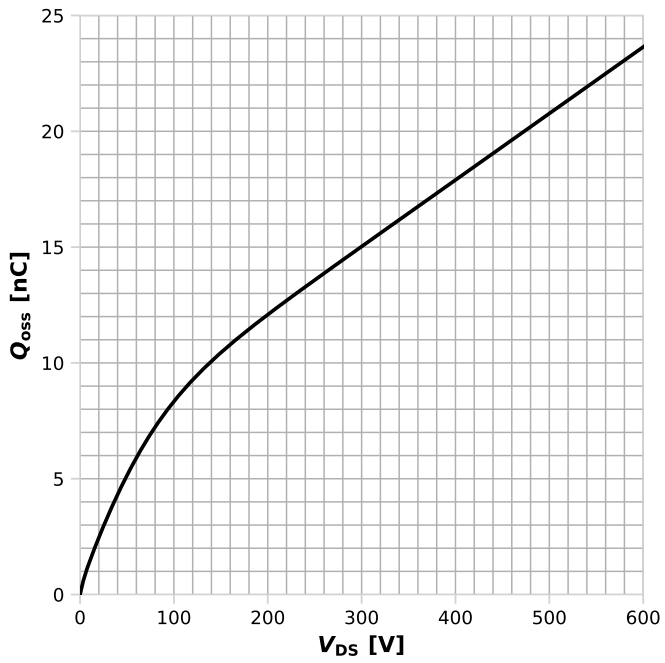
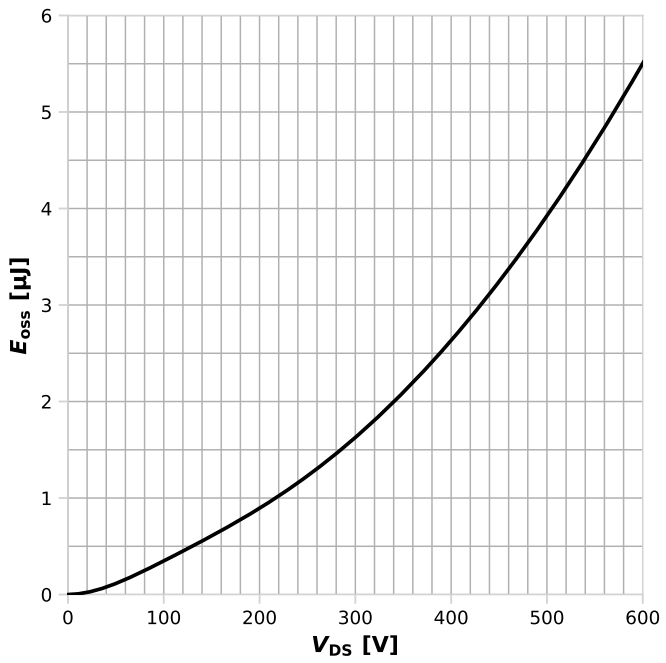
Diagram 17 Typ. gate charge	Diagram 18: Typ. capacitances
	
V_{GS}=f(Q_{gate}); I_D=4.0 A pulsed; I_G=4.5 mA; parameter: V_{DD}	C=f(V_{DS}); V_{GS}=0 V

Diagram 19: Typ. output charge	Diagram 20: Typ. Coss stored energy
	
Q_{oss}=f(V_{DS})	E_{oss}=f(V_{DS})

5 Test circuits

Table 8 Reverse channel characteristics test

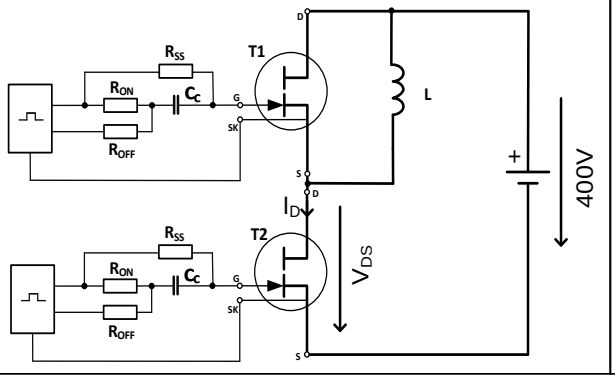
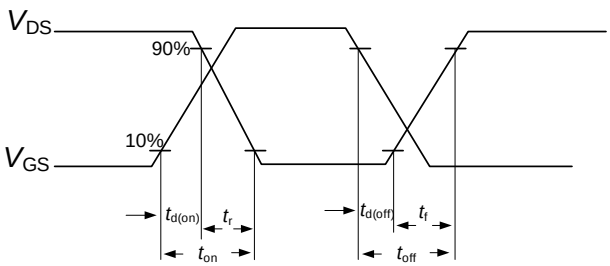
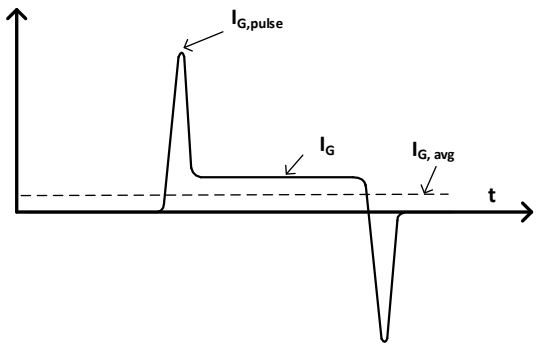
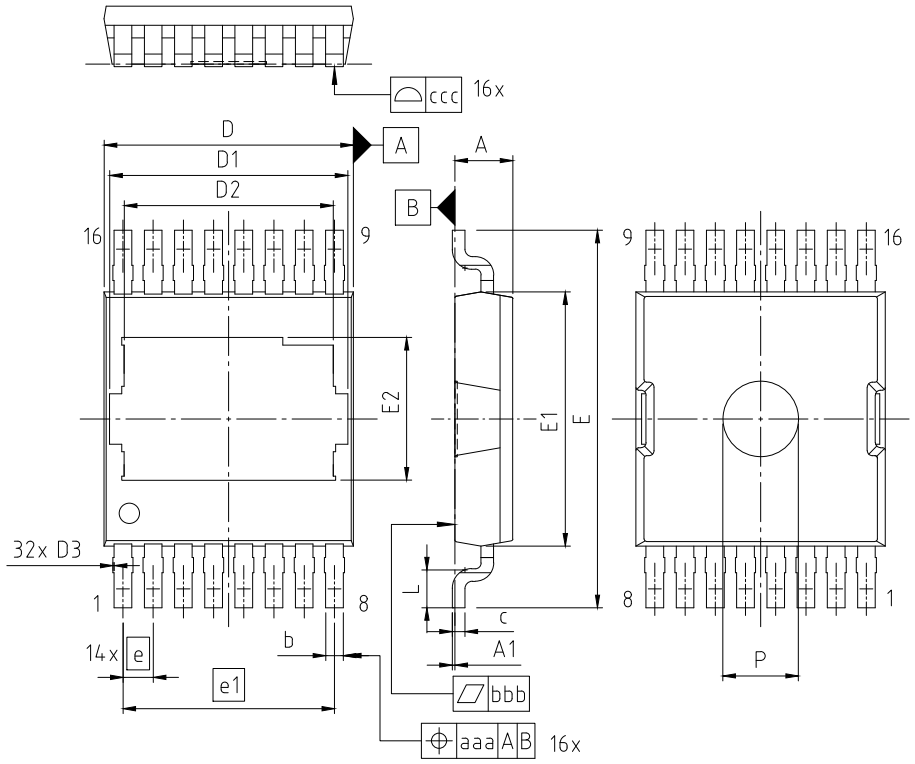
Switching times with inductive load	Switching times waveform
	

Table 9 Gate current switching waveform

Gate current switching waveform


6 Package outlines



PACKAGE - GROUP NUMBER:	PG-HDSOP-16-U05				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	2.25	2.35	e	1.20	
A1	0.01	0.16	e1	8.40	
b	0.60	0.80	L	1.40	1.60
c	0.40	0.60	P	2.90	3.10
D	9.70	10.10	aaa	0.25	
D1	9.46		bbb	0.02	
D2	8.20	8.40	ccc	0.10	
D3	0.15				
E	14.80	15.20			
E1	10.00	10.30			
E2	5.57	5.77			

NOTES:
ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

Figure 1 Outline PG-HDSOP-16, dimensions in mm

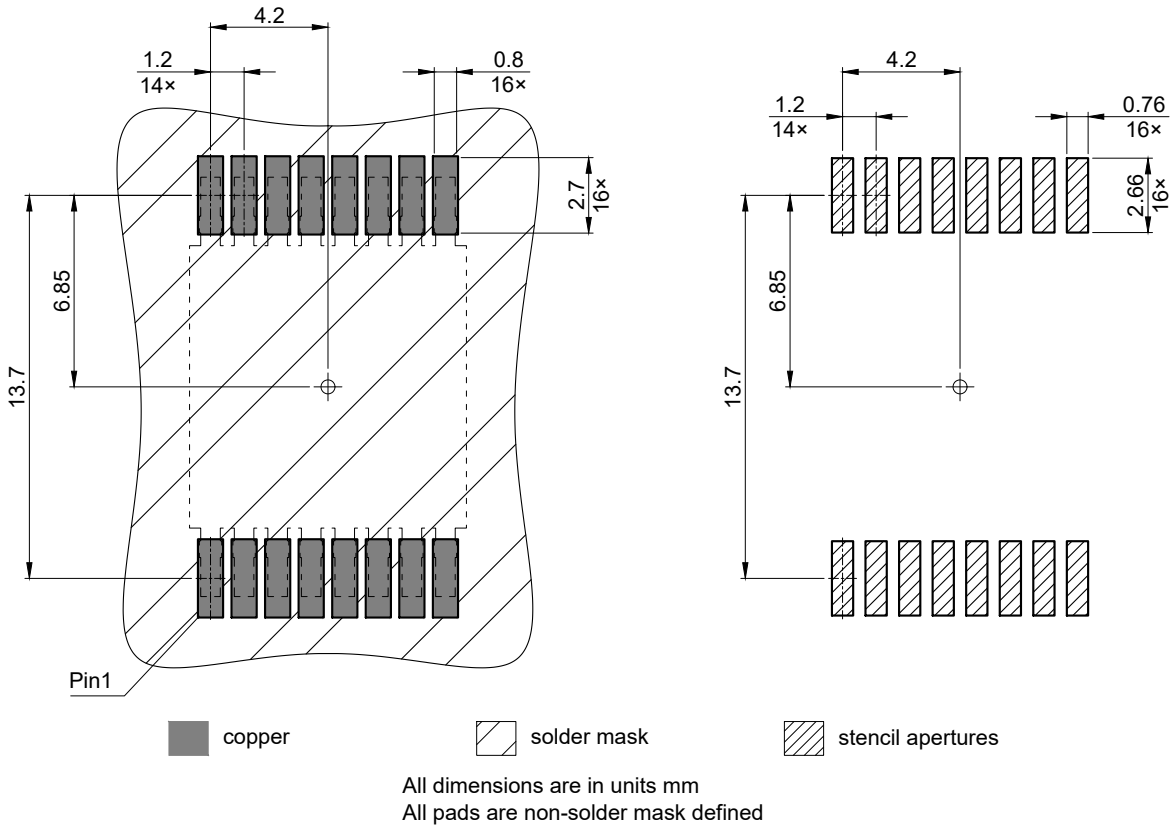


Figure 2 Footprint drawing PG-HDSOP-16, dimensions in mm

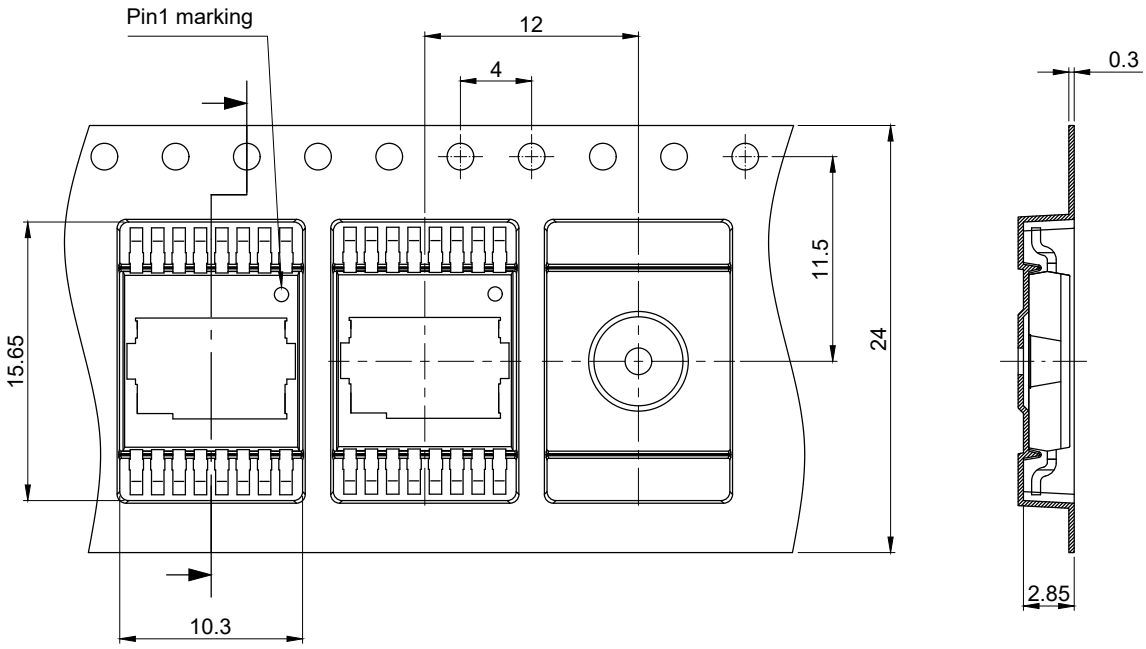


Figure 3 Packaging variant PG-HDSOP-16, dimensions in mm

7 Appendix A

Table 10 Related links

- CoolGaN™ webpage
- CoolGaN™ reliability white paper
- CoolGaN™ gate driver application note
- CoolGaN™ applications information
- Package information

Revision history

IGLT65R110D2

Revision 2026-03-03, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-10-29	Release of final
1.1	2026-03-03	Updated formatting, package and footprint drawings, and footnotes. Added typical gate current $I_{G,avg}$ in Table 2.

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