2.5 V/3.3 V 3.0 GHz Differential 1:4 LVPECL Fanout Buffer

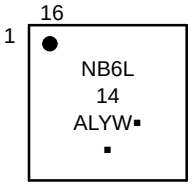
Multi−Level Inputs with Internal Termination

NB6L14

1

QFN−16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

Description

The NB6L14 is a 3.0 GHz differential 1:4 LVPECL clock or data fanout buffer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. This feature allows the NB6L14 to accept various logic standards, such as LVPECL, LVCMOS, LVTTL, CML, or LVDS logic levels. The VREF_AC reference output can be used to rebias capacitor−coupled differential or single−ended input signals. The 1:4 fanout design was optimized for low output skew applications.

The NB6L14 is a member of the ECLinPS MAX™ family of high performance clock and data management products.

Features

- Input Clock Frequency > 3.0 GHz
- Input Data Rate > 2.5 Gb/s
- < 20 ps Within Device Output Skew
- 350 ps Typical Propagation Delay
- 150 ps Typical Rise and Fall Times
- Differential LVPECL Outputs, 700 mV Amplitude, Typical
- LVPECL Mode Operating Range: V_{CC} = 2.375 V to 3.63 V with GND = 0 V
- Internal 50 Ω Input Termination Resistors Provided
- VREF_AC Reference Output Voltage
- −40°C to +85°C Ambient Operating Temperature
- Available in 3 mm x 3 mm 16 Pin QFN
- These are Pb−Free Devices

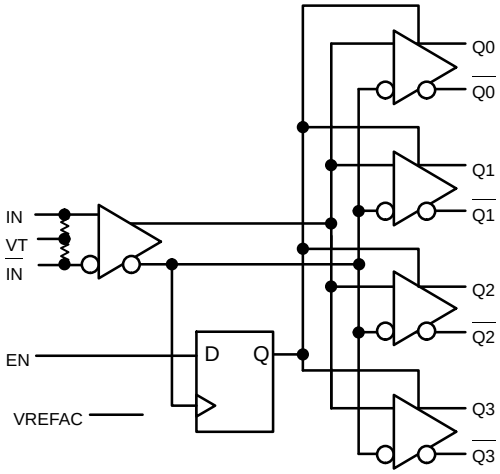


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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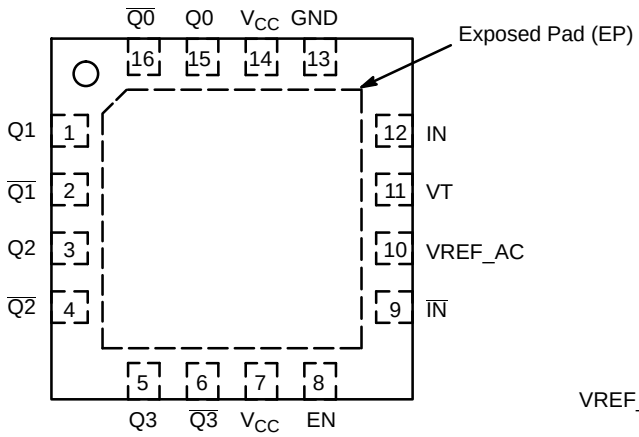

Figure 2. QFN−16 Pinout
(Top View)

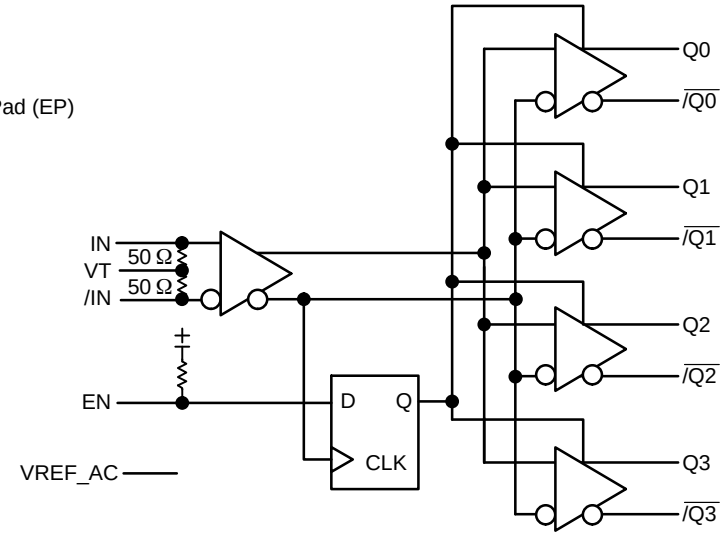

Figure 3. Logic Diagram

Table 1. EN TRUTH TABLE

IN	$\overline{IN}$	EN	Q0:Q3	$\overline{Q0}$:$\overline{Q3}$
0	1	1	0	1
1	0	1	1	0
x	x	0	0+	1+

+ = On next negative transition of the input signal (IN).
x = Don't care.

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q1	LVPECL Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}–2.0 V.
2	$\overline{Q1}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
3	Q2	LVPECL Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
4	$\overline{Q2}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
5	Q3	LVPECL Output	Non−inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
6	$\overline{Q3}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC} – 2.0 V.
7	V_{CC}	−	Positive Supply Voltage
8	EN	LVTTL/LVCMOS	Synchronous Output Enable. When LOW, Q outputs will go LOW and $\overline{Q}$ outputs will go HIGH on the next negative transition of IN input. The internal DFF register is clocked on the falling edge of IN input (see Figure 20). The EN pin has an internal pullup resistor and defaults HIGH when left open.
9	$\overline{IN}$	LVPECL, CML, LVDS, HSTL	Inverted Differential Clock Input. Internal 50 Ω Resistor to Termination Pin, VT.
10	VREF_AC		Output Voltage Reference for capacitor−coupled inputs, only.
11	VT		Internal 100 Ω center−tapped Termination Pin for IN and $\overline{IN}$.
12	IN	LVPECL, CML, LVDS, HSTL	Non−inverted Differential Clock Input. Internal 50 Ω Resistor to Termination Pin, VT.
13	GND	−	Negative Supply Voltage
14	V_{CC}	−	Positive Supply Voltage
15	Q0	LVPECL Output	Noninverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}–2.0 V.
16	$\overline{Q0}$	LVPECL Output	Inverted Differential Output. Typically Terminated with 50 Ω Resistor to V_{CC}–2.0 V.
−	EP	−	The Exposed Pad (EP) on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

1. In the differential configuration when the input termination pin VT, is connected to a common termination voltage or left open, and if no signal is applied on IN/$\overline{IN}$ inputs, then the device will be susceptible to self−oscillation.

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Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 4 kV > 100 V
Moisture Sensitivity (Note 2)	QFN−16	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		167
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.0	V
V_{Io}	Positive Input/Output	GND = 0 V	$-0.5\ V \le V_{Io} \le V_{CC} + 0.5\ V$	4.0	V
I_{IN}	Input Current Source or Sink Current (IN/$\overline{IN}$)			±50	mA
I_{VREF_AC}	Source or Sink Current on VT Pin			±2.0	mA
I_{OUT}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	QFN−16 QFN−16	42 35	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	QFN−16	4	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 5. DC CHARACTERISTICS, Multi−Level Inputs, LVPECL Outputs
V_{CC} = 2.375 V to 3.63 V, GND = 0 V, T_A = −40°C to +85°C

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Inputs and Outputs Open)	35	47	65	mA
LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS					
V_{OH}	Output HIGH Voltage (Notes 4 and 5) (Q, $\overline{Q}$) V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 1145 2155 1355	V_{CC} − 1020 2280 1480	V_{CC} − 895 2405 1605	mV
V_{OL}	Output LOW Voltage (Notes 4 and 5) (Q, $\overline{Q}$) V_{CC} = 3.3 V V_{CC} = 2.5 V	V_{CC} − 1945 1355 555	V_{CC} − 1875 1475 675	V_{CC} − 1695 1605 805	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (See Figures 10 and 11)					
V_{th}	Input Threshold Reference Voltage Range (Note 6)	1100		V_{CC} − 100	mV
V_{IH}	Single−Ended Input High Voltage	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 100	mV
V_{ISE}	Single−Ended Input Voltage Amplitude (V_{IH} − V_{IL})	200		V_{CC} − GND	mV
V_{REFAC}					
V_{REFAC}	Output Reference Voltage (V_{CC} ≥ 2.5 V)	V_{CC} − 1.525	V_{CC} − 1.425	V_{CC} − 1.325	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (See Figures 12 and 13) (Note 7)					
V_{IHD}	Differential Input HIGH Voltage	1200		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{IHD} − 100	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 8)	950		V_{CC} – 50	mV
V_{ID}	Differential Input Voltage (IN−$\overline{IN}$) (V_{IHD}–V_{ILD})	100		V_{CC} − GND	mV
I_{IH}	Input HIGH Current IN/$\overline{IN}$ (VT Open)	−150		+150	μA
I_{IL}	Input LOW Current IN/$\overline{IN}$ (VT Open)	−150		+150	μA
LVTTL/LVCMOS INPUT DC ELECTRICAL CHARACTERISTICS					
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage	GND		0.8	V
I_{IH}	Input HIGH Current, V_{CC} = V_{IN} = 3.63 V	−10		50	μA
I_{IL}	Input LOW Current, V_{CC} = 3.63 V, V_{IN} = 0 V	−150		0	μA
TERMINATION RESISTORS					
R_{TIN}	Internal Input Termination Resistor (IN to VT)	40	50	60	Ω
R_{DIFF_IN}	Differential Input Resistance (IN to $\overline{IN}$)	80	100	120	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. LVPECL outputs loaded with 50 Ω to V_{CC} − 2.0 V for proper operation.
5. Input and output parameters vary 1:1 with V_{CC}.
6. V_{th} is applied to the complementary input when operating in single−ended mode.
7. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
8. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.

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Table 6. AC CHARACTERISTICS V_{CC} = 2.375 V to 3.63 V, GND = 0 V, T_A = −40°C to +85°C (Note 9)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (Note 10) $f_{IN} \le 1.25$ GHz 1.25 GHz ≤ f_{in} ≤ 2.0 GHz 2.0 GHz ≤ f_{in} ≤ 3.0 GHz	 550 380 250	 700 500 320		mV
f_{DATA}	Maximum Operating Data Rate		2.5		Gb/s
t_{PD}	Propagation Delay IN to Q	250	370	500	ps
t_S	Set−Up Time (Note 11) EN to IN, $\overline{IN}$	300			ps
t_H	Hold Time (Note 11) EN to IN, $\overline{IN}$	300			ps
t_{SKEW}	Within−Device Skew (Note 12) Device to Device Skew (Note 13)		5.0	20 150	ps
t_{JITTER}	RMS Random Jitter (Note 14) f_{IN} = 2.5 GHz Peak−to−Peak Data Dependent Jitter (Note 15) f_{DATA} = 2.5 Gb/s		 14	1.0	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 10)	100		V_{CC} − GND	mV
t_r,t_f	Output Rise/Fall Times @ Full Output Swing (20%−80%)	70	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

9. Measured by forcing V_{INPP} (min) from a 50% duty cycle clock source. All loading with an external R_L = 50 Ω to V_{CC} – 2.0 V. Input edge rates 40 ps (20%−80%).
10. Input and output voltage swing is a single−ended measurement operating in differential mode.
11. Set−up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set−up and hold times do not apply.
12. Within device skew is measured between two different outputs under identical power supply, temperature and input conditions.
13. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.
14. Additive RMS jitter with 50% duty cycle clock signal.
15. Additive peak−to−peak data dependent jitter with input NRZ data at PRBS $2^{\wedge 23}$−1 and K28.5 at 2.5Gb/s.

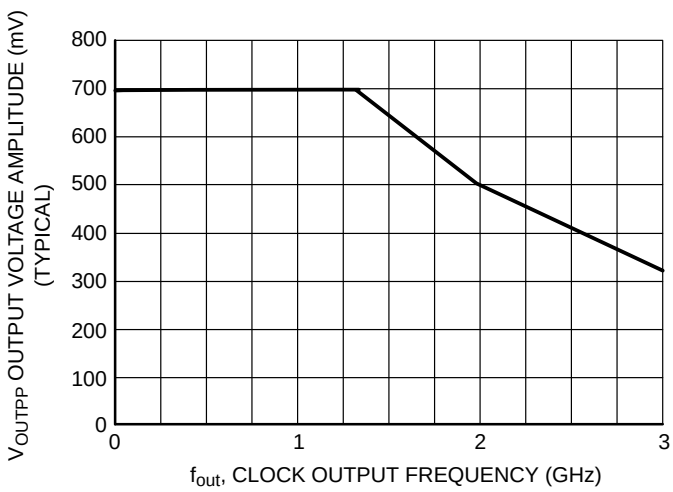

Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Output Frequency at Ambient Temperature (Typical)

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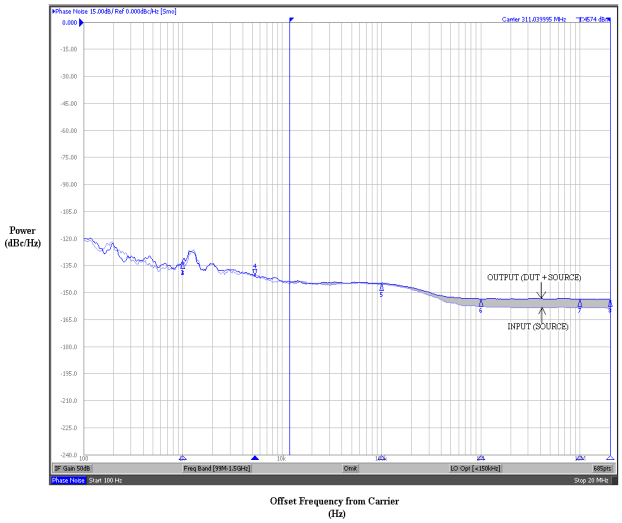

Figure 5. Typical Phase Noise Plot at $f_{carrier}$ = 311.04 MHz

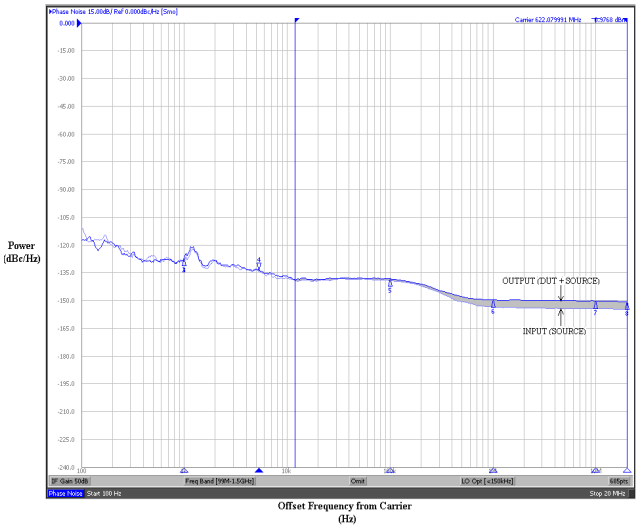

Figure 6. Typical Phase Noise Plot at $f_{carrier}$ = 622.08 MHz

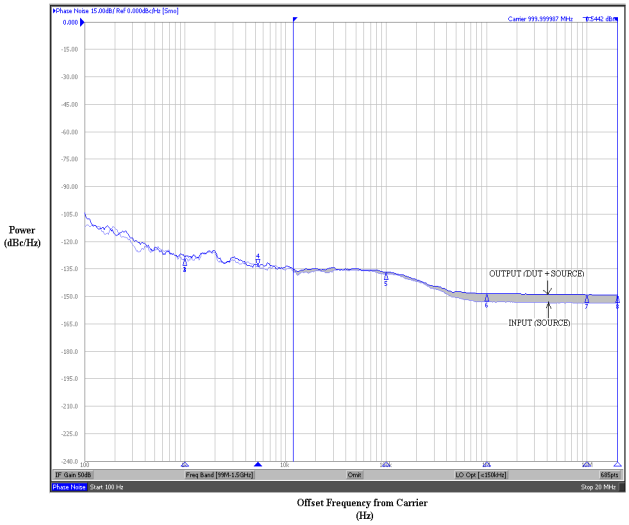

Figure 7. Typical Phase Noise Plot at $f_{carrier}$ = 1 GHz

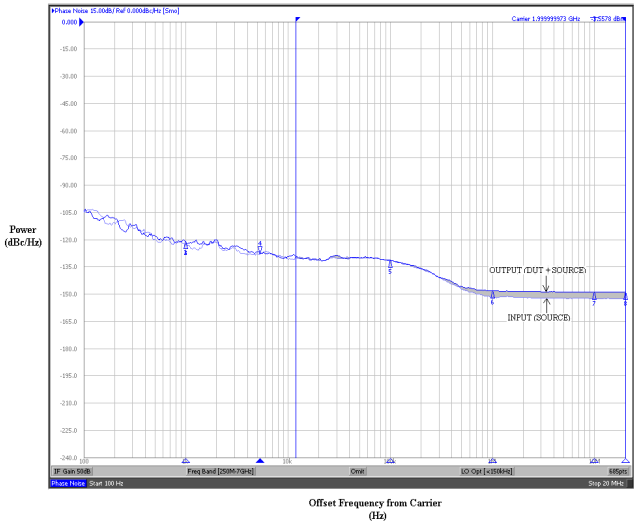

Figure 8. Typical Phase Noise Plot at $f_{carrier}$ = 2 GHz

The above phase noise plots captured using Agilent E5052A show additive phase noise of the NB6L14 device at frequencies 311.04 MHz, 622.08 MHz, 1 GHz and 2 GHz respectively at an operating voltage of 3.3 V in room temperature. The RMS Phase Jitter contributed by the device (integrated between 12 kHz and 20 MHz; as shown in the shaded region of the plot) at each of the frequencies is 27 fs, 17 fs, 13 fs and 5 fs respectively. The input source used for the phase noise measurements is Agilent E8663B.

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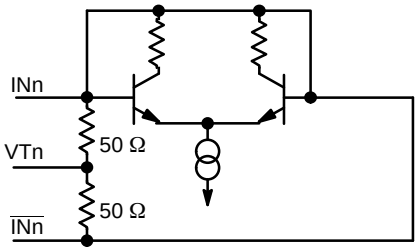

Figure 9. Input Structure

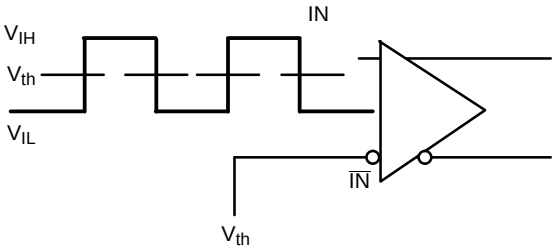

Figure 10. Differential Input Driven Single−Ended

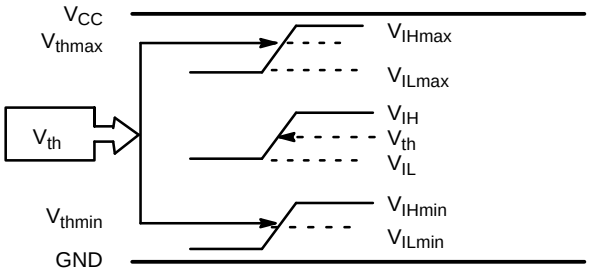

Figure 11. V_{th} Diagram

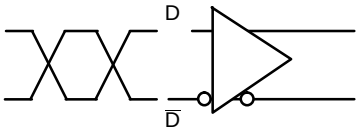

Figure 12. Differential Inputs Driven Differentially

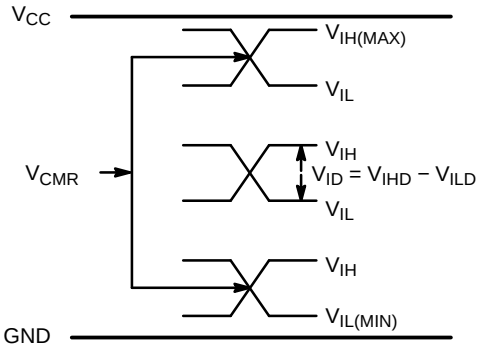

Figure 13. V_{CMR} Diagram

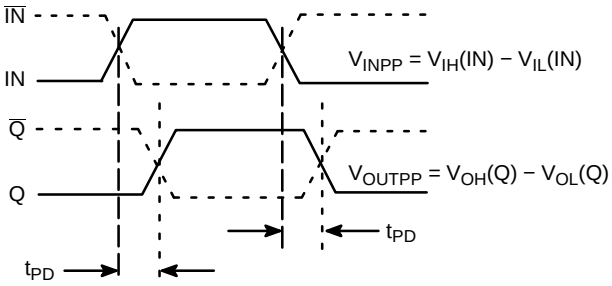

Figure 14. AC Reference Measurement

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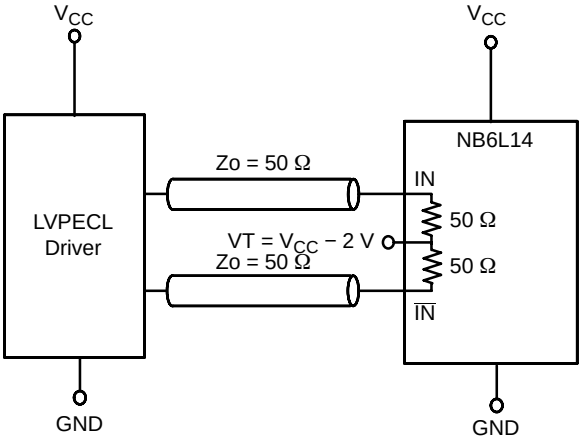

Figure 15. LVPECL Interface

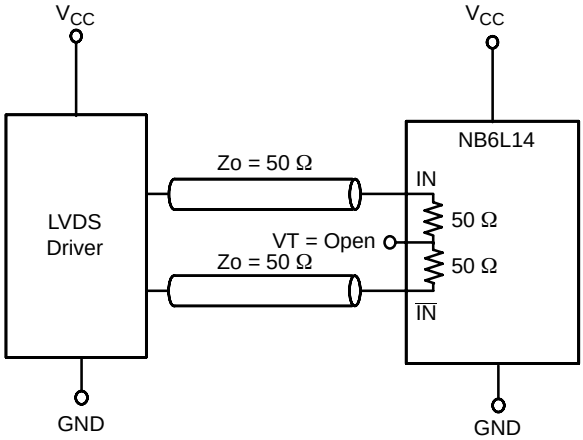

Figure 16. LVDS Interface

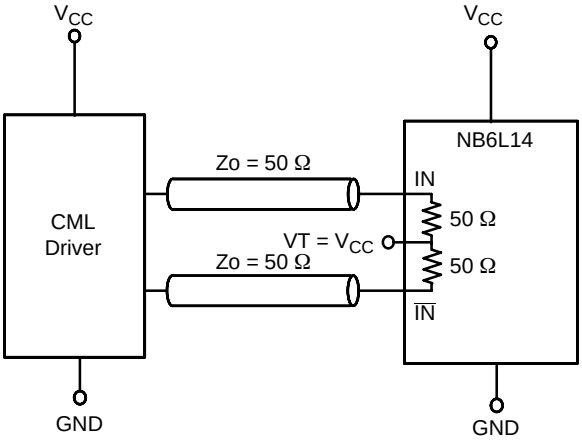

Figure 17. Standard 50 Ω Load CML Interface

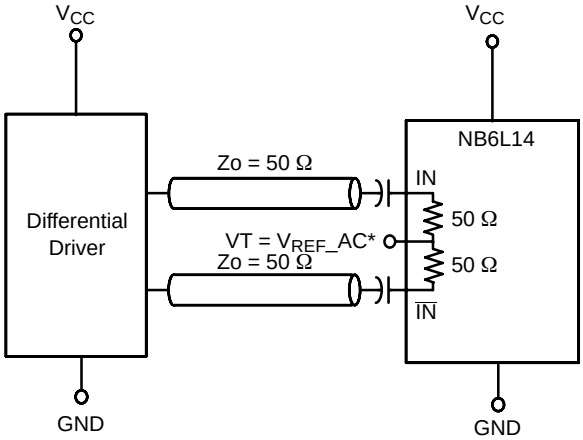

Figure 18. Capacitor−Coupled Differential Interface (VT Connected to V_{REFAC})

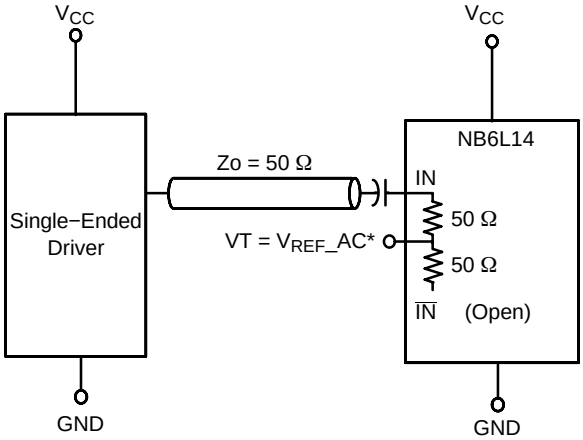

Figure 19. Capacitor−Coupled Single−Ended Interface (VT Connected to V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

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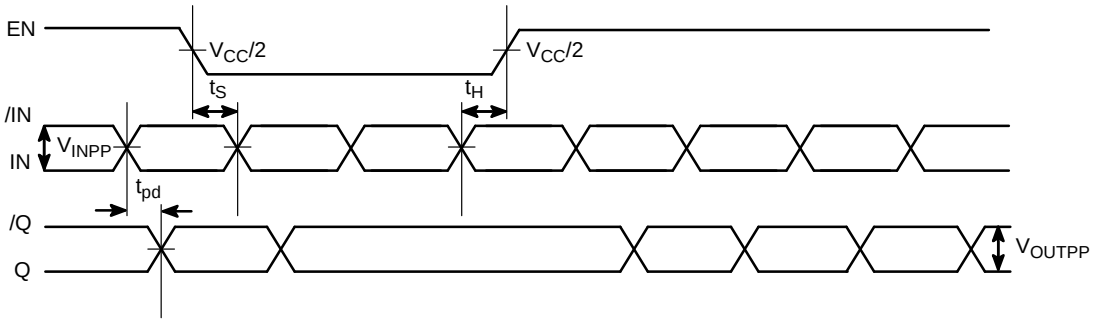

Figure 20. EN Timing Diagram

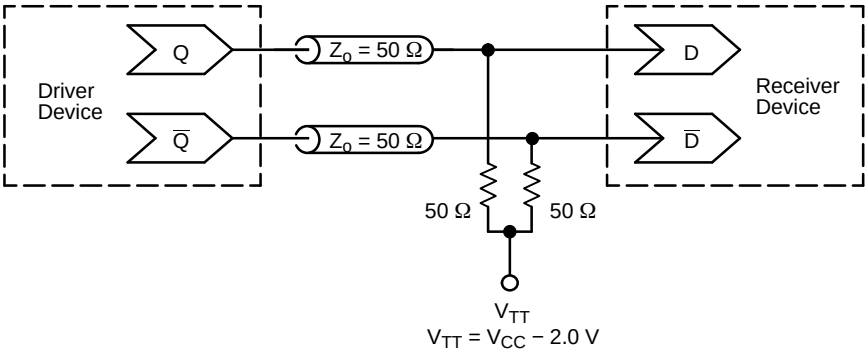

Figure 21. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
NB6L14MNG	QFN−16, 3x3 mm (Pb−Free)	123 Units / Rail
NB6L14MNR2G	QFN−16, 3x3 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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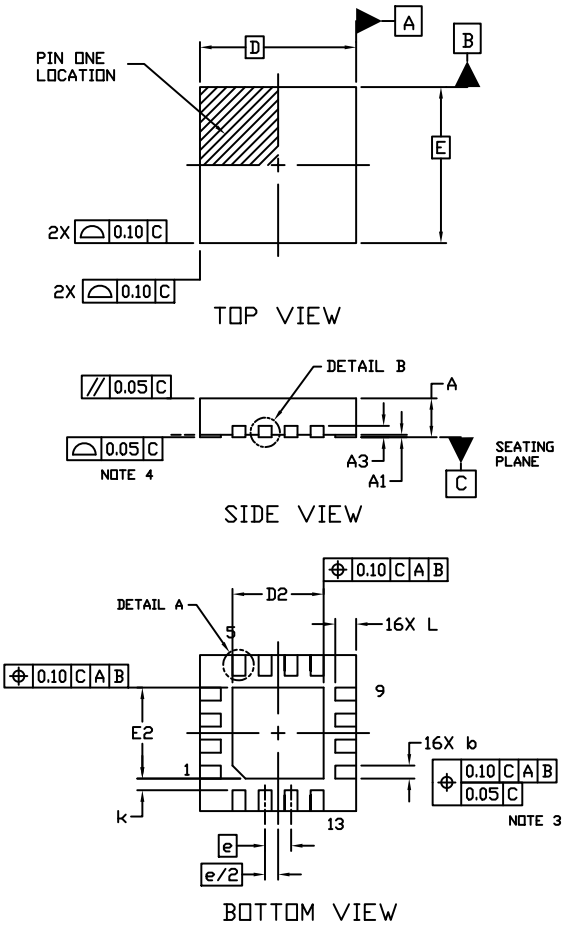
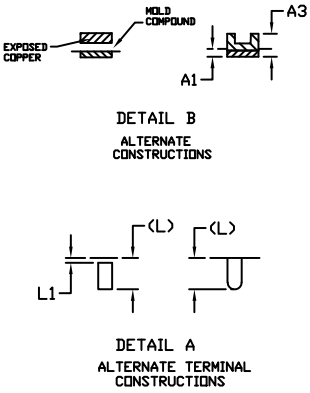
QFN16 3x3, 0.5P
CASE 485G
ISSUE G

1
SCALE 2:1

DATE 08 OCT 2021

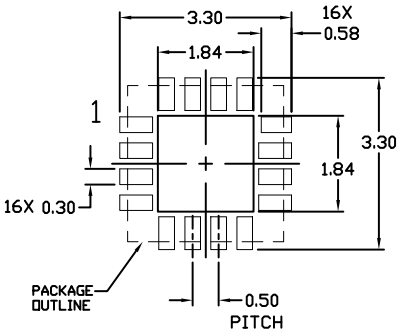


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*

XXXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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