SiI9777CLUC Product Family Qualification Summary

Lattice (Silicon Image) Document # SII-RS-02001 March 2016

Dear Customer,

Enclosed is Lattice (Silicon Image) Semiconductor's SiI9777CLUC Product Family Qualification Summary Report.

This report was created to assist you in the decision making process of selecting and using our products. The information contained in this report represents the entire qualification effort for this device family.

The information is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

Your feedback is valuable to Lattice (Silicon Image). If you have suggestions to improve this report, or the data included, we encourage you to contact your Lattice (Silicon Image) representative.

Sincerely,

James M. Orr
Vice President,
Corporate Quality
Lattice Semiconductor Corporation

Contents

INTRODUCTION

The Lattice (Silicon Image) SiI9777CLUC is a versatile High Definition Multimedia Interface 2.0 (HDMI®) transmitter/port processor, with support for Mobile High-Definition Link 3 (MHL®) and High-bandwidth Digital Content Protection 2.2 (HDCP). The device's 18 Gb/s transmitter and receiver features support delivery of full resolution 4K Ultra High Definition (UltraHD) 4:4:4 video to a 4K television set at 50 Hz or 60 Hz frame rate.

As port processor, all four inputs support HDMI 2.0 at up to 18 Gb/s, and two of the inputs can also support MHL 3 input at resolutions of up to 4K @30 Hz. The three outputs offer a flexible configuration, including the ability to split an 18 Gb/s signal into two 9 Gb/s outputs. Audio and video can be routed to separate transmitters and two separate 300 MHz output streams can be routed from two input sources. As a transmitter, the SiI9777CLUC supports one output with HDMI 2.0 at up to 18 Gb/s with HDCP 2.2. A second output offers legacy-compatible HDMI 1.4 with audio output only.

In transmitter configuration, the SiI9777CLUC can merge two video input streams up to 9 Gb/s each into one 18 Gb/s output stream. This is useful to merge two 300 MHz input streams that contain one-half of a 4K × 2K @ 60 Hz 4:4:4 frame each, into one 18 Gb/s, 600 Mega-characters/second/channel (Mcsc) stream with HDCP 2.2.

As a transmitter, the SiI9777CLUC can also convert certain types of reduced blanking formats such as a 337 MHz TMDS™ input of 10-bit 4K @ 60 Hz 4:2:0 into an HDMI 2.0 standard 4K @ 60 Hz 4:2:2 10-bit output with HDCP 2.2. This enables the design of a set-top box that can deliver full quality, 10-bit UltraHD with HDCP 2.2, using a decoder circuit built with HDMI 1.4 technology.
The SiI9777CLUC implements the HDCP 2.2 Specification to protect the delivery of premium content. HDCP 2.2 can be applied in transmitter, receiver, and repeater configurations. HDCP 1.4 support is also included, allowing the transmitter to interoperate with the installed base of legacy source devices.

The SiI9777CLUC transmitter/port processor supports AVR compatibility mode, which enables it to output audio/video content through one transmitter with HDCP 1.4 or 2.2 content protection, while the second transmitter outputs audio-only content through a transmitter with HDCP 1.4 protection.

An internal Microcontroller Unit (MCU) greatly simplifies software development and reduces the amount of I2C data transactions required to control the transmitter. The MCU firmware is loaded into the transmitter from external SPI flash at reset. A slim programming interface allows host control with minimal software effort.

LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #SiI-QA-0007). All product qualification plans are generated in conformance with Lattice Semiconductor's (Silicon Image) Qualification Procedure (Doc. # SiI-QA-0007) with failure analysis performed in conformance with Lattice Semiconductor's (Silicon Image) Failure Analysis Procedure (Doc. #SiI-QA-0045). Both documents are referenced in Lattice Semiconductor's (Silicon Image) Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8D process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

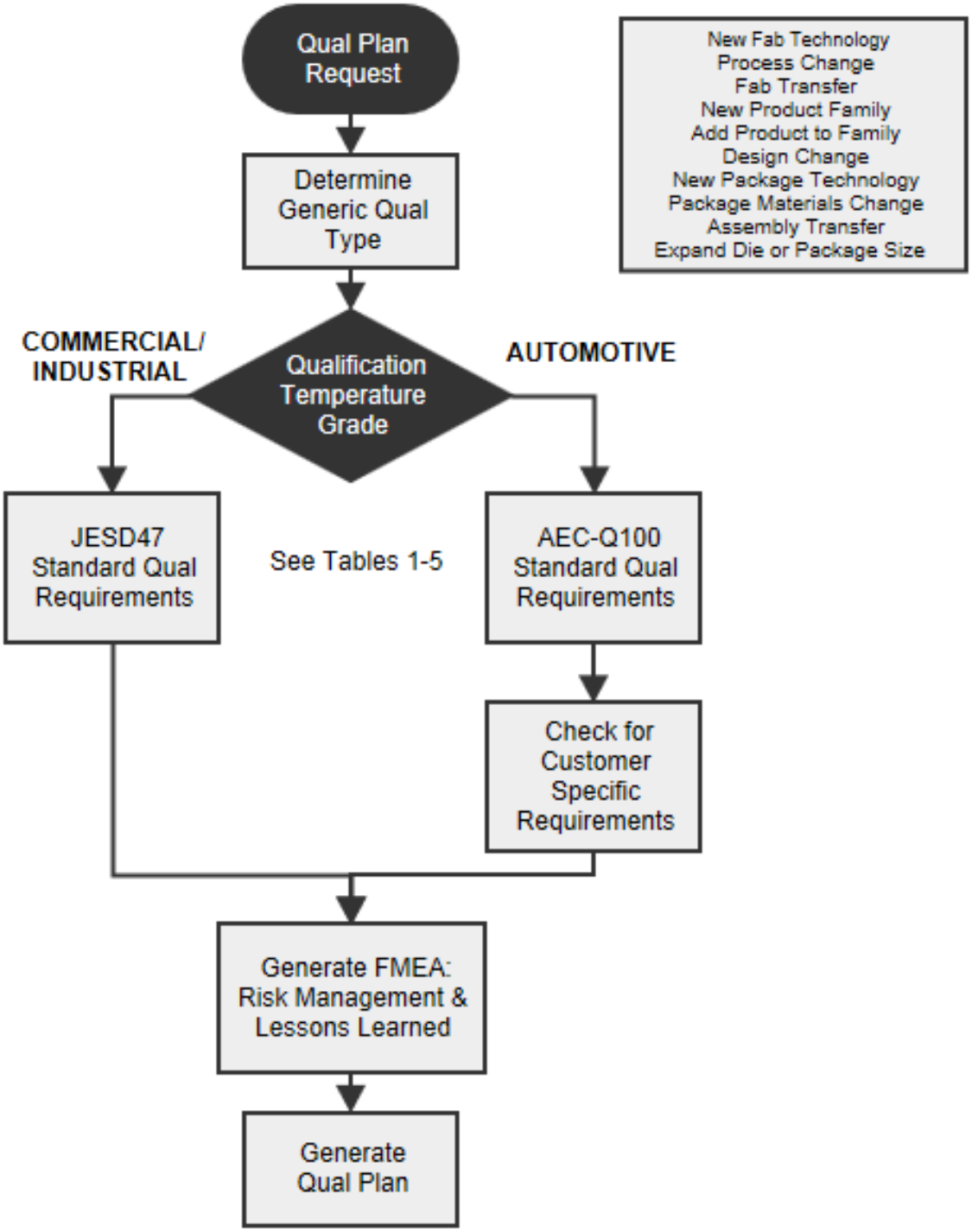
Product families are qualified based upon the requirements outlined in Table#1. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice (Silicon Image) Reliability Monitor Report which can be obtained upon request.

Lattice (Silicon Image) Standard Product Qualification Process Flow

This diagram represents the standard qualification flow used by Lattice (Silicon Image) to qualify new Product Families. The target end market for the Product Family determines which flow options are used. The SiI9777CLUC Product Family was qualified using the Commercial Option.

Figure1



Standard Qualification Testing

Table#1

TEST	STANDARD	TEST CONDITIONS
High Temperature Operating Life (HTOL)	JESD22-A108D	125°C Ambient and max operating supplies
Human Body Model ESD (HBM)	JESD22-A114F	25°C (Technology/Device dependent Performance Targets)
Machine Body Model ESD (MM)	JESD22-A115C	25°C (Technology/Device dependent Performance Targets)
Charged Device Model ESD (CDM)	JESD22-C101E	25°C (Technology/Device dependent Performance Targets)
Latch-Up (LU)	JESD78D	Class II, +/-200mA trigger current and AMR operating supplies

QUALIFICATION DATA FOR SII9777CLUC PRODUCT

Product Family: SiI9777CLUC
Packages offered: 208 LQFP
Process Technology Node: 55nm, 1P7M
Process Technology Fab: TSMC Fab.14

SiI9777CLUC Product Life (HTOL) Data

High Temperature Operating Life (HTOL) Test:

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JESD22-A108D "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at specified voltages as described in test conditions for each device type.

The Early Life Failure Rate (ELFR) test uses large samples sizes for a short duration (48hrs ≤ t ≤ 168 hrs) HTOL stress to determine the infant mortality rate of a device family.

Life Test (HTOL) Conditions:
Stress Duration: 168, 500, 1000 hours
Stress Conditions: Max operating supplies, Ambient = 125°C
Method: JESD22-A108D

SiI9777CLUC Product Life Results

Rev. ID	Lot #	SiI9777CLUC
1.1	P6R465.13XYT	0/77
1.2	P4FAAD4.01Q	0/77

SiI9777 Cumulative Life Testing Device Hours = 144,000
SiI9777 Result / Sample Size = 0 / 144
SiI9777 FIT Rate = 81.76 FIT
FIT Assumptions: CL=60%, AE=0.7eV, Tjref=55C

SiI9777 HTOL (168 Hrs) Cumulative Result / Sample Size = 0 / 144
SiI9777 HTOL (500 Hrs) Cumulative Result / Sample Size = 0 / 144
SiI9777 HTOL (1000 Hrs) Cumulative Result / Sample Size = 0 / 144
Test Chip Cumulative Sample Size = 0 / 144

SiI9777CLUC Product – ESD and Latch Up Data

Electrostatic Discharge-Human Body Model:

The SiI9777CLUC product was tested per JESD22-A114F Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI9777CLUC ESD-HBM Data

Rev. ID	Lot #	SiI9777CLUC
1.1	P6R465.13XYT	2000V
1.2	P4FAAD4.01Q	2000V

HBM classification for Commercial/Industrial products, per JESD22-A114F.
All HBM levels indicated are dual-polarity (±).
HBM worst-case performance is the package with the smallest RLC parasitics.

Electrostatic Discharge-Machine Model:

The SiI9777CLUC product was tested per JESD22-A115C Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM) procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI9777CLUC ESD-MM Data

Rev. ID	Lot #	SiI9777CLUC
1.1	P6R465.13XYT	150V
1.2	P4FAAD4.01Q	150V

MM classification for Commercial/Industrial products, per JESD22-A115C.
All MM levels indicated are dual-polarity (±).
MM worst-case performance is the package with the smallest RLC parasitic.

Electrostatic Discharge-Charged Device Model:

The SiI9777CLUC product family was tested per the JESD22-C101E, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI9777CLUC ESD-CDM Data

Rev. ID	Lot #	SiI9777CLUC
1.1	P6R465.13XYT	500V
1.2	P4FAAD4.01Q	500V

CDM classification for Commercial/Industrial products, per JESD22-C101E.
All CDM levels indicated are dual-polarity (±).
CDM worst-case performance is the package with the largest bulk capacitance.

Latch-Up:

The SiI9777CLUC product was tested per the JESD78D IC Latch-up Test procedure.

All units were tested at room ambient prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

SiI9777CLUC Latch-up Data

Rev. ID	Lot #	SiI9777CLUC
Rev1.1	P6R465.10XX	200mA
Rev1.2	P4FAAD4.01Q	200mA

I-Test classification for Commercial/Industrial products, per JESD78D.
All I-Test levels indicated are dual-polarity (±).
I-Test worst-case performance is the package with access to the most IOs.

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